Integrated Circuit Systems, Inc.

ICS86953I

LOW SKEW, 1-TO-9 DIFFERENTIAL-TO-LVCMOS / LVTTL ZERO DELAY BUFFER

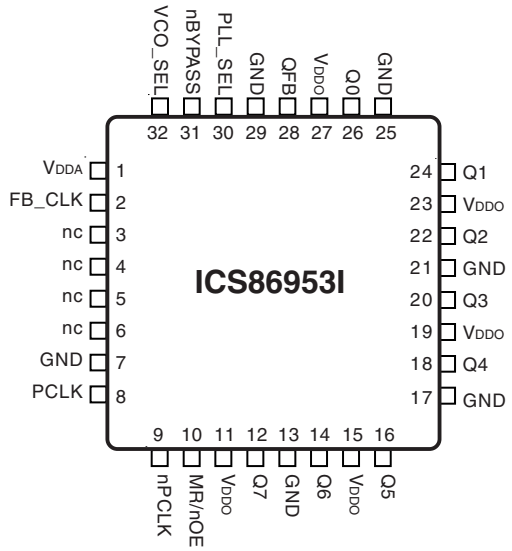
GENERAL DESCRIPTION

The ICS86953I is a low voltage, low skew 1-to-9 Differential-to-LVCMOS/LVTTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The PCLK, nPCLK pair can accept most standard differential input levels. With output frequencies up to 110MHz, the ICS86953I is targeted for high performance clock applications. Along with a fully integrated PLL, the ICS86953I contains frequency configurable outputs and an external feedback input for regenerating clocks with "zero delay".

FEATURES

- 9 single ended LVCMOS/LVTTL outputs; (8) clocks, (1) feedback
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, CML, SSTL
- Maximum output frequency: PLL Mode, 110MHz
- VCO range: 200MHz to 500MHz
- Output skew: 75ps (maximum)
- Cycle-to-cycle jitter: 50ps (maximum)
- Static phase offset: 90ps ± 110ps
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Pin compatible to the MPC953

PIN ASSIGNMENT



32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y package
Top View

BLOCK DIAGRAM

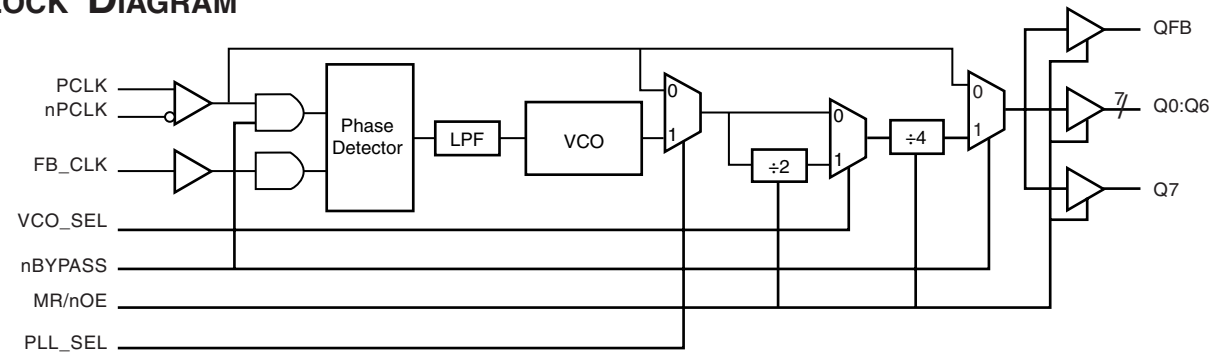


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	FB_CLK	Input	Pullup	Feedback clock input. LVCMOS / LVTTL interface levels.
3, 4, 5, 6	nc	Unused		No connect.
7, 13, 17, 21, 25, 29	GND	Power		Power supply ground.
8	PCLK	Input	Pullup	Non-inverting differential clock input.
9	nPCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internally biased to $V_{DDO}/2$.
10	MR/nOE	Input	Pulldown	Active High Master Reset. Active Low Output Enable. When logic HIGH, the internal dividers are reset and the outputs are tri-stated (HiZ). When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
11, 15, 19, 23, 27	V_{DDO}	Power		Output supply pins.
12, 14, 16, 18, 20, 22, 24, 26	Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Clock outputs. LVCMOS / LVTTL interface levels. 14Ω typical output impedance.
28	QFB	Output		Feedback clock output. LVCMOS / LVTTL interface levels. 14Ω typical output impedance.
30	PLL_SEL	Input	Pullup	Selects VCO when HIGH. When LOW, selects PCLK, nPCLK. LVCMOS / LVTTL interface levels.
31	nBYPASS	Input	Pullup	Selects PLL when HIGH. When LOW, in Bypass mode.
32	VCO_SEL	Input	Pullup	Selects VCO ÷2 when HIGH. Selects VCO ÷1 when LOW. LVCMOS / LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDA}, V_{DDO} = 3.465V	5	7	12	pF
R_{OUT}	Output Impedance			14		Ω

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

Input	Outputs
MR/nOE	**QFB, Q0:Q7**
1	HiZ
0	Enabled

TABLE 3B. PROGRAMMABLE OUTPUT FREQUENCY FUNCTION TABLE

Inputs			Operation	Outputs
Bypass	**PLL_SEL**	**VCO_SEL**		**QFB, Q0:Q7**
0	X	X	Test Mode: PLL and divider bypass	CLK
1	0	0	Test Mode: PLL bypass	CLK/4
1	0	1	Test Mode: PLL bypass	CLK/8
1	1	0	PLL Mode	VCO/4
1	1	1	PLL Mode	VCO/8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DDA} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DDA}	Analog Supply Current				20	mA
I_{DDO}	Output Supply Current				75	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	VCO_SEL, nBYPASS, PLL_SEL, MR/nOE		2		V_{DD} + 0.3	V
		FB_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	VCO_SEL, nBYPASS, PLL_SEL, MR/nOE		-0.3		0.8	V
		FB_CLK		-0.3		1.3	V
I_{IN}	Input Current					±120	µA
V_{OH}	Output High Voltage; NOTE 1		I_{OH} = -20mA	V_{DD} - 0.6			V
V_{OL}	Output Low Voltage; NOTE 1		I_{OL} = 20mA			0.6	V

NOTE: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement section, "3.3V Output Load Test Circuit".

TABLE 4C. LVPECL DC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IN}	Input Current				±120	µA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLK, nPCLK is V_{DD} + 0.3V.

TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

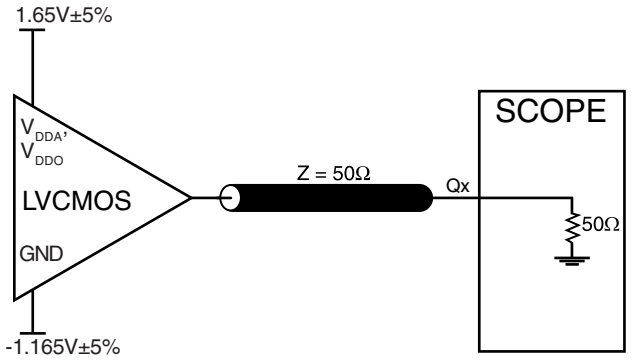
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency				110	MHz

TABLE 6. AC CHARACTERISTICS, $V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

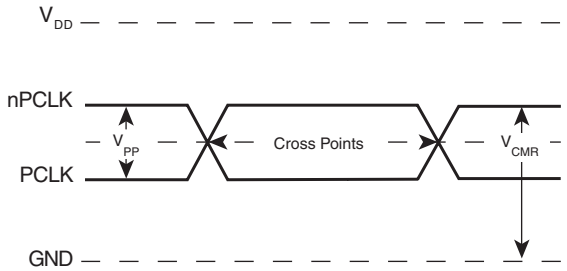
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	PLL Mode	VCO_SEL = 1	25		62.5	MHz
		PLL Mode	VCO_SEL = 0	50		110	MHz
		Bypass Mode				200	MHz
t_{PD}	Propagation Delay; NOTE 1	PCLK, nPCLK		2		6	ns
*t*sk(o)	Output Skew; NOTE 2, 4		Measured on rising edge at $V_{DD}/2$			75	ps
*t*jitter(cc)	Cycle-to-Cycle Jitter; NOTE 5					50	ps
t(Ø)	Static Phase Offset; NOTE 3, 5			-20	90	200	ps
t_R	Output Rise Time		0.8V to 2.0V	0.1		1.0	ns
t_F	Output Fall Time		0.8V to 2.0V	0.1		1.0	ns
odc	Output Duty Cycle			45	50	55	%
t_{LOCK}	PLL Lock Time					10	ms
t_{EN}	Output Enable Time; NOTE 4					6	ns
t_{DIS}	Output Disable Time; NOTE 4					7	ns

NOTE: Termination of 50Ω to $V_{DD}/2$.
NOTE 1: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

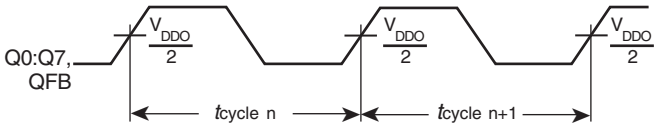
PARAMETER MEASUREMENT INFORMATION



3.3V OUTPUT LOAD AC TEST CIRCUIT



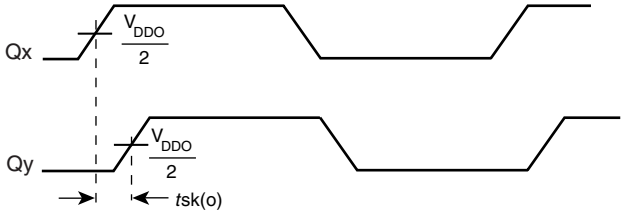
DIFFERENTIAL INPUT LEVEL



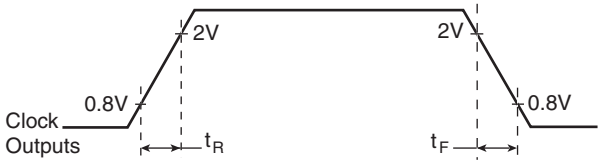
$tjit(cc) = tcycle\ n - tcycle\ n+1$

1000 Cycles

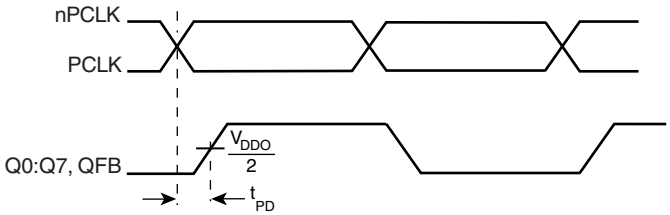
CYCLE-TO-CYCLE JITTER



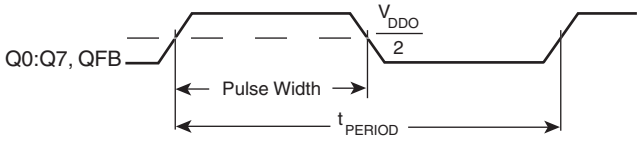
OUTPUT SKEW



OUTPUT RISE/FALL TIME

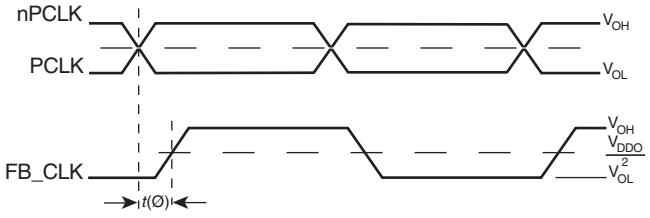


PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



$tjit(Ø) = \left| t(Ø) - t(Ø)_{mean} \right|$ = Phase Jitter

$t(Ø)_{mean}$ = Static Phase Offset

(where $t(Ø)$ is any random sample, and $t(Ø)_{mean}$ is the average of the sampled cycles measured on controlled edges)

PHASE JITTER & STATIC PHASE OFFSET

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

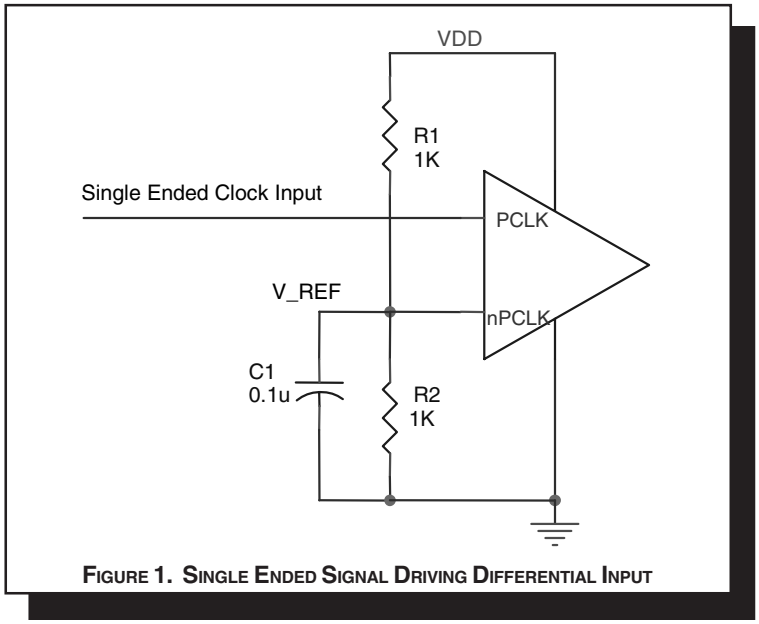


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS86953I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

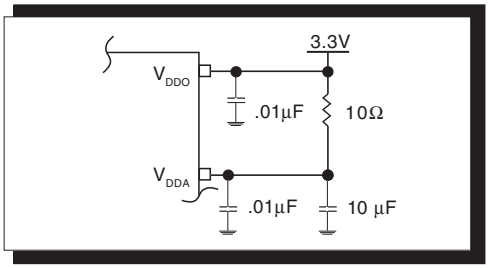


FIGURE 2. POWER SUPPLY FILTERING

LVPECL CLOCK INPUT INTERFACE

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

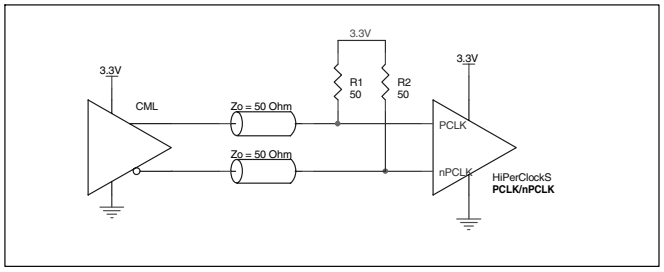


FIGURE 3A. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A CML DRIVER

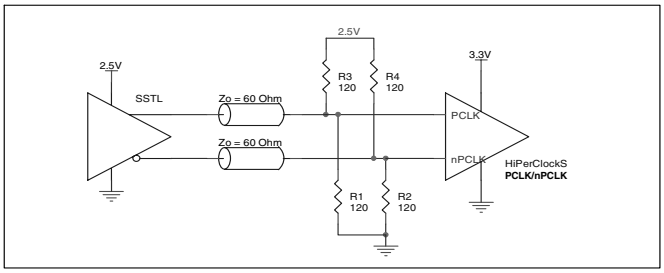


FIGURE 3B. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY AN SSTL DRIVER

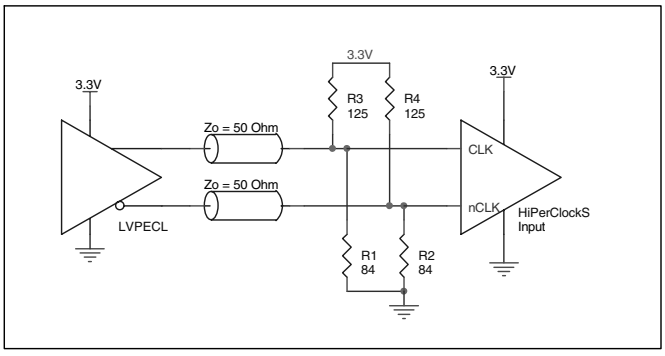


FIGURE 3C. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

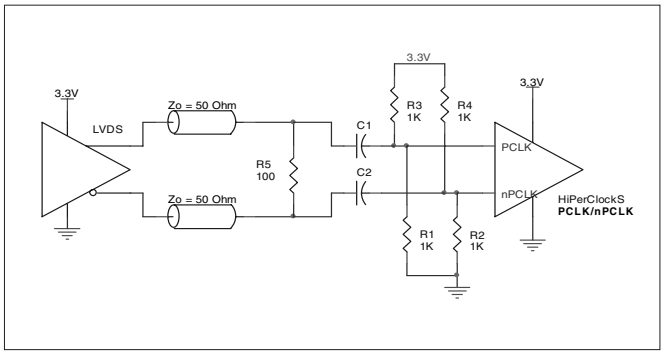


FIGURE 3D. HIPERCLOCKS PCLK/NPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

LAYOUT GUIDELINE

The schematic of the ICS86953I layout example is shown in *Figure 4A.* The ICS86953I recommended PCB board layout for this example is shown in *Figure 4B.* This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

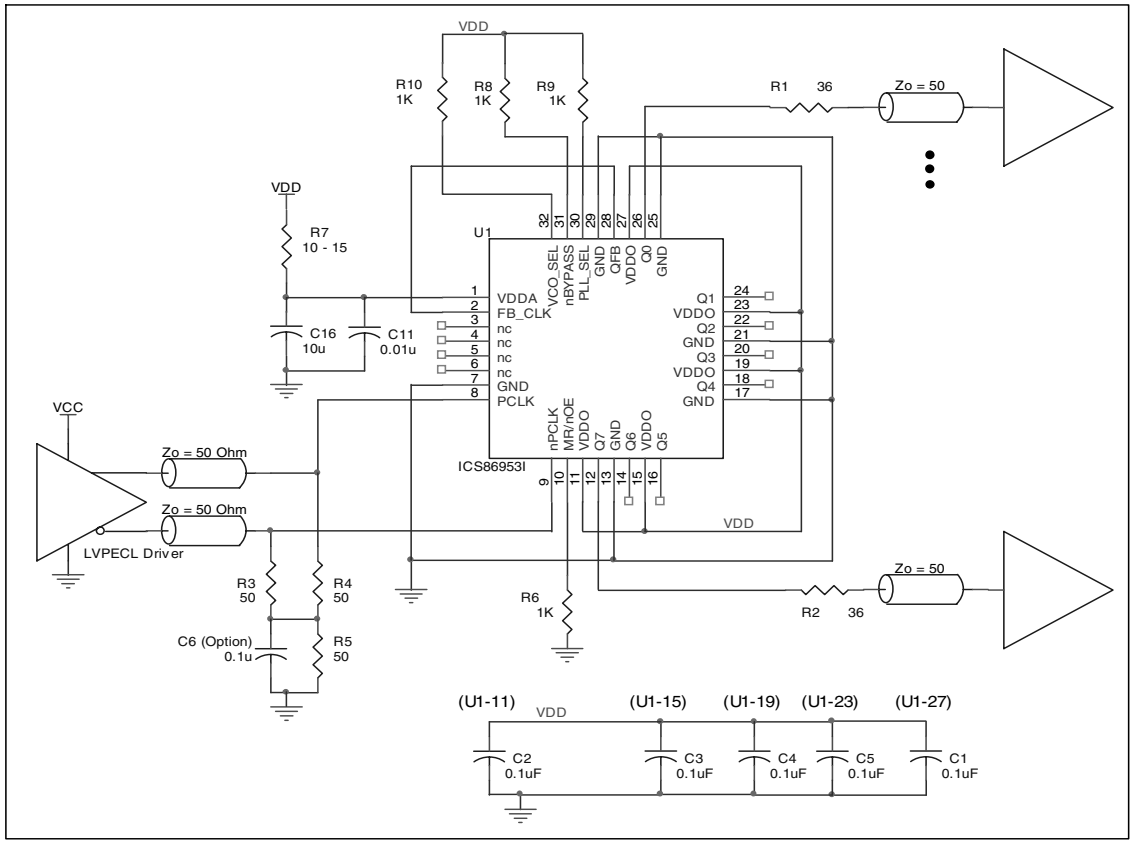


FIGURE 4A. ICS86953I LVCMOS ZERO DELAY BUFFER SCHEMATIC EXAMPLE

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

POWER AND GROUNDING

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the V_{DDA} pin as possible.

CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The series termination resistors should be located as close to the driver pins as possible.

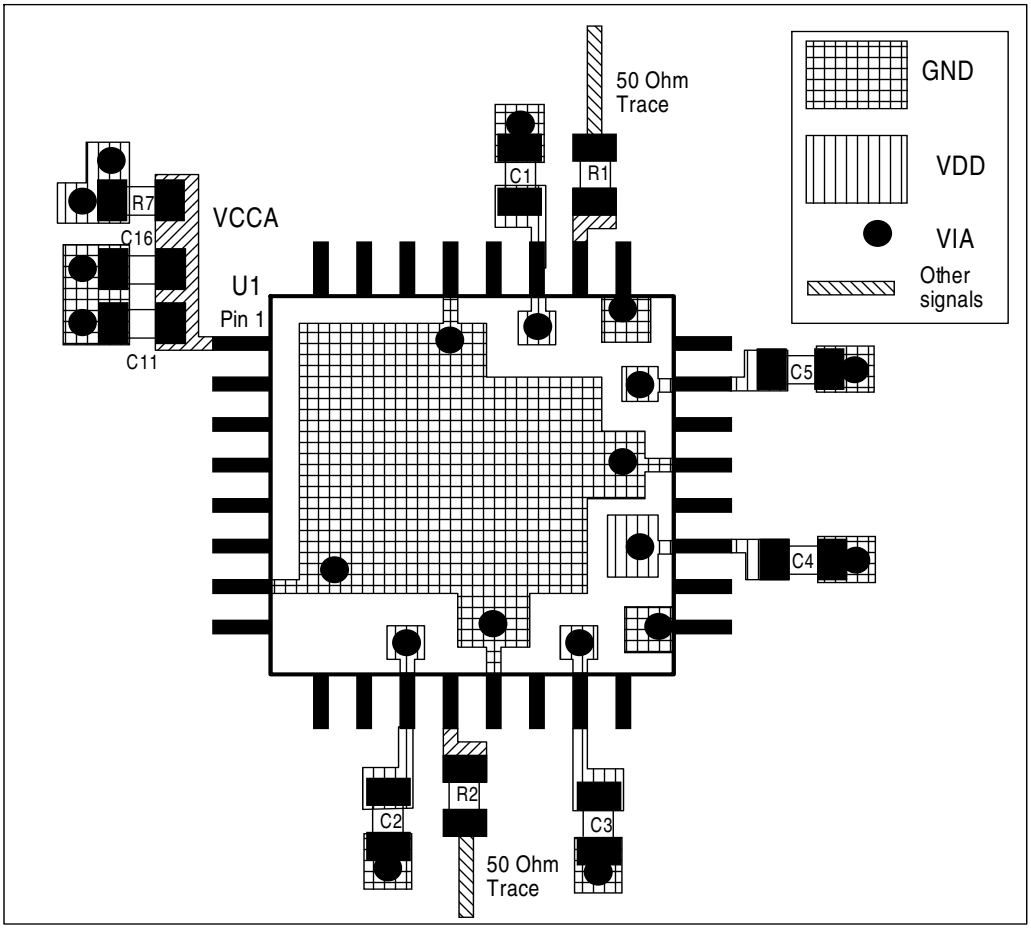


FIGURE 4B. PCB BOARD LAYOUT FOR ICS86953I

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 32 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS86953I is: 1758

PACKAGE OUTLINE - Y SUFFIX FOR 32 LEAD LQFP

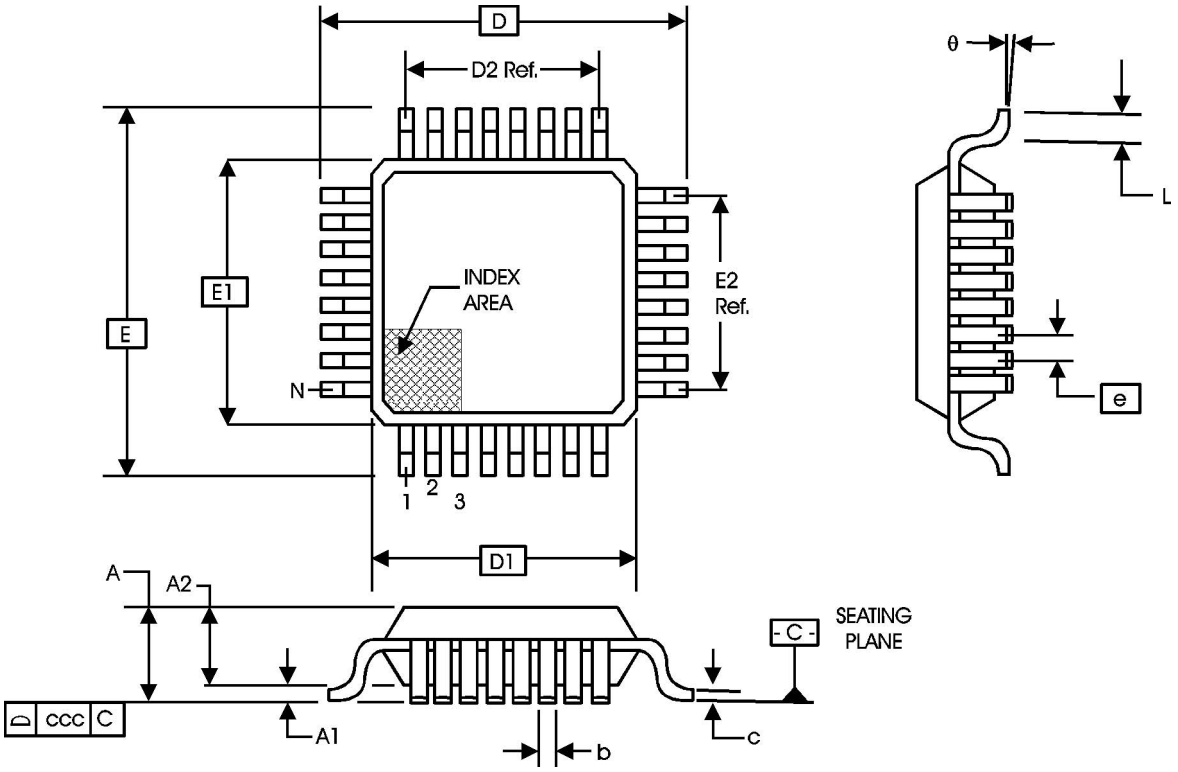


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N		32	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.60 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.60 Ref.	
e		0.80 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

Reference Document: JEDEC Publication 95, MS-026

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS86953BYI	ICS86953BYI	32 Lead LQFP	250 per tray	-40°C to 85°C
ICS86953BYIT	ICS86953BYI	32 Lead LQFP on Tape and Reel	1000	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T1	2	Pin Description Table - added *Pullup* and *Pulldown* to pin 9 and updated MR/nOE pin description.	10/8/03
	T2	2	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical. Added C_{PD} values of 5 min. and 7 typical.	
		6	Updated *Single Ended Signal Driving Differential Input diagram.*	
		7	Added *LVPECL Clock Input Interface section.*	
		8 & 9	Added *Layout Guideline section.*	
B	T2	2	Pin Characteristics Table - added R_{OUT} row.	4/23/04