256 MBit Synchronous DRAM

Target Information (Rev. 0.6)

- High Performance:

	-8	-10	Units
fCK	125	100	MHz
tCK3	8	10	ns
tAC3	6	7	ns
tAC2	6	8	ns

- Single Pulsed $\overline{\text{RAS}}$ Interface
- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C operating temperature
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{\text{CAS}}$ Latency: 2, 3, 4
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  1, 2, 4, 8 and full page for Sequential type
  1, 2, 4, 8 for Interleave Type
-

- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x4, x8)
- Data Mask for byte control (x16)
- Auto Refresh (CBR) and Self Refresh
- Suspend Mode and Power Down Mode
- 8192 refresh cycles / 128 ms
- Random Column Address every CLK (1-N Rule)
- Single 3.3V +/- 0.3V Power Supply
- LVTTL and SSTL_3 (Class II) Interface versions
- Plastic Packages:
  P-TSOPII-54 400mil width (x4, x8, x16)

The HYB39S25640x/80x/16xT are four bank Synchronous DRAM's organized as 4 banks x 16MBit x4, 4 banks x 8MBit x8 and 4 banks x 4Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates for CAS-latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with SIEMENS' advanced 256MBit DRAM process technology.

The device is designed to comply with all JEDEC standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.
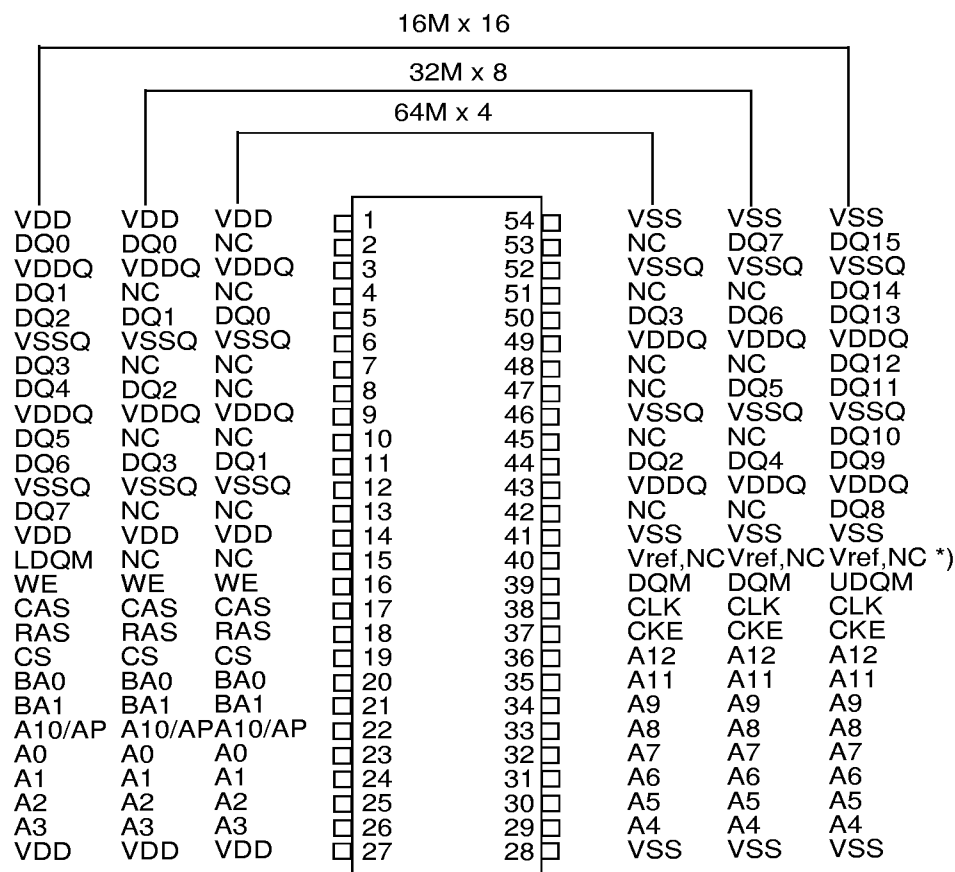
Auto Refresh (CBR) and Self Refresh operation are supported. These devices operates with a single 3.3V +/- 0.3V power supply and are available in TSOPII packages.

Ordering Information

Type	Ordering Code	Package	Description
LVTTL-version:			
HYB 39S256400T-8		P-TSOP-54-2 (400mil)	125MHz 4B x 16M x 4 SDRAM
HYB 39S256400T-10		P-TSOP-54-2 (400mil)	100MHz 4B x 16M x 4 SDRAM
HYB 39S256800T-8		P-TSOP-54-2 (400mil)	125MHz 4B x 8M x 8 SDRAM
HYB 39S256800T-10		P-TSOP-54-2 (400mil)	100MHz 4B x 8M x 8 SDRAM
HYB 39S256160T-8		P-TSOP-54-2 (400mil)	125MHz 4B x 4M x 16 SDRAM
HYB 39S256160T-10		P-TSOP-54-2 (400mil)	100MHz 4B x 4M x 16 SDRAM
SSTL-version:			
HYB 39S256402T-8		P-TSOP-54-2 (400mil)	125 MHz 4B x 16M x 4 SDRAM
HYB 39S256402T-10		P-TSOP-54-2 (400mil)	100 MHz 4B x 16M x 4 SDRAM
HYB 39S256802T-8		P-TSOP-54-2 (400mil)	125 MHz 4B x 8M x 8 SDRAM
HYB 39S256802T-10		P-TSOP-54-2 (400mil)	100 MHz 4B x 8M x 8 SDRAM
HYB 39S256162T-8		P-TSOP-54-2 (400mil)	125 MHz 4B x 4M x 16 SDRAM
HYB 39S256162T-10		P-TSOP-54-2 (400mil)	100 MHz 4B x 4M x 16 SDRAM

Pin Description and Pinouts:

CLK	Clock Input	DQ	Data Input /Output
CKE	Clock Enable	DQM, LDQM, UDQM	Data Mask
$\overline{CS}$	Chip Select	Vdd	Power (+3.3V)
$\overline{RAS}$	Row Address Strobe	Vss	Ground
$\overline{CAS}$	Column Address Strobe	Vddq	Power for DQ's (+ 3.3V)
$\overline{WE}$	Write Enable	Vssq	Ground for DQ's
A0-A12	Address Inputs	NC	not connected
BA0, BA1	Bank Select	Vref	Reference Voltage (SSTL version only)

Target Information

16M x 16

32M x 8

64M x 4

16M x 16	32M x 8	64M x 4	Pin	Pin	64M x 4	32M x 8	16M x 16
VDD	VDD	VDD	1	54	VSS	VSS	VSS
DQ0	DQ0	NC	2	53	NC	DQ7	DQ15
VDDQ	VDDQ	VDDQ	3	52	VSSQ	VSSQ	VSSQ
DQ1	NC	NC	4	51	NC	NC	DQ14
DQ2	DQ1	DQ0	5	50	DQ3	DQ6	DQ13
VSSQ	VSSQ	VSSQ	6	49	VDDQ	VDDQ	VDDQ
DQ3	NC	NC	7	48	NC	NC	DQ12
DQ4	DQ2	NC	8	47	NC	DQ5	DQ11
VDDQ	VDDQ	VDDQ	9	46	VSSQ	VSSQ	VSSQ
DQ5	NC	NC	10	45	NC	NC	DQ10
DQ6	DQ3	DQ1	11	44	DQ2	DQ4	DQ9
VSSQ	VSSQ	VSSQ	12	43	VDDQ	VDDQ	VDDQ
DQ7	NC	NC	13	42	NC	NC	DQ8
VDD	VDD	VDD	14	41	VSS	VSS	VSS
LDQM	NC	NC	15	40	Vref,NC	Vref,NC	Vref,NC *)
WE	WE	WE	16	39	DQM	DQM	UDQM
CAS	CAS	CAS	17	38	CLK	CLK	CLK
RAS	RAS	RAS	18	37	CKE	CKE	CKE
CS	CS	CS	19	36	A12	A12	A12
BA0	BA0	BA0	20	35	A11	A11	A11
BA1	BA1	BA1	21	34	A9	A9	A9
A10/AP	A10/AP	A10/AP	22	33	A8	A8	A8
A0	A0	A0	23	32	A7	A7	A7
A1	A1	A1	24	31	A6	A6	A6
A2	A2	A2	25	30	A5	A5	A5
A3	A3	A3	26	29	A4	A4	A4
VDD	VDD	VDD	27	28	VSS	VSS	VSS

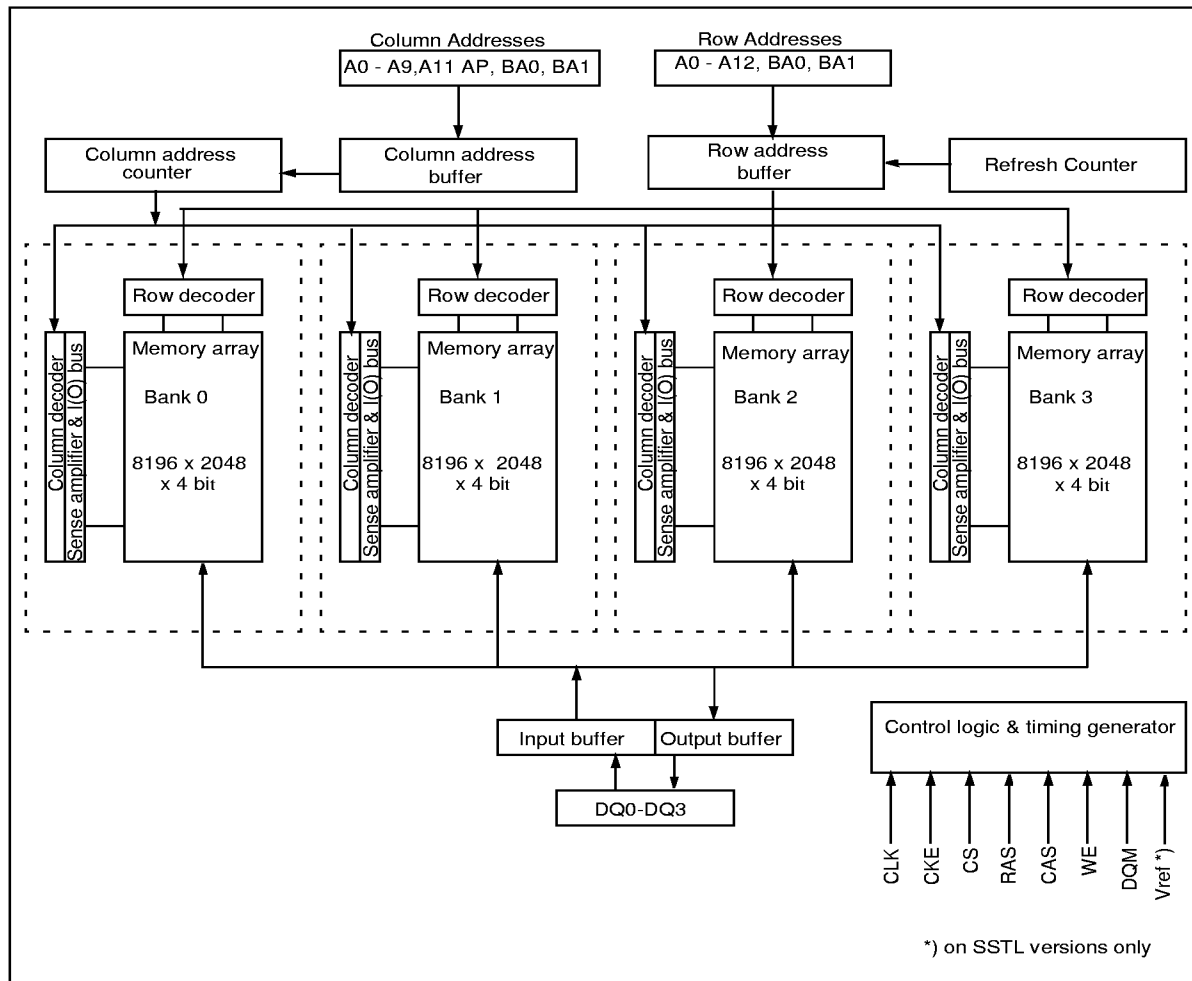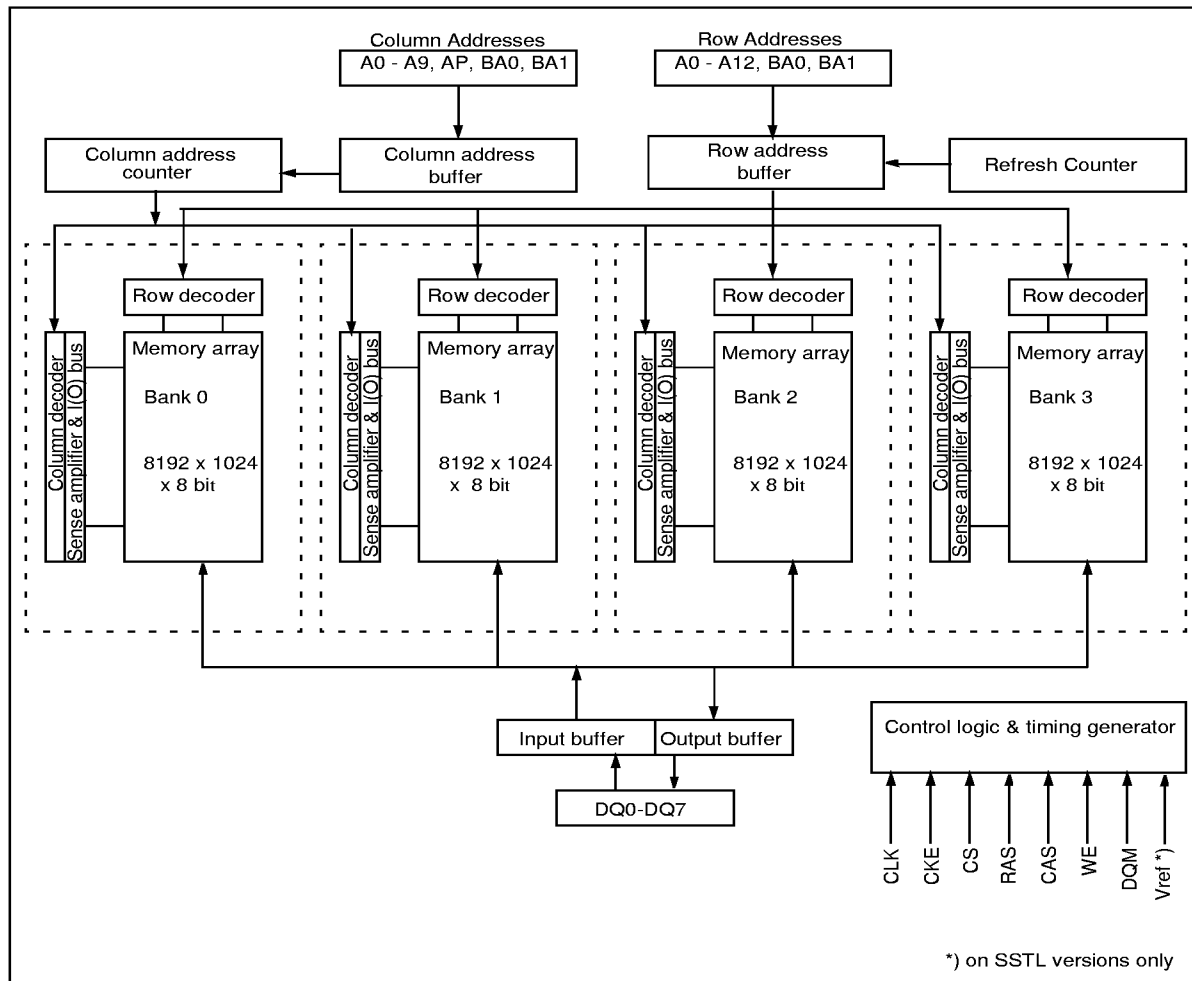**TSOPII-54 (400 mil x 875 mil, 0.8 mm pitch)**

*) This pin is NC for LV-TTL and Vref for SSTL versions

Pinout for x4, x8 & x16 organised 256M-DRAMs

Target information

Block Diagram for 64M x 4 SDRAM (13 / 11 / 2 addressing)

Block Diagram for 32M x 8 SDRAM (13 / 10 / 2 addressing)

Block Diagram for 16M x16 SDRAM (13 / 9 / 2 addressing)

Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Pulse	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the command to be executed by the SDRAM.
A0 - A12	Input	Level	—	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-An defines the column address (CA0-CAn) when sampled at the rising clock edge. CAn depends from the SDRAM organisation: 64M x 4 SDRAM CAn = CA9,CA11 (Page Length = 2048 bits) 32M x 8 SDRAM CAn = CA9 (Page Length = 1024 bits) 16M x 16 SDRAM CAn = CA8 (Page Length = 512 bits) In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 (=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A10 is low, then BA0 and BA1 are used to define which bank to precharge.
BA0,BA1	Input	Level	—	Bank Select (BS) Inputs. Selects which bank is to be active.
DQx	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQM LDQM UDQM	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. One DQM input it present in x4 and x8 SDRAMs, LDQM and UDQM controls the lower and upper bytes in x16 SDRAMs.
VDD,VSS	Supply			Power and ground for the input buffers and the core logic.
VDDQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.
Vref	Input	Level	—	Reference voltage for SDRAM versions supporting SSTL interface

Target information
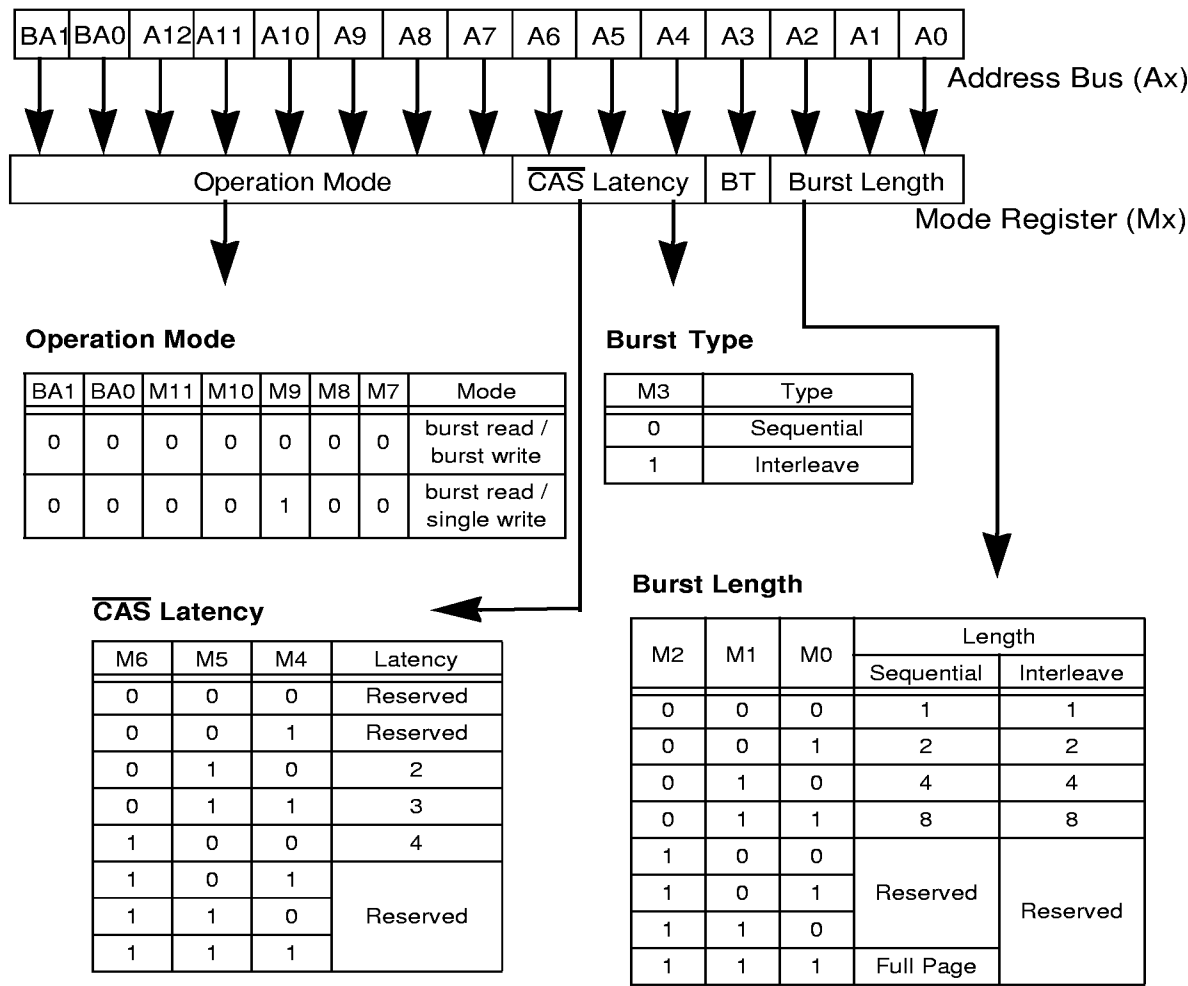
Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the truth table for the operation commands.

Operation	Device State	CKE n-1	CKE n	DQM	BS0 BS1	AP= A10	Addr .	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Active	Idle[3]	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active[3]	H	X	X	V	L	V	L	H	L	L
Write with Autoprecharge	Active[3]	H	X	X	V	H	V	L	H	L	L
Read	Active[3]	H	X	X	V	L	V	L	H	L	H
Read with Autoprecharge	Active[3]	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active[4]	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H / L	X / H	X / H	X / X
Clock Suspend Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Entry (Precharge or active standby)	Idle Active[5]	H	L	X	X	X	X	H / L	X / H	X / H	X / X
Clock Suspend Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Exit	Any (Power Down)	L	H	X	X	X	X	H / L	X / H	X / H	X / L
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Note:

1. V = Valid, x = Don't Care, L = Low Level, H = High Level

2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.

3. This is the state of the banks designated by BS0, BS1 signals.

4. Device state is Full Page Burst operation

5. Power Down Mode can not entry in the burst cycle. When this command assert in the burst mode cycle device is clock suspend mode.

Address Input for Mode Set (Mode Register Operation)

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Address Bus (Ax)

Operation Mode	$\overline{\text{CAS}}$ Latency	BT	Burst Length

Mode Register (Mx)

Operation Mode

BA1	BA0	M11	M10	M9	M8	M7	Mode
0	0	0	0	0	0	0	burst read / burst write
0	0	0	0	1	0	0	burst read / single write

Burst Type

M3	Type
0	Sequential
1	Interleave

$\overline{\text{CAS}}$ Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

M2	M1	M0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Target information

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner.During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed VDD+0.3V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200 µs is required followed by a precharge of both banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight Auto Refresh cycles (CBR) are also required.These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a CAS **Latency** Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in precharged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

Read and Write Operation

When $\overline{RAS}$ is low and both $\overline{CAS}$ and $\overline{WE}$ are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A CAS cycle is triggered by setting $\overline{RAS}$ high and $\overline{CAS}$ low at a clock timing after a necessary delay, t_{RCD}, from the RAS timing. $\overline{WE}$ is used to define either a read ($\overline{WE}$ = H) or a write ($\overline{WE}$ = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 143 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8 and full page. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is '2', then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Full page burst operation is only possible using the sequential burst type and page length is a function of the I/O organisation and column addressing. Full page burst operation do not self terminate once the burst length has been reached. In other words, unlike burst length of 2, 3 or 8, full page burst continues until it is terminated using another command.

Target information

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum tRAS or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycle is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and precharge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

Burst Length and Sequence:

Burst Length	Starting Address (A2 A1 A0)	Sequential Burst Addressing (decimal)	Interleave Burst Addressing (decimal)
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	001	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	010	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	011	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	100	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	101	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	110	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	111	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0
Full Page	nnn	Cn, Cn+1, Cn+2,.....	not supported

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$-before-$\overline{RAS}$ refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum tRC time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one tRC delay is required prior to any access command.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to „high" at a clock timing, data outputs are disabled and become high impedance after two clock delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is low, it freezes the internal clock and extends data read and write operations. One clock delay is required for mode entry and exit (Clock Suspend Latency t_{CSL}).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (trp) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (tref) of the device. Exit from this mode is performed by taking CKE „high". One clock delay is required for mode entry and exit.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock before the last data out for $\overline{CAS}$ latencies 2, two clocks for $\overline{CAS}$ latencies 3 and three clocks for CAS latencies 4. If CAS10 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to t_{WR} (Write recovery time) after the last data in.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for CAS latency = 2, two clocks before the last data out for CAS latency = 3 and three clocks before the last data out for CAS latency= 4. Writes require a time delay twr from the last data out to apply the precharge command.

Bank Selection by Address Bits

A10	BA0	BA1	
0	0	0	Bank 0

A10	BA0	BA1	
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	x	x	all Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Precharge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

Absolute Maximum Ratings

Operating temperature range .... 0 to + 70 °C

Storage temperature range .... − 55 to + 150 °C

Input/output voltage .... − 0.3 to Vcc+0.3 V

Power supply voltage VDD / VDDQ .... − 0.3 to + 4.6 V

Power Dissipation .... 1 W

Data out current (short circuit) .... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operation and Characteristics for LV-TTL versions:

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.3	V	1, 2
Input low voltage	V_{IL}	− 0.3	0.8	V	1, 2
Output high voltage (I_{OUT} = − 2.0 mA)	V_{OH}	2.4	–	V	3
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V	3
Input leakage current, any input (0 V < V_{IN} < Vddq, all other inputs = 0 V)	$I_{I(L)}$	− 5	5	µA	
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	− 5	5	µA	

Notes:
1. All voltages are referenced to VSS.
2. Vih may overshoot to Vcc + 2.0 V for pulse width of < 4ns with 3.3V. Vil may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	max. Values	Unit
Input capacitance (CLK)	C_{I1}	6	pF
Input capacitance (A0-A12, BA0,BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM)	C_{I2}	4	pF
Input / Output capacitance (DQ)	C_{IO}	5	pF
Vref	C_{REF}	8	pF

Recommended Operation and Characteristics for SSTL-versions:
T_A = 0 to 70 °C; V_{SS} = 0 V;

Parameter	Symbol	Limit Values			Unit	Notes
		min.	**typ.**	**max.**		
Power Supply Voltage	Vcc	3.0	3.3	3.6	V	
Power Supply Voltage for I/O Buffer	Vccq	3.0	3.3	3.6	V	
Input Reference Voltage	Vref	1.3	1.5	1.7	V	5
Termination Voltage	Vtt	Vref-0.05	Vref	Vref+0.05		6
Input high voltage	V_{IH}	Vref + 0.2	–	Vccq+0.3	V	3
Input low voltage	V_{IL}	– 0.3	–	Vref + 0.2	V	4
Output high voltage (I_{OUT} = – 16 mA)	V_{OH}	Vtt + 0.8	–	–	V	
Output low voltage (I_{OUT} = 16 mA)	V_{OL}	–	–	Vtt-0.8	V	
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 5		5	μA	
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 5		5	μA	

Notes:
3. Vih(max) = Vccq + 1.2 V for pulse width < 5 ns
4. Vil(max) = Vssq -1.2 V for pulse width < 5 ns
5. The value of Vref may be selected by the user to provide optimum noise margin in the system. Vref has to be in the range between 0.43 * Vccq and 0.47 * Vccq and is expected to track variations in Vccq.
6. Vtt of transmitting device must track Vref of receiving device

Operating Currents (T_A = 0 to 70°C, VCC = 3.3V $\pm$ 0.3V

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	-8	-10		Note
			max.			
OPERATING CURRENT	1 bank operation	ICC1			mA	7
trc=trcmin., tck=tckmin. Active-precharge command cycling, without burst operation	4 bank interleave operation	ICC1B			mA	7
PRECHARGE STANDBY CURRENT in Power Down Mode	tck = min.	ICC2P	1	1	mA	7
$\overline{CS}$ =VIH (min.), CKE<=Vil(max)	tck = Infinity	ICC2PS	1	1	mA	
PRECHARGE STANDBY CURRENT in Non-Power Down Mode	tck = min.	ICC2			mA	7
$\overline{CS}$ = VIH (min.), CKE>=Vih(min)	tck = Infinity	ICC2S			mA	
NO OPERATING CURRENT	CKE>=VIH(min.)	ICC3			mA	
tck = min., $\overline{CS}$ = VIH(min), active state (max. 4 banks)	CKE<=VIL(max.) (Power down mode)	ICC3P	2	2	mA	
BURST OPERATING CURRENT tck = min., Read/Write command cycling		ICC4			mA	7,8
AUTO REFRESH CURRENT tck = min., Auto Refresh command cycling		ICC5			mA	7
SELF REFRESH CURRENT Self Refresh Mode, CKE=0.2V		ICC6	2.5	2.5	mA	

Notes:

7. These parameters depend on the cycle rate and these values are measured by the cycle rate under the ....minimum value of tck and trc. Input signals are changed one time during tck.

8. These parameter depend on output loading. Specified values are obtained with output open.

AC Characteristics 1)2)3)
T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 3.3 V $\pm$ 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	
		-8		-10			
		min	max	min	max		

Clock and Clock Enable

Parameter	Symbol	min	max	min	max	Unit	
Clock Cycle Time							
$\overline{CAS}$ Latency = 4	t_{CK}	8	–	10	–	ns	
$\overline{CAS}$ Latency = 3		8	–	10	–	ns	
$\overline{CAS}$ Latency = 2		8	–	10	–	ns	
Clock Frequency							
$\overline{CAS}$ Latency = 4	t_{CK}	–	125	–	100	MHz	
$\overline{CAS}$ Latency = 3		–	125	–	100	MHz	
$\overline{CAS}$ Latency = 2		–	125	–	83	MHz	
Access Time from Clock							2, 4
$\overline{CAS}$ Latency = 4	t_{AC}	–	5	–	6	ns	
$\overline{CAS}$ Latency = 3		–	5.5	–	6	ns	
$\overline{CAS}$ Latency = 2		–	6	–	7	ns	
Clock High Pulse Width	t_{CH}	3	–	3	–	ns	
Clock Low Pulse Width	t_{CL}	3	–	3	–	ns	
Transition time	t_T	0.5	10	0.5	10	ns	

Setup and Hold Times

Parameter	Symbol	min	max	min	max	Unit	
Input Setup Time	t_{IS}	1.5	–	2	–	ns	5
Input Hold Time	t_{IH}	0.5	–	1	–	ns	5
CKE Setup Time	t_{CKS}	1.5	–	2	–	ns	5
CKE Hold Time	t_{CKH}	0.5	–	1	–	ns	5
Mode Register Set-up time	t_{RSC}	16	–	20	–	ns	
Power Down Mode Entry Time	t_{SB}	0	8	0	10	ns	

Common Parameters

Parameter	Symbol	min	max	min	max	Unit	
Row to Column Delay Time	t_{RCD}	16	–	24	–	ns	6
Row Active Time	t_{RAS}	45	100k	60	100k	ns	6
Row Cycle Time	t_{RC}	70	–	90	–	ns	6
Row Precharge Time	t_{RP}	16	–	20	–	ns	6

Target information

Parameter	Symbol	Limit Values				Unit	
		-8		-10			
		min	max	min	max		
Activate(a) to Activate(b) Command period	t_{RRD}	16	–	20	–	ns	6
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	t_{CCD}	1	–	1	–	CLK	

Refresh Cycle

Parameter	Symbol	min	max	min	max	Unit	
Refresh Period (8192 cycles)	t_{REF}	–	128	–	128	ms	
Self Refresh Exit Time	t_{SREX}	10	–	10	–		

Read Cycle

Parameter	Symbol	min	max	min	max	Unit	
Data Out Hold Time	t_{OH}	3	–	3	–	ns	2
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	8	3	10	ns	8
DQM Data Out Disable Latency	t_{DQZ}	2	–	2	–	CLK	

Write Cycle

Parameter	Symbol	min	max	min	max	Unit	
Write Recovery Time	t_{WR}	8	–	10	–	ns	
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	

Target Information

Notes for AC Parameters:

1. For proper power-up see the operation section of this data sheet.
2. AC timing tests for LV-TTL versions have V_{il} = 0.4 V and V_{ih} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is meas ured between V_{ih} and V_{il}. All AC measurements assume t_T=1ns with the AC output load circuit shown in fig.1.Specified tac and toh parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.
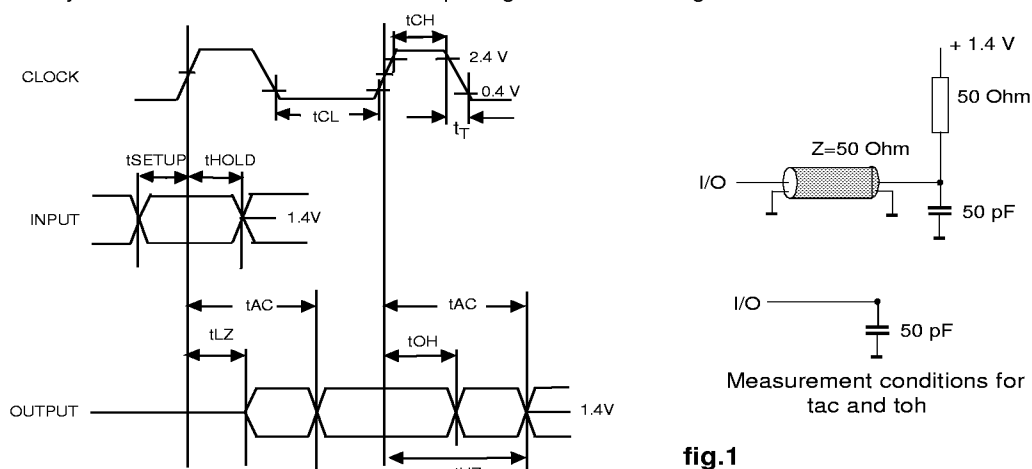
fig.1

3. AC timing test conditions for SSTL_3 versions:
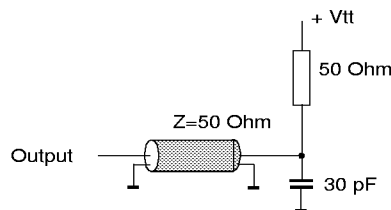
fig.1

Termination Voltage	0.45 x Vccq
Reverence Level of Output Signals (Vref)	0.45 x Vccq
Output Load	see fig. 1
Transition Time (Rise and Fall) of Input Signals	1 ns
Reference Level of Input Signals (Vref)	0.45 x Vccq

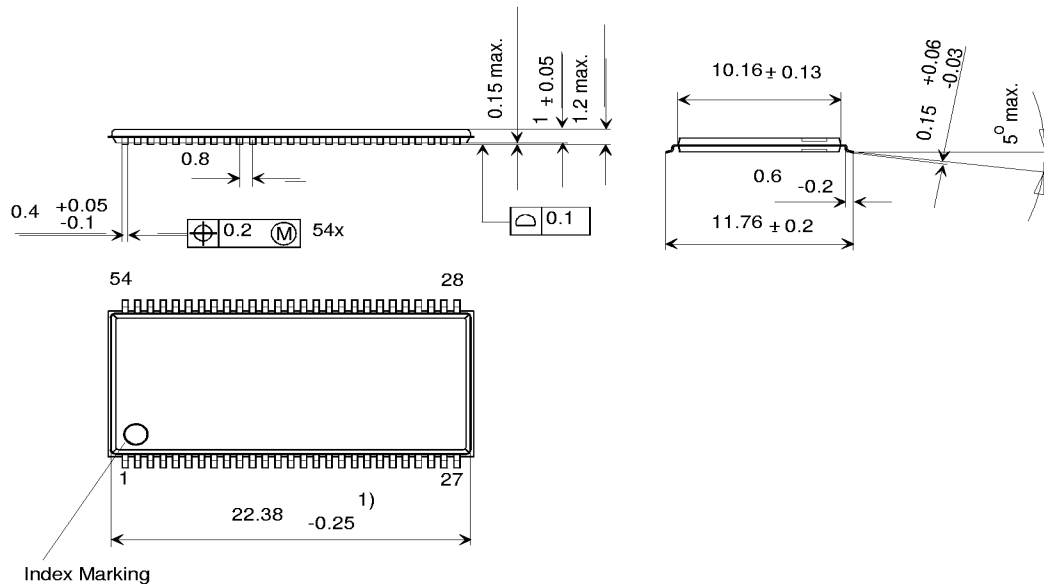4. If clock rising time is longer than 1 ns, a time (t_T/2 - 0.5) ns has to be added to this parameter.
5. If tT is longer than 1 ns, a time (t_T -1) ns has to be added to this parameter.
6. These parameter account for the number of clock cycle and depend on the operating frequency of the clock, as follows:
   the number of clock cycle = specified value of timing period (counted in fractions as a whole number)
   Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.

Package Outlines

Plastic Package P-TSOPII-54 (400mil, 0.8mm lead pitch)
Thin small outline package, SMD

0.15 max.

1 ± 0.05

1.2 max.

10.16 ± 0.13

0.15 $^{+0.06}_{-0.03}$

5° max.

0.8

0.6 $_{-0.2}$

11.76 ± 0.2

0.4 $^{+0.05}_{-0.1}$

$\oplus$ 0.2 Ⓜ 54x

$\square$ 0.1

54   28

1   27

1)
22.38 $_{-0.25}$

Index Marking

1) Does not include plastic or metal protrusion of 0.15 max. per side

TSOPII-54 (400 mil)
TSOP54-2.DRW

Target information