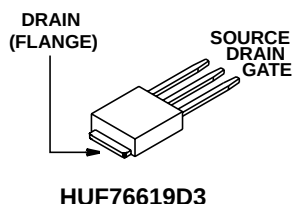


18A, 100V, 0.087 Ohm, N-Channel, Logic Level UltraFET Power MOSFET

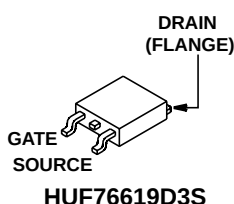


Packaging

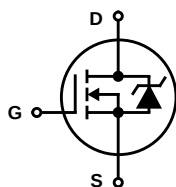
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.085\Omega$, $V_{GS} = 10V$
 - $r_{DS(ON)} = 0.087\Omega$, $V_{GS} = 5V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER® Electrical Models
 - Spice and SABER® Thermal Impedance Models
 - www.semi.Intersil.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76619D3	TO-251AA	76619D
HUF76619D3S	TO-252AA	76619D

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-252AA variant in tape and reel, e.g., HUF76619D3ST.

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	HUF76619D3, HUF76619D3S	UNITS
Drain to Source Voltage (Note 1)	100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	100	V
Gate to Source Voltage	± 16	V
Drain Current		
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 5V$)	18	A
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10V$) (Figure 2)	18	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 5V$)	12	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 4.5V$) (Figure 2)	12	A
Pulsed Drain Current	Figure 4	
Pulsed Avalanche Rating	Figures 6, 17, 18	
Power Dissipation	75	W
Derate Above 25°C	0.5	W/ $^\circ\text{C}$
Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief TB334.	260	$^\circ\text{C}$

NOTES:

1. $T_J = 25^\circ\text{C}$ to 150°C .

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

HUF76619D3, HUF76619D3S

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	100	-	-	V	
		I _D = 250μA, V _{GS} = 0V , T _C = -40 ⁰ C (Figure 12)	95	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 95V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 90V, V _{GS} = 0V, T _C = 150 ⁰ C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 18A, V _{GS} = 10V (Figures 9, 10)	-	0.065	0.085	Ω	
		I _D = 12A, V _{GS} = 5V (Figure 9)	-	0.072	0.087	Ω	
		I _D = 12A, V _{GS} = 4.5V (Figure 9	-	0.074	0.089	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	TO-251AA, TO-252AA	-	-	2.0	⁰ C/W	
Thermal Resistance Junction to Ambient	R _{θJA}		-	-	100	⁰ C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)							
Turn-On Time	t _{ON}	V _{DD} = 50V, I _D = 12A V _{GS} = 4.5V, R _{GS} = 12Ω (Figures 15, 21, 22)	-	-	137	ns	
Turn-On Delay Time	t _{d(ON)}		-	10	-	ns	
Rise Time	t _r		-	82	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	32	-	ns	
Fall Time	t _f		-	42	-	ns	
Turn-Off Time	t _{OFF}		-	-	111	ns	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 50V, I _D = 18A V _{GS} = 10V, R _{GS} = 12Ω (Figures 16, 21, 22)	-	-	53	ns	
Turn-On Delay Time	t _{d(ON)}		-	6	-	ns	
Rise Time	t _r		-	30	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	50	-	ns	
Fall Time	t _f		-	52	-	ns	
Turn-Off Time	t _{OFF}		-	-	153	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 30V, I _D = 12A, I _{g(REF)} = 1.0mA (Figures 14, 19, 20)	-	24	29	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	13	16	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	0.74	0.89	nC
Gate to Source Gate Charge	Q _{gs}			-	2.2	-	nC
Reverse Transfer Capacitance	Q _{gd}			-	6.7	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 13)	-	767	-	pF	
Output Capacitance	C _{OSS}		-	138	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	20	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 12\text{A}$	-	-	1.25	V
		$I_{SD} = 6\text{A}$	-	-	1.0	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 12\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	101	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 12\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	333	nC

Typical Performance Curves

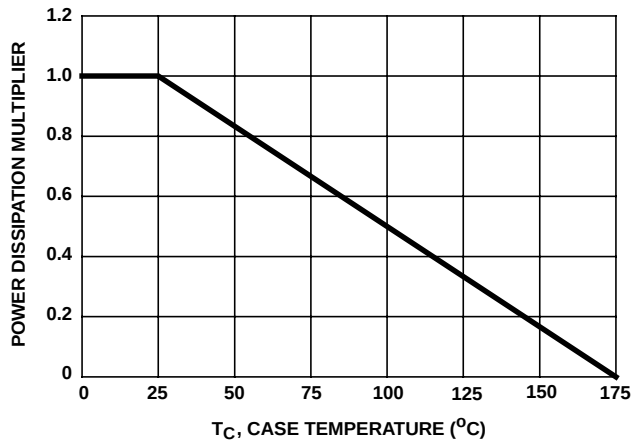


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

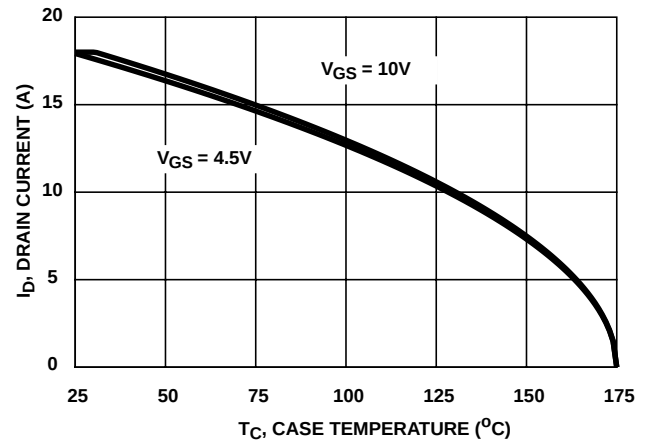


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

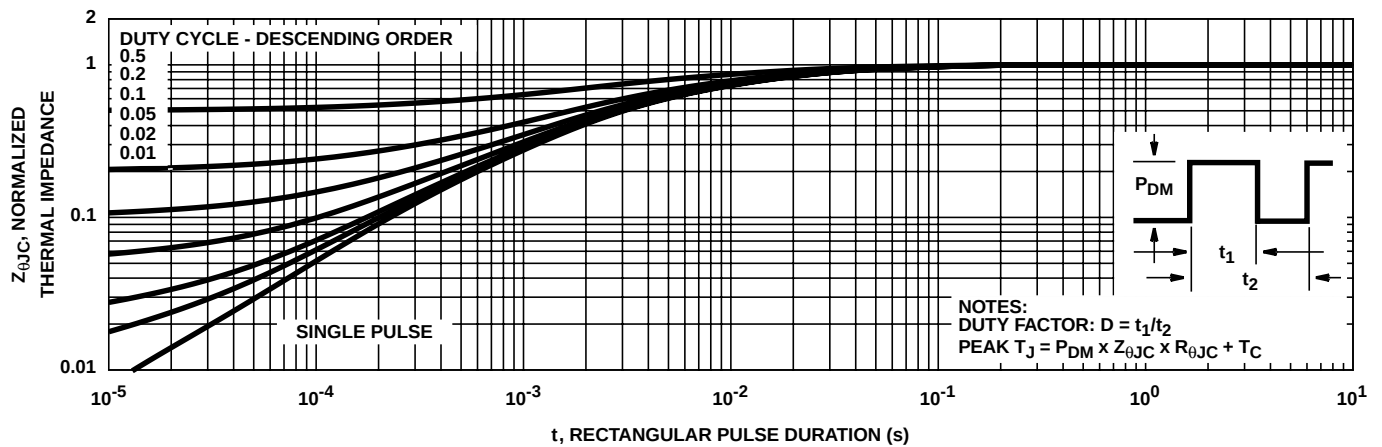


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

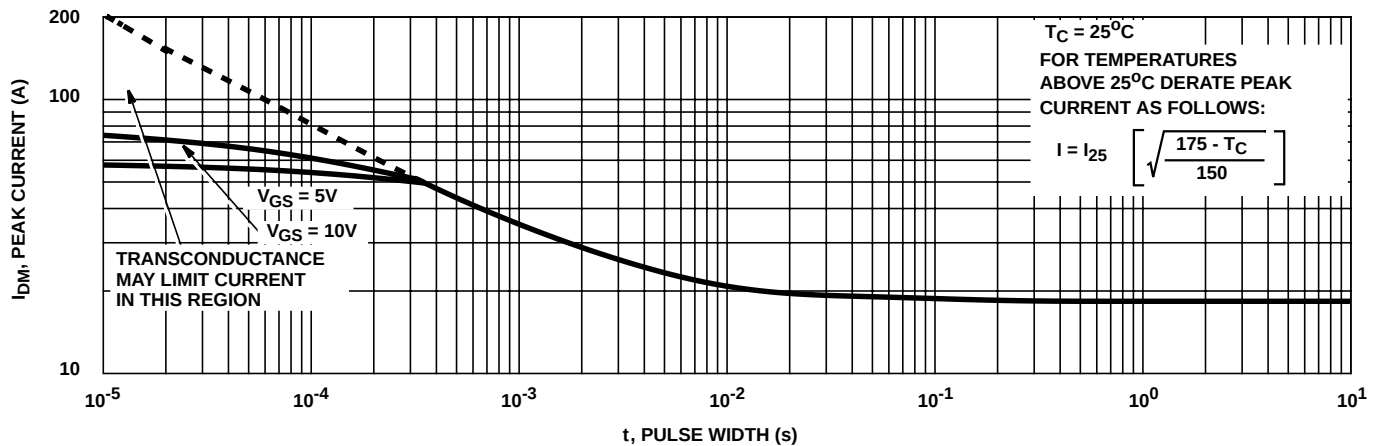


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

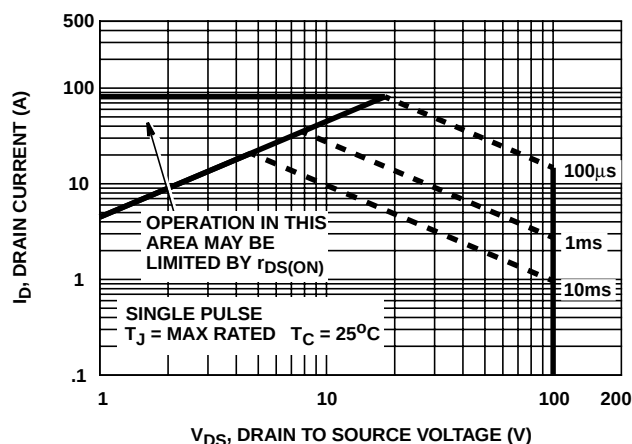
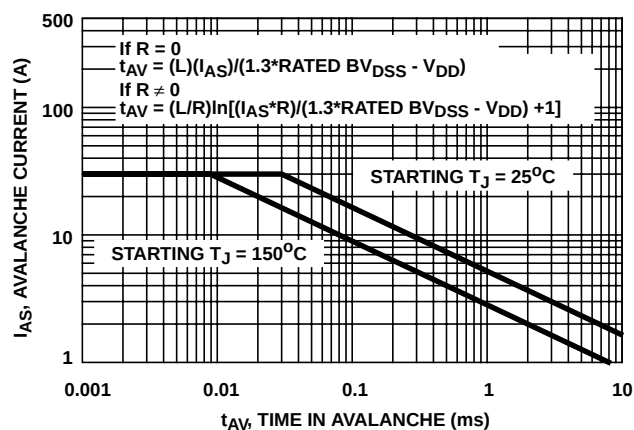


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

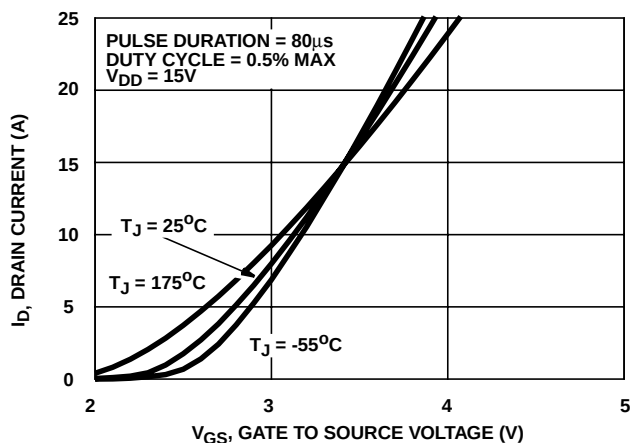


FIGURE 7. TRANSFER CHARACTERISTICS

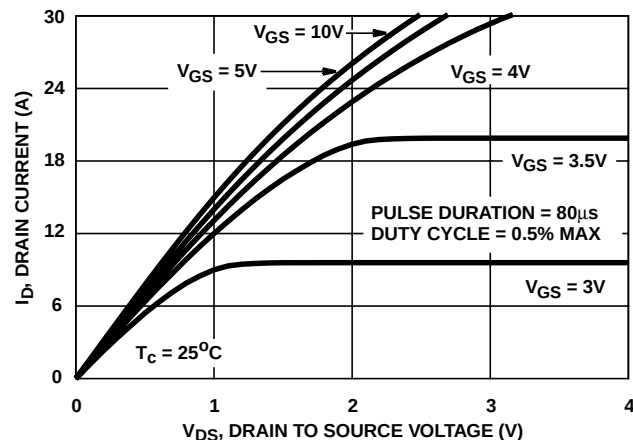


FIGURE 8. SATURATION CHARACTERISTICS

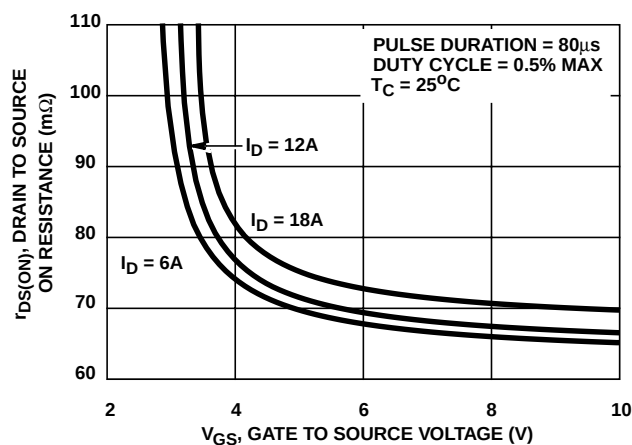


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs. GATE VOLTAGE AND DRAIN CURRENT

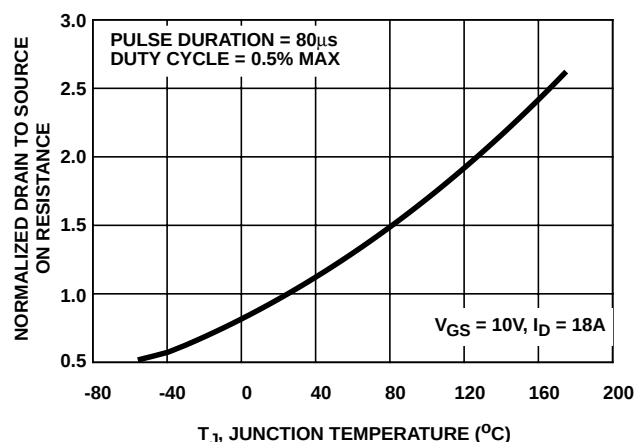


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs. JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

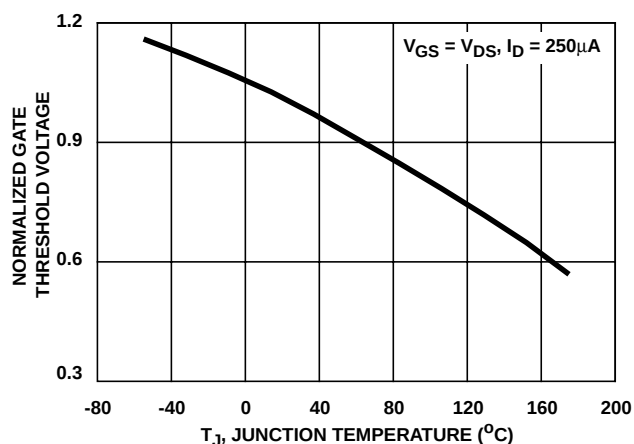


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

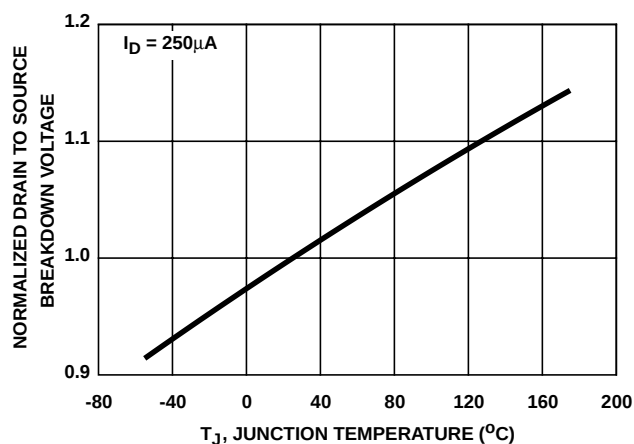


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

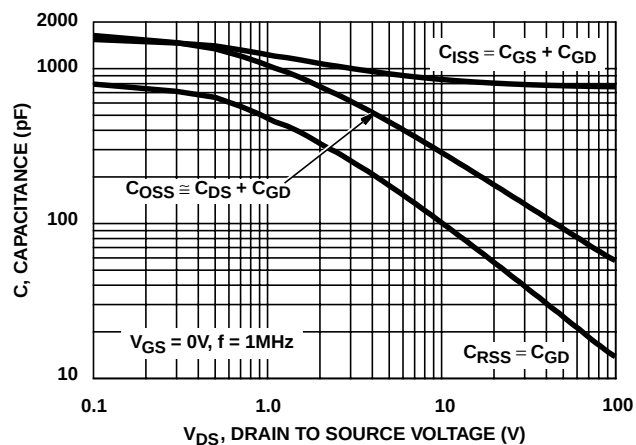
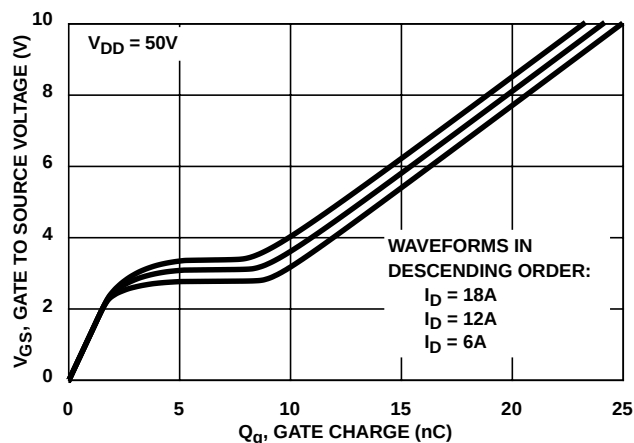


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

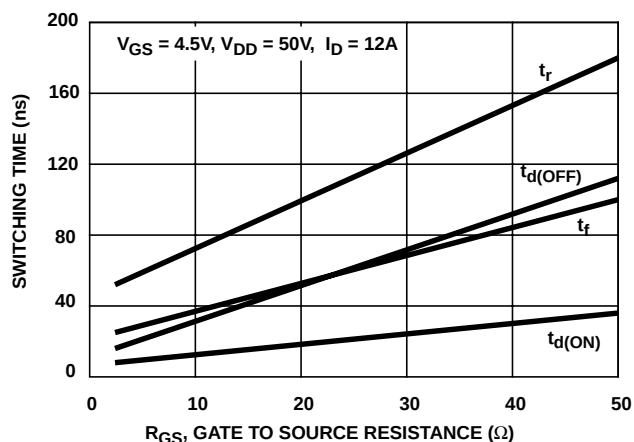


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

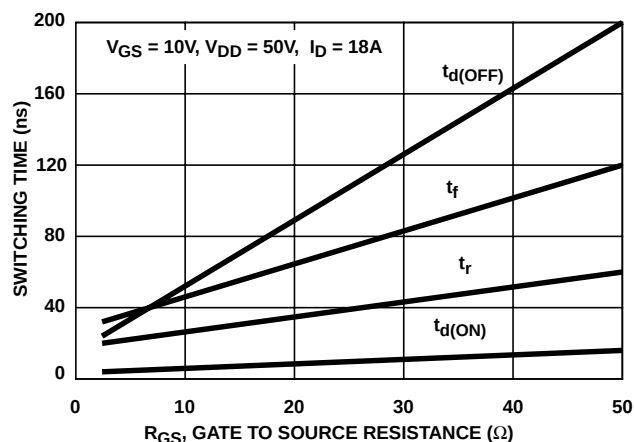


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

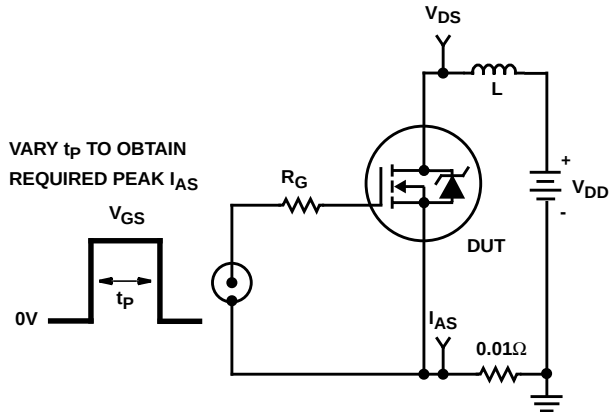


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

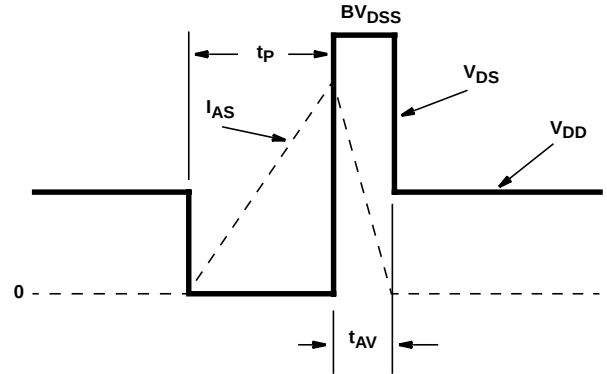


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

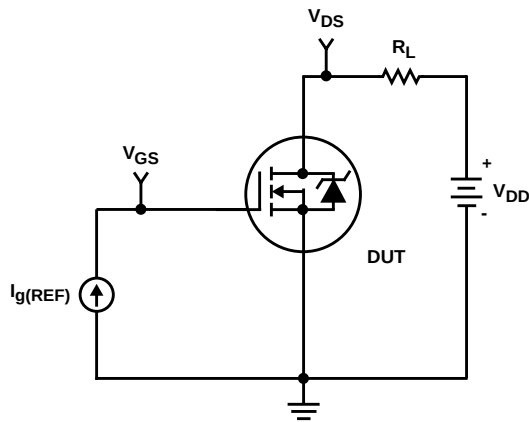


FIGURE 19. GATE CHARGE TEST CIRCUIT

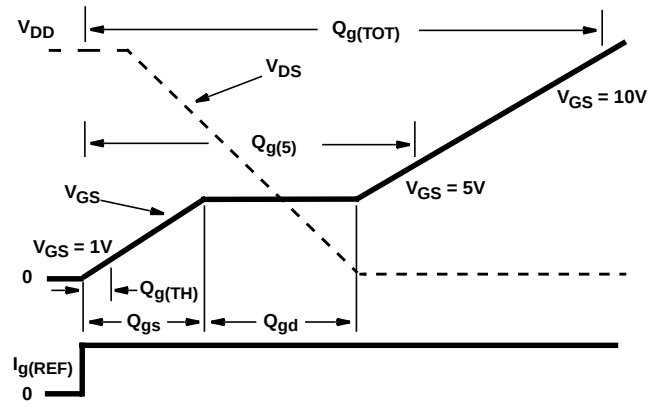


FIGURE 20. GATE CHARGE WAVEFORMS

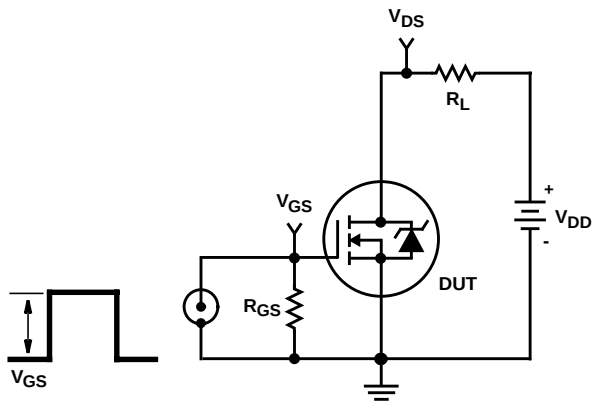


FIGURE 21. SWITCHING TIME TEST CIRCUIT

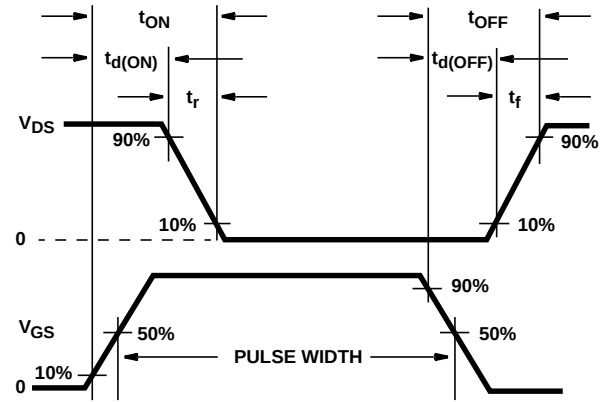


FIGURE 22. SWITCHING TIME WAVEFORM

SABER Electrical Model

REV 28 August 1999

template huf76619 n2,n1,n3

electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is = 5.9e-13, cjo = 9.0e-10, tt = 1e-7, m = 0.65)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 9e-10, is = 1e-30, m = 0.9, n = 10)
m..model mmedmod = (type=_n, vto = 1.85, kp = 4, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.22, kp = 50, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.60, kp = 0.05, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -4.5, voff = -2.0)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -2.0, voff = -4.5)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -0.3, voff = 0.2)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.2, voff = -0.3)
```

c.ca n12 n8 = 1.3e-9

c.cb n15 n14 = 1.4e-9

c.cin n6 n8 = 7.5e-10

d.dbody n7 n71 = model=dbodymod

d.dbreak n72 n11 = model=dbreakmod

d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1.0e-9

l.lgate n1 n9 = 1.73e-10

l.lsource n3 n7 = 6.12e-10

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u

m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1 = 1.05e-3, tc2 = -5e7

res.rbody n71 n5 = 1.3e-2, tc1 = 1e-5, tc2 = 0

res.rdbreak n72 n5 = 5.80e-1, tc1 = 1e-3, tc2 = -2e-5

res.rdrain n50 n16 = 3.95e-2, tc1 = 11.5e-3, tc2 = 2.6e-5

res.rgate n9 n20 = 2.95

res.rldrain n2 n5 = 10

res.rlgate n1 n9 = 1.7

res.rlsource n3 n7 = 6.1

res.rslc1 n5 n51 = 1e-6, tc1 = 3e-3, tc2 = 1.0e-6

res.rslc2 n5 n50 = 1e3

res.rsource n8 n7 = 23e-3, tc1 = 1e-3, tc2 = 1e-6

res.rvtemp n18 n19 = 1, tc1 = -1.5e-3, tc2 = 1.0e-6

res.rvthres n22 n8 = 1, tc1 = -1.8e-3, tc2 = -6.5e-6

spe.ebreak n11 n7 n17 n18 = 117.5

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

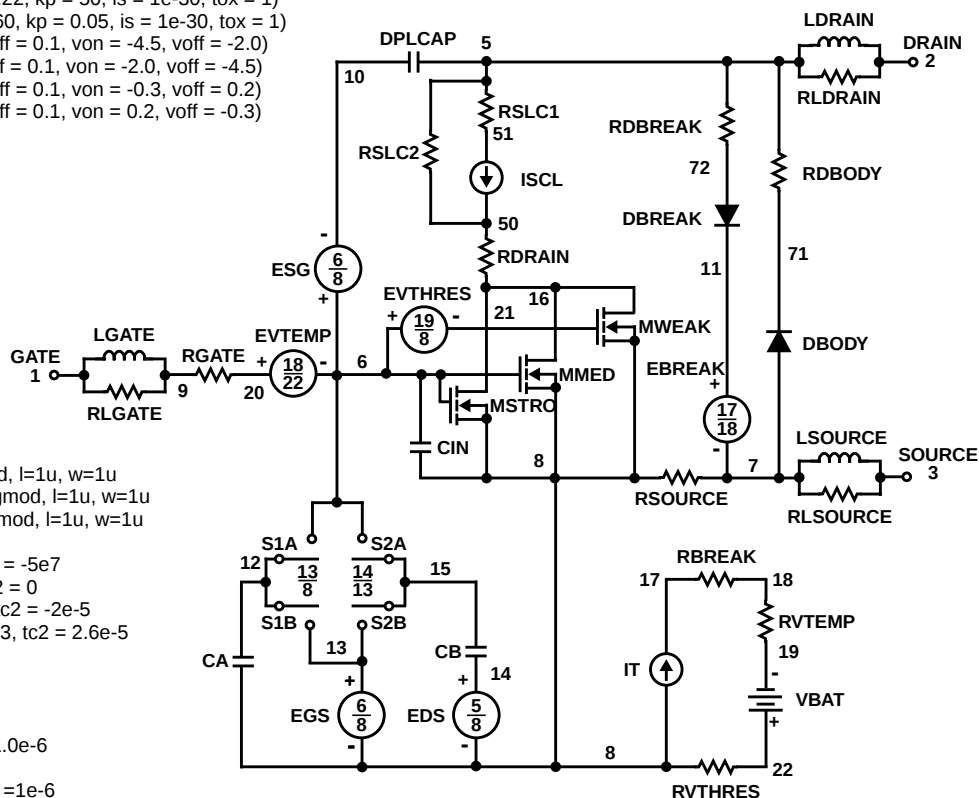
equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = (((v(n5,n51))/(1e-9+abs(v(n5,n51))))*(abs(v(n5,n51)*1e6/35))** 3.7))

}

}



SPICE Thermal Model

REV 28August 1999

HUF76619T

CTHERM1 th 6 1.0e-3
CTHERM2 6 5 3.0e-3
CTHERM3 5 4 4.0e-3
CTHERM4 4 3 7.0e-3
CTHERM5 3 2 1.0e-2
CTHERM6 2 tl 5.0e-1

R THERM1 th 6 9.31e-3
R THERM2 6 5 8.11e-2
R THERM3 5 4 2.0e-1
R THERM4 4 3 4.5e-1
R THERM5 3 2 7.0e-1
R THERM6 2 tl 2.0e-1

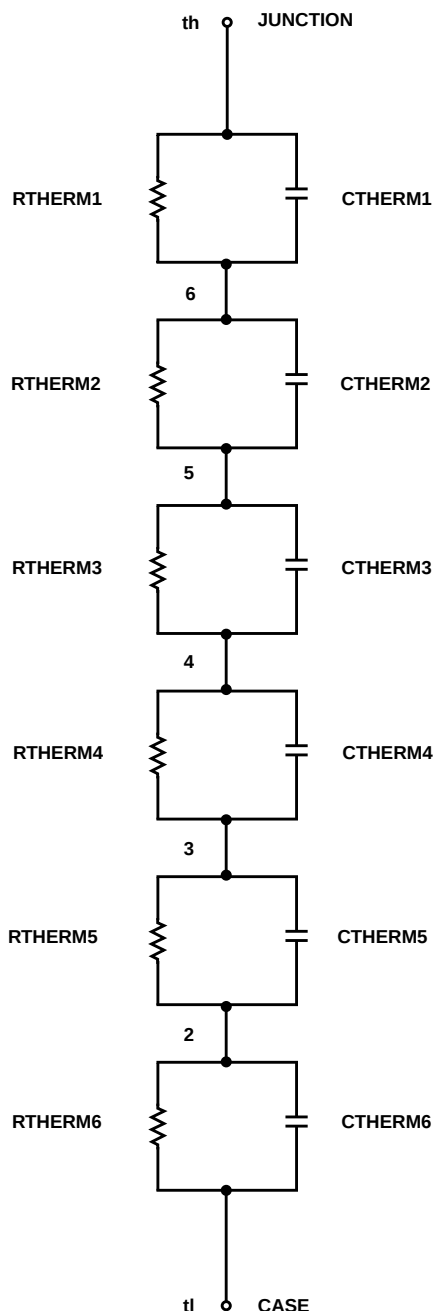
SABER Thermal Model

SABER thermal model HUF76619T

template thermal_model th tl
thermal_c th, tl

```
{
  ctherm.ctherm1 th 6 = 1.0e-3
  ctherm.ctherm2 6 5 = 3.0e-3
  ctherm.ctherm3 5 4 = 4.0e-3
  ctherm.ctherm4 4 3 = 7.0e-3
  ctherm.ctherm5 3 2 = 1.0e-2
  ctherm.ctherm6 2 tl = 5.0e-1
```

```
  rtherm.rtherm1 th 6 = 9.31e-3
  rtherm.rtherm2 6 5 = 8.11e-2
  rtherm.rtherm3 5 4 = 2.0e-1
  rtherm.rtherm4 4 3 = 4.5e-1
  rtherm.rtherm5 3 2 = 7.0e-1
  rtherm.rtherm6 2 tl = 2.0e-1
}
```



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