

Single 16-Channel/Differential 8-Channel CMOS Analog Multiplexers

April 1997

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- ON-Resistance 100Ω (Max)
- Low Power Consumption ($P_D < 1.2\text{mW}$)
- Fast Transition Time (300ns Max)
- Low Charge Injection
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Battery Operated Systems
- Data Acquisition
- Medical Instrumentation
- Hi-Rel Systems
- Communication Systems
- Automatic Test Equipment

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG406AK/883	-55 to 125	28 Ld Cerdip	F28.6
DG407AK/883	-55 to 125	28 Ld Cerdip	F28.6

Description

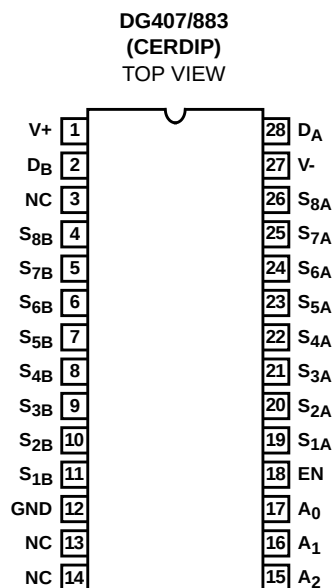
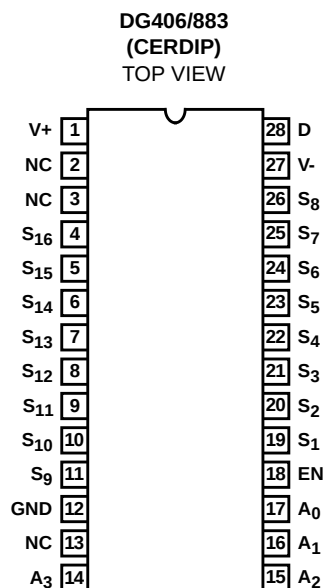
The DG406/883 and DG407/883 monolithic CMOS analog multiplexers are drop-in replacements for the popular DG506A/883 and DG507A/883 series devices. They each include an array of sixteen analog switches, a TTL and CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

These multiplexers feature lower signal ON resistance ($< 100\Omega$) and faster transition time ($t_{\text{TRANS}} < 250\text{ns}$) compared to the DG506A/883 and DG507A/883. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG406 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V_{P-P} signals when operating with $\pm 15\text{V}$ power supplies.

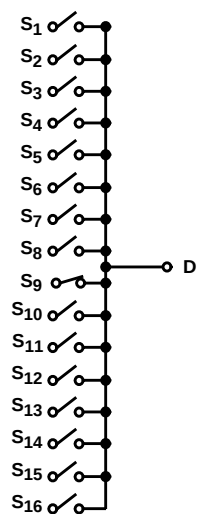
The sixteen switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a $\pm 5\text{V}$ analog input range.

Pinouts

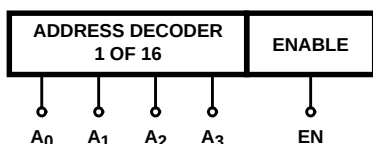


Functional Block Diagrams

DG406



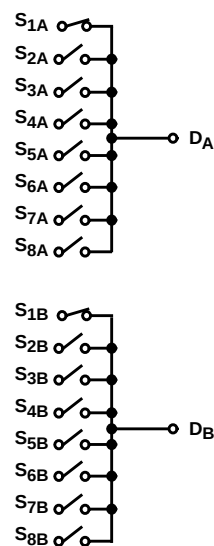
TO DECODER LOGIC
CONTROLLING BOTH
TIERS OF MUXING



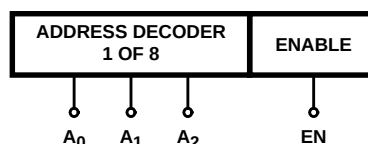
DG406 TRUTH TABLE

A ₃	A ₂	A ₁	A ₀	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG407



TO DECODER LOGIC
CONTROLLING BOTH
TIERS OF MUXING



DG407 TRUTH TABLE

A ₂	A ₁	A ₀	EN	ON SWITCH PAIR
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} < 0.8V$
 Logic "1" = $V_{AH} > 2.4V$
 X = Don't Care

DG406/883, DG407/883

Absolute Maximum Ratings

Voltages Referenced to V-

V++44.0V
 GND 25V
 Digital Inputs, V_S, V_D (Note 1) (V-) -2V to (V+) +2V or 20mA,
 Whichever Occurs First
 Current (Any Terminal) 30mA
 Peak Current, S or D 100mA
 (Pulsed 1ms, 10% Duty Cycle Max)

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W) θ_{JC} (°C/W)
 CERDIP Package 55 12
 Maximum Junction Temperature 150°C
 Maximum Storage Temperature Range -65°C to 150°C

Operating Conditions

Temperature Range -55°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices tested at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB- GROUP	DEVICE TYPE	(NOTE 3) MIN	(NOTE 3) MAX	UNITS	
Drain-Source ON Resistance	r _{DS(ON)}	V _D = 10V, I _S = -10mA V _D = -10V, I _S = 10mA (Note 4)	1, 3	All	-	90	Ω	
			2	All	-	120	Ω	
Matching Between Channels	Δr _{DS(ON)}	r _{DS(ON)} Max - r _{DS(ON)} Min (Note 3)	1	All	-	15	Ω	
Source OFF Leakage Current	I _{S(OFF)}	V _{EN} = 0V, V _S = ±10V, V _D = +10V	1	All	-0.5	0.5	nA	
			2, 3	All	-50	50	nA	
Drain OFF Leakage Current DG406	I _{D(OFF)}	V _{EN} = 0V, V _S = ±10V, V _D = +10V	1	DG406	-1	1	nA	
			2, 3		-200	200	nA	
			DG407	1	DG407	-1	1	nA
				2, 3		-100	100	nA
Drain ON Leakage Current DG406	I _{D(ON)}	V _S = V _D = ±10V Sequence Each Switch ON (Note 4)	1	DG406	-1	1	nA	
			2, 3		-200	200	nA	
			DG407	1	DG407	-1	1	nA
				2, 3		-100	100	nA
Logic High Input Current	I _{AH}	V _A = 2.4V, 15V	1, 2, 3	All	-1	1	μA	
Logic Low Input Current	I _{AL}	V _{EN} = 0V, 2.4V, V _A = 0V	1, 2, 3	All	-1	1	μA	
Positive Supply Current	I _{CC}	V _{EN} = 2.4V, V _A = 0V	1	All	-	100	μA	
			2, 3	All	-	500	μA	
Negative Supply Current	I _{EE}		1	All	-1	-	μA	
			2, 3	All	-10	-	μA	

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices tested at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB- GROUP	DEVICE TYPE	(NOTE 3) MIN	(NOTE 3) MAX	UNITS
Positive Standby Current	I _{CC} Standby	V _{EN} = V _A = 0V or 5V	1	All	-	30	μA
			2, 3	All	-	75	μA
Negative Standby Current	I _{EE} Standby		1	All	-1	-	μA
			2, 3	All	-10	-	μA

NOTES:

- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

TABLE 1A. ELECTRICAL PERFORMANCE SPECIFICATIONS (SINGLE SUPPLY)

Devices tested at +V_{SUPPLY} = +12V, -V_{SUPPLY} = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB- GROUP	DEVICE TYPE	MIN	MAX	UNITS
Drain-Source ON Resistance	r _{DS(ON)}	V _D = 3V, 10V I _S = -1mA	1	All	-	120	Ω
Positive Current	I _{CC}	V _{EN} = 0V or 5V, V _A = 0V or 5V	1	All	-	30	μA
			2, 3	All	-	75	μA
Negative Current	I _{EE}		1	All	-1	-	μA
			2, 3	All	-5	-	μA
Switching Time of Multiplexer	t _{TRANS}	V _{S1} = 8V, V _{SS} = 0V, V _{IN} = 2.4V	1	All	-	450	ns
Enable Turn-ON Time	t _{ON(EN)}	V _{INH} = 2.4V, V _{INL} = 0V, V _{S1} = 5V	1	All	-	600	ns
Enable Turn-OFF Time	t _{OFF(EN)}		1	All	-	300	ns

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices tested at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB- GROUP	DEVICE TYPE	MIN	MAX	UNITS
Transition Time	t _{TRANS}	C _L = 35pF, R _L = 300Ω, See Figure 1	9	All	-	300	ns
			10, 11	All	-	400	ns
Enable Turn-ON Time	t _{ON(EN)}	C _L = 35pF, R _L = 300Ω, See Figure 2	9	All	-	200	ns
			10, 11	All	-	400	ns
Enable Turn-OFF Time	t _{OFF(EN)}		9	All	-	150	ns
			10, 11	All	-	300	ns
Break Before Leakage Current	t _{OPEN}	C _L = 35pF, R _L = 300Ω, See Figure 3	9	All	25	-	ns
			10, 11	All	10	-	ns

DG406/883, DG407/883

TABLE 3. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Devices tested at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP (°C)	MIN	TYP	MAX	UNITS
Off Isolation Time	V _{ISO}	V _{EN} = 0V, R _L = 1K, f = 100kHz, GEN = 1V _{P-P} Sine Wave, See Figure 5	5	25	50	-	-	dB
Charge Transfer Error	V _{CTE}	C _L = 10nF, V _S = 0V, R _S = 0Ω, See Figure 4	5	25	-	-	10	mV
Crosstalk	V _{CT}	R _L = 1K, f = 100kHz, GEN = 1V _{P-P} Sine Wave, See Figure 5	5	25	50	-	-	dB
Source OFF Capacitance	C _{S(OFF)}	V _{EN} = 0V, V _S = 0V, f = 1MHz	65	25	-	-	10	pF
Drain OFF Capacitance DG406	C _{D(OFF)}	V _{EN} = 0V, V _D = 0V, f = 1MHz	5	25	-	-	200	pF
DG407			5	25	-	-	100	pF
Drain ON Capacitance DG406	C _{D(ON)}	V _{EN} = 0V, V _D = 0V, f = 1MHz	5	25	-	-	400	pF
DG407			5	25	-	-	200	pF

NOTE:

- Parameters listed via process parameters and are not directly tested at final production. These parameters are lab characterized upon design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production rich reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn0In)	1
Final Electrical Test Parameters	1 (Note 6), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Group C and D Endpoints	1

NOTE:

- PDA applied to Subgroup 1 only.

Test Circuits and Waveforms

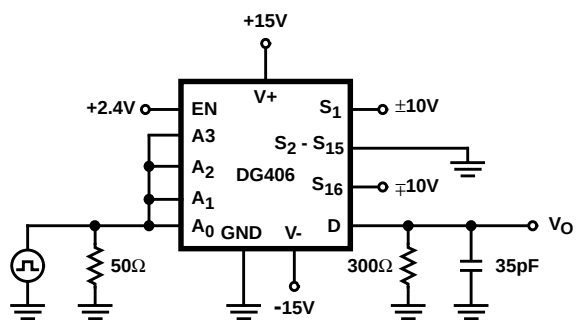


FIGURE 1A.

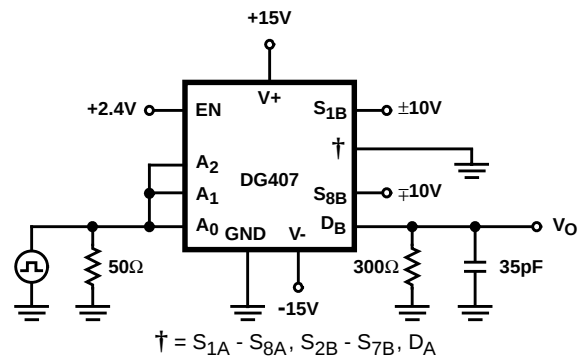


FIGURE 1B.

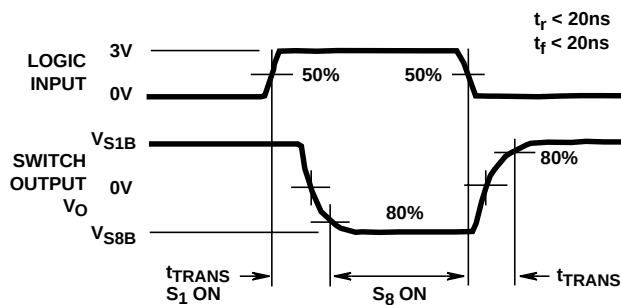


FIGURE 1C.

FIGURE 1. TRANSITION TIME

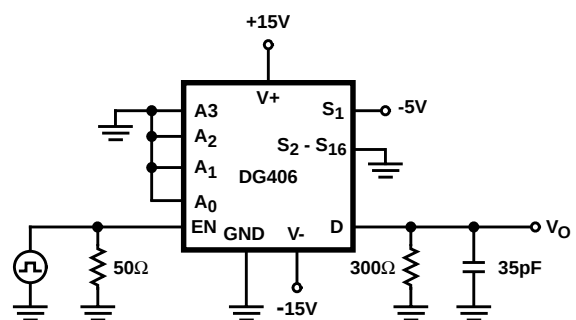


FIGURE 2A.

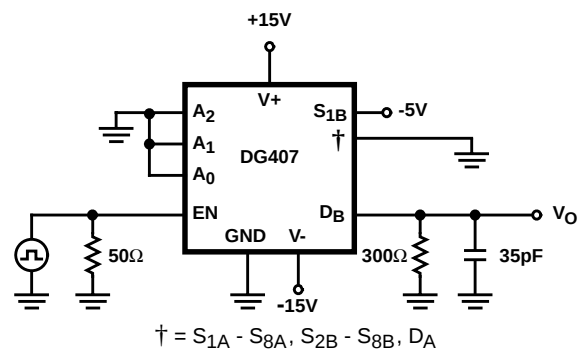


FIGURE 2B.

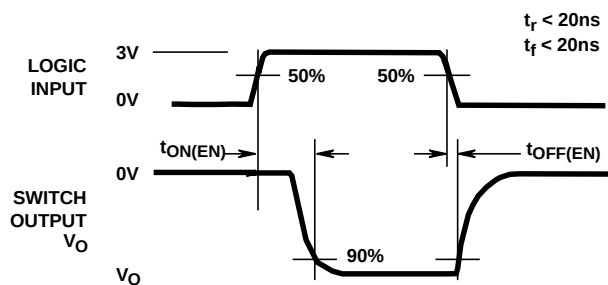


FIGURE 2C.

FIGURE 2. ENABLE SWITCHING TIME

Test Circuits and Waveforms (Continued)

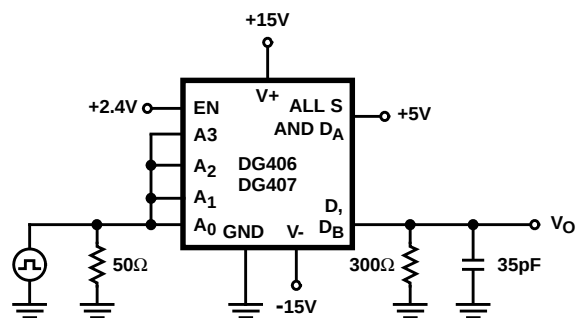


FIGURE 3A.

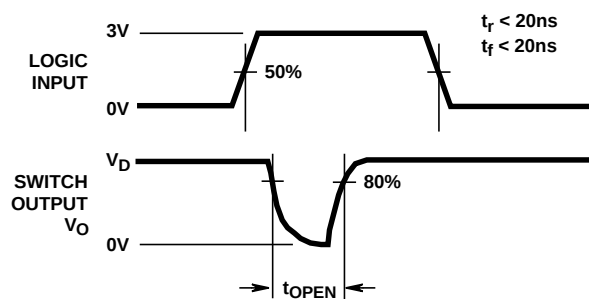


FIGURE 3B.

FIGURE 3. BREAK-BEFORE-MAKE INTERVAL

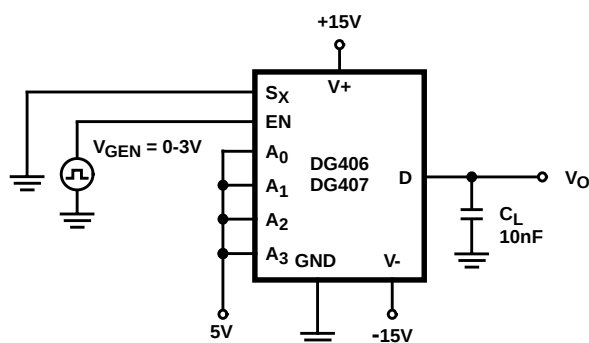


FIGURE 4. CHARGE INJECTION

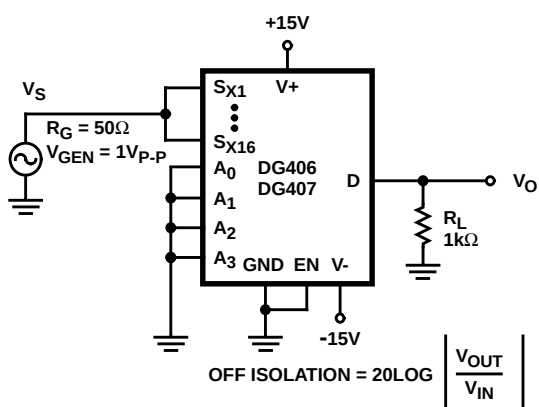
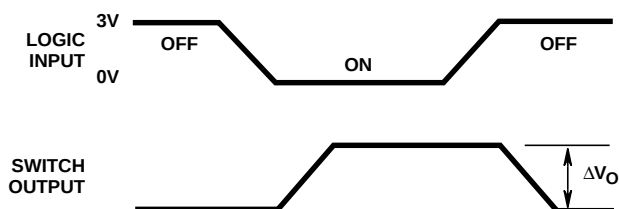


FIGURE 5. OFF ISOLATION

$$\text{OFF ISOLATION} = 20 \log \left| \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right|$$

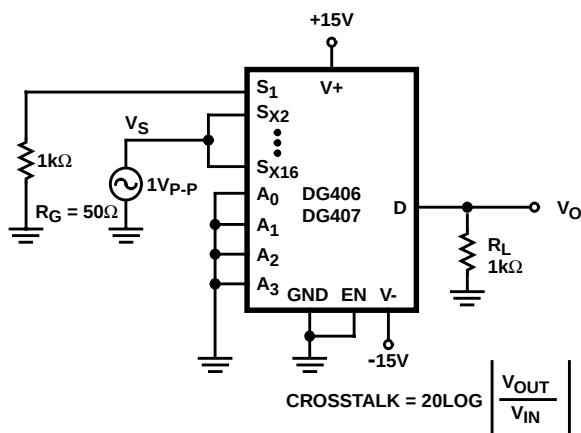
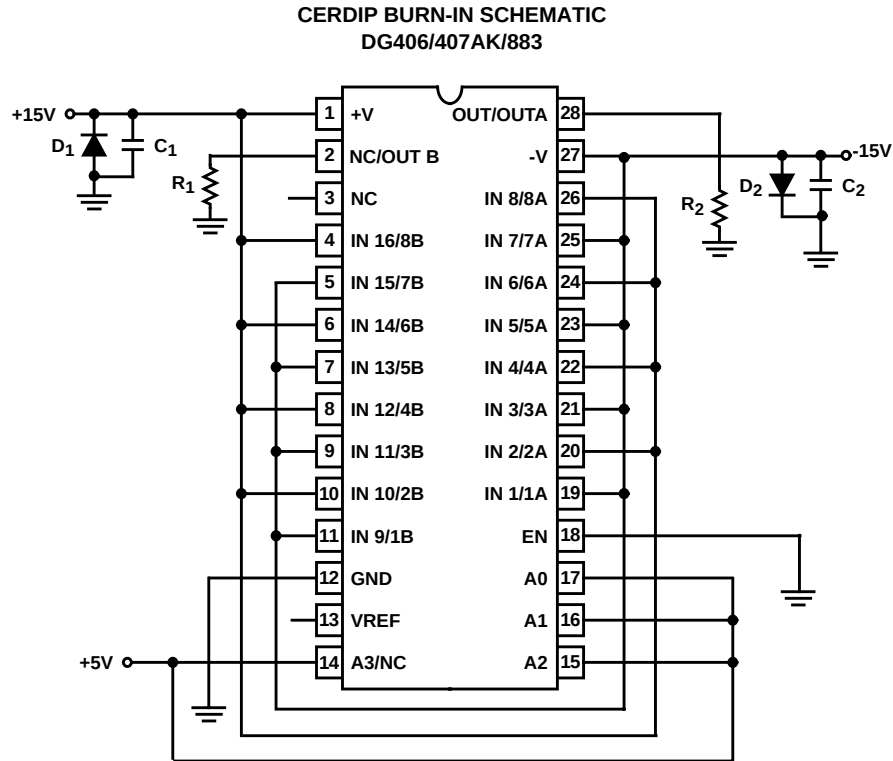


FIGURE 6. CROSSTALK

$$\text{CROSSTALK} = 20 \log \left| \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right|$$

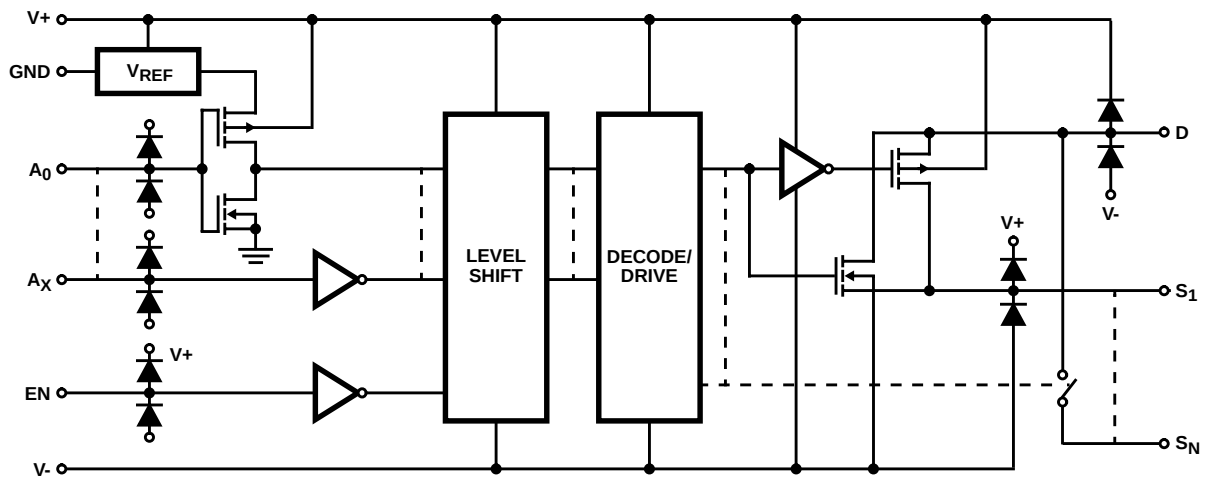
Burn-In Circuit



NOTE:

$R_1, R_2 = 10k\Omega \pm 5\%$, 1/2W or 1/4W (Per Socket)
 $C_1, C_2 = 0.01\mu F$ (Min, Per Socket) or $0.1\mu F$ (Min, Per Row)
 $D_1, D_2 = IN402$ (or Equivalent, Per Board)

Schematic Diagram (Typical Channel)



Typical Design Information

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves

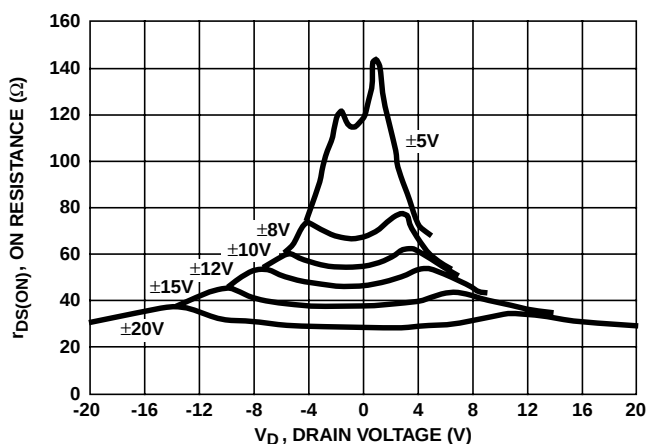


FIGURE 7. $r_{DS(ON)}$ vs V_D AND SUPPLY

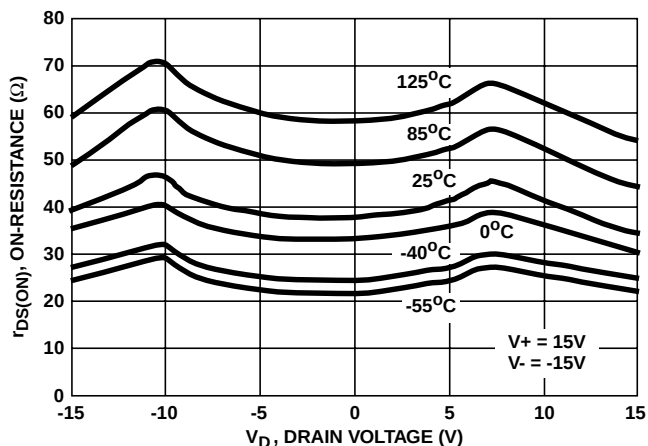


FIGURE 8. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

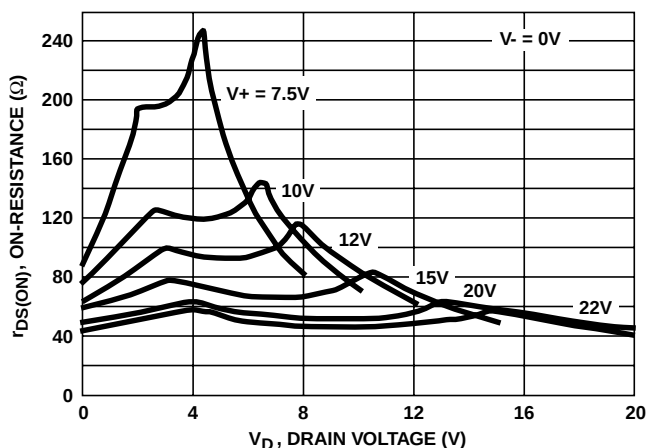


FIGURE 9. $r_{DS(ON)}$ vs V_D AND SUPPLY

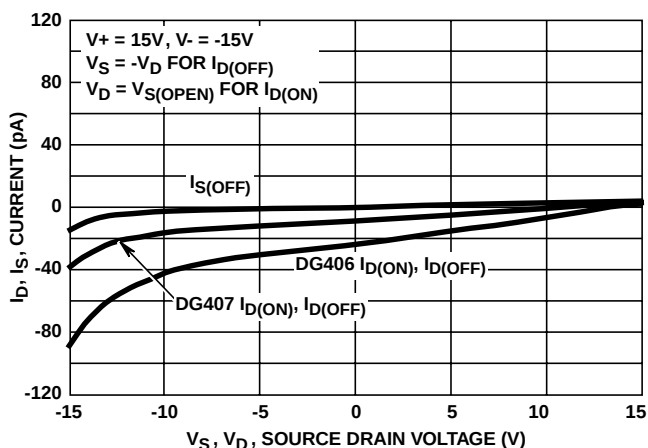


FIGURE 10. I_D , I_S LEAKAGE CURRENTS vs ANALOG VOLTAGE

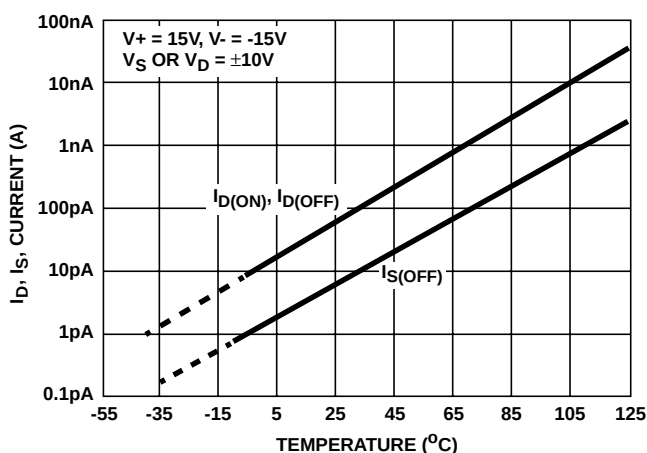


FIGURE 11. I_D , I_S LEAKAGE vs TEMPERATURE

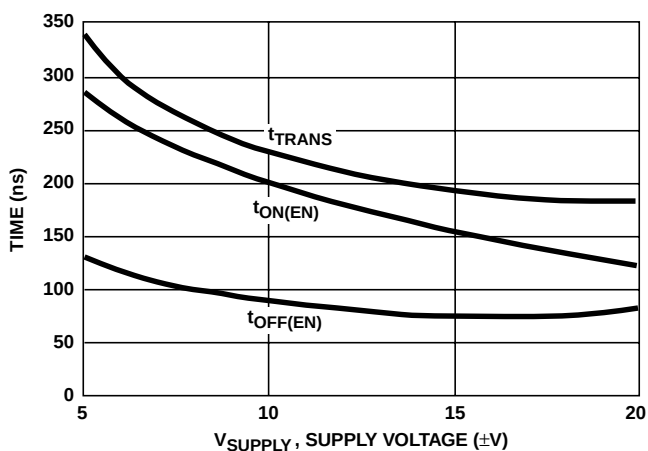


FIGURE 12. SWITCHING TIMES vs BIPOLAR SUPPLIES

Typical Performance Curves (Continued)

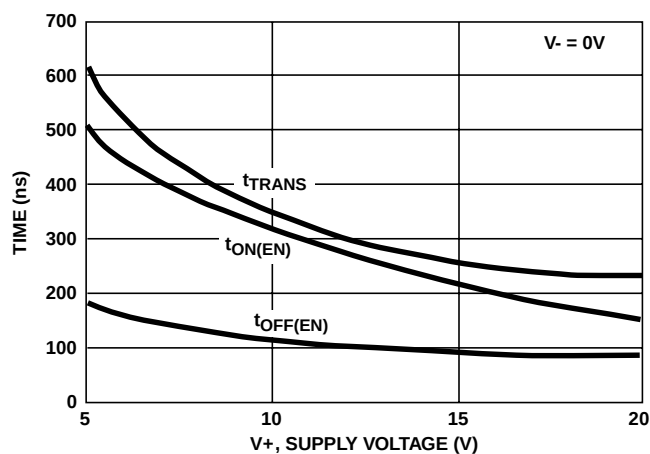


FIGURE 13. SWITCHING TIMES vs SINGLE SUPPLY

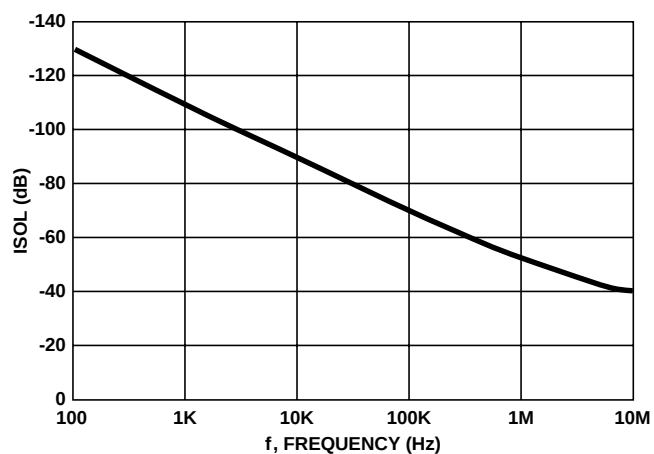


FIGURE 14. OFF-ISOLATION vs FREQUENCY

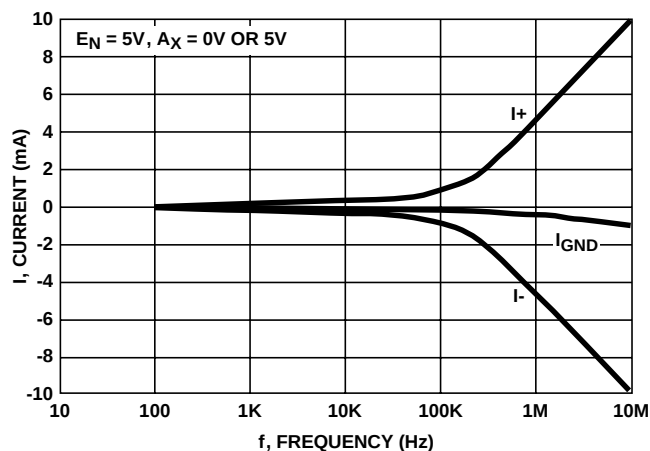


FIGURE 15. SUPPLY CURRENTS vs SWITCHING FREQUENCY

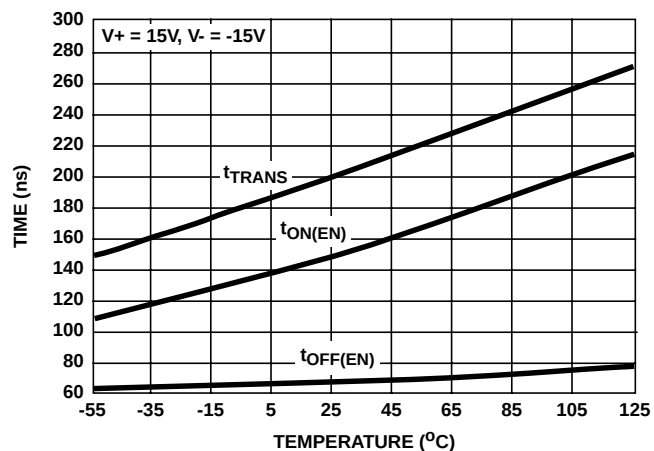


FIGURE 16. t_{ON}/t_{OFF} vs TEMPERATURE

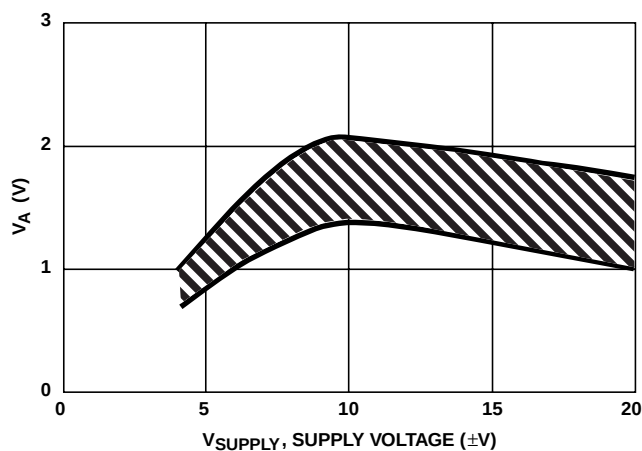


FIGURE 17. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

2490 μ m x 4560 μ m x 485 μ m $\pm$ 25 μ m

METALLIZATION:

Type: SiAl

Thickness: 12k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

PASSIVATION:

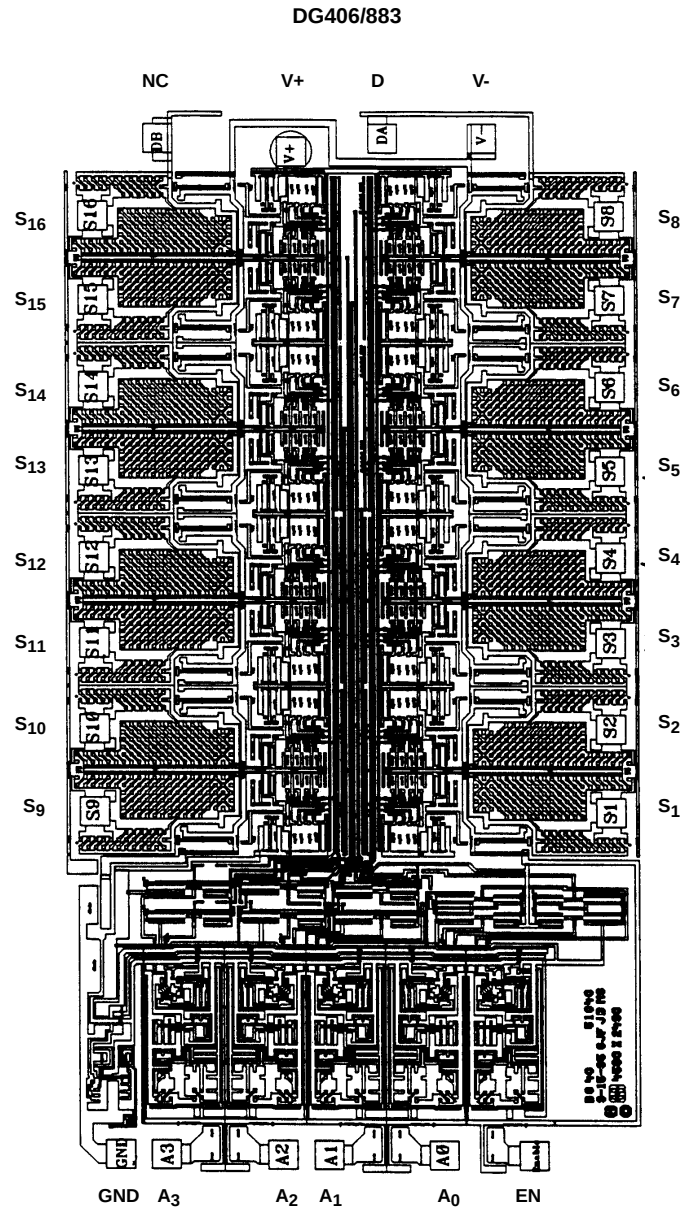
Type: Nitride

Thickness: 8k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout



Die Characteristics

DIE DIMENSIONS:

2490 μ m x 4560 μ m x 485 μ m $\pm$ 25 μ m

METALLIZATION:

Type: SiAl

Thickness: 12k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

PASSIVATION:

Type: Nitride

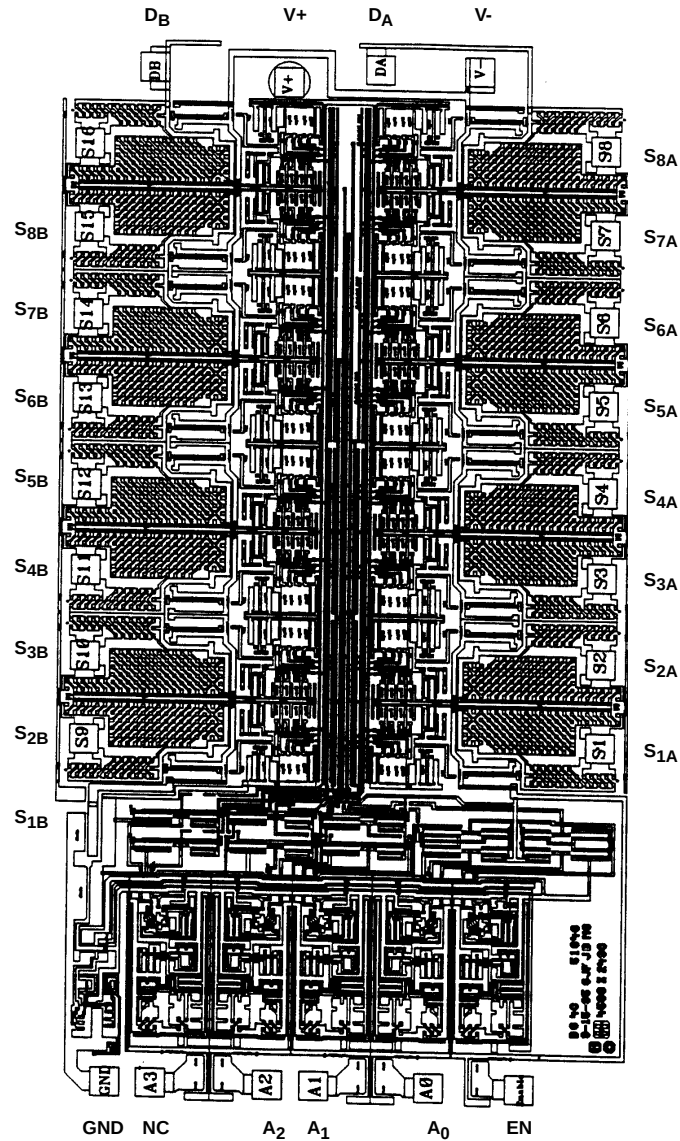
Thickness: 8k $\text{\AA}$ $\pm$ 1k $\text{\AA}$

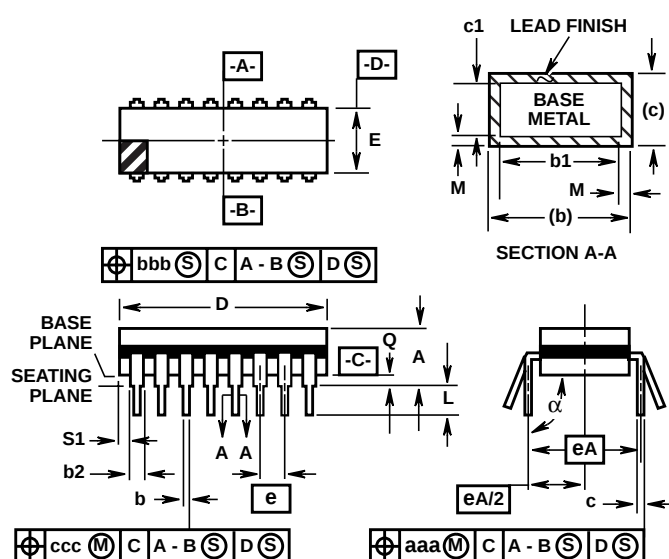
WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout

DG407/883



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

**F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

Rev. 0 4/94

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