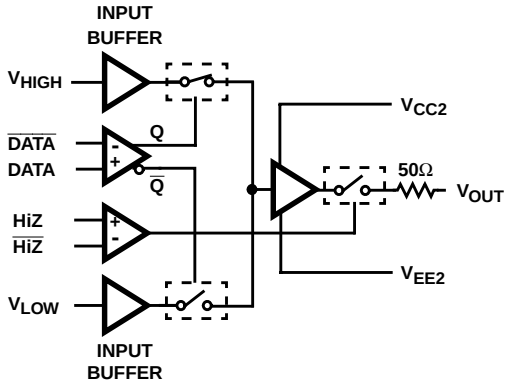
Data Sheet | September 1998 | File Number 3689.4

## 800MHz Monolithic Pin Driver

The HFA5251 is a very high speed monolithic pin driver solution for high performance test systems. The device will switch at high data rates between two input voltage levels providing variable amplitude pulses. The output impedance is trimmed to achieve a precision 50Ω source for impedance matching. Two differential ECL/TTL compatible inputs control the operation of the HFA5251, one controlling the $V_{HIGH}/V_{LOW}$ switching and the other controlling the output's high-impedance state. The HFA5251's 800MHz data rate makes it compatible with today's high-speed VLSI test systems and the +7V to -2V output swing allows testing of all common logic families.

The HFA5251 is manufactured in Intersil's proprietary complementary bipolar UHF-1 process. The HFA5251 is offered in die form. Contact your local sales representative for packaging options.

## Functional Diagram




**TRUTH TABLE FOR $V_{OUT}$**

| | | DATA | |
|---|---|---|---|
| | | 0 | 1 |
| HiZ | 0 | $V_{LOW}$ | $V_{HIGH}$ |
| | 1 | HiZ | HiZ |

## Features

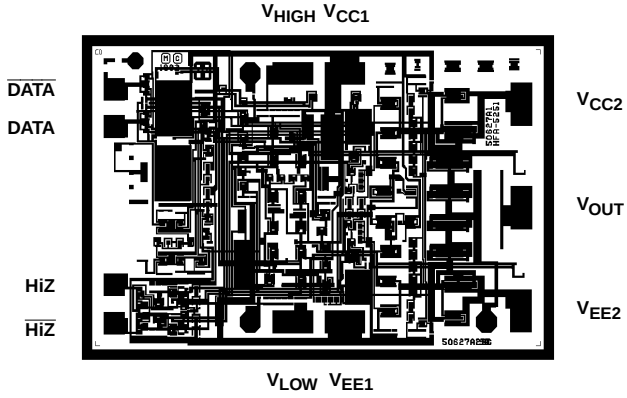
- High Digital Data Rate . . . . . 800MHz
- Very Fast Rise/Fall Times. . . . . 500ps
- Wide Output Range . . . . . +7V to -2V
- Precise 50Ω Output Impedance
- High Impedance, Three-State Output Control

## Applications

- IC Tester Pin Electronics
- Pattern Generators
- Pulse Generators
- Level Comparator/Translator

## Pinout

**HFA5251 (DIE FORM)**



## Pin Descriptions

| NAME | FUNCTION |
|---|---|
| $V_{CC1}$ | Positive Supply. Nominal value is 10V ±0.2V. Reducing supply voltage below 9.8V will reduce positive output voltage swing. The total supply voltage from $V_{CC1}$ to $V_{EE1}$ should not exceed 15.6V for normal operation or exceed 17.0V to prevent damage. Intersil recommends two wire bonds to this pad to provide the lowest possible impedance. In addition, power supply decoupling chip capacitors of 470pF, 0.1µF and a 10µF tantalum are recommended. |
| $V_{EE1}$ | Negative Supply. Nominal value is -5.2V ±0.2V. A supply voltage more positive than -5.0V will reduce negative output voltage swing. The total supply voltage from $V_{CC1}$ to $V_{EE1}$ should not exceed 15.6V for normal operation or exceed 17.0V to prevent damage. Intersil recommends two wire bonds to this pad to provide the lowest possible impedance. In addition, power supply decoupling chip capacitors of 470pF, 0.1µF and a 10µF tantalum are recommended. |
| $V_{CC2}$ | Output Stage Positive Supply. Nominal voltage and cautions are the same as for $V_{CC1}$. Having decoupling chip capacitors close to $V_{CC2}$ and $V_{EE2}$ is essential since large AC current will flow through this pad to the output during transients. Normally $V_{CC1}$ and $V_{CC2}$ are connected together close to the die and share decoupling capacitors. Intersil recommends two wire bonds for this pad. |
| $V_{EE2}$ | Output Stage Negative Supply. Nominal voltage and cautions are the same as for $V_{EE1}$. Having decoupling chip capacitors close to $V_{CC2}$ and $V_{EE2}$ is essential since large AC current will flow through this pad to the output during transients. Normally $V_{EE1}$ and $V_{EE2}$ are connected together close to the die and share decoupling capacitors. Intersil recommends two wire bonds for this pad. |
| $V_{HIGH}$ | Input Voltage High is used to set the output high level $V_{OH}$. $V_{HIGH}$ is sensitive to capacitively coupled AC noise. Protection from high frequency noise can be achieved with a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this precaution the pin driver may oscillate due to feedback from the output through the PC board ground. |
| $V_{LOW}$ | Input Voltage Low is used to set the output low level $V_{OL}$. $V_{LOW}$ is sensitive to capacitively coupled AC noise. Protection from high frequency noise can be achieved with a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this precaution the pin driver may oscillate due to feedback from the output through the PC board ground. |
| $V_{OUT}$ | Driver Output. The output impedance has been laser trimmed to match a 50Ω transmission line ±2Ω. Custom output impedance trimming is available (contact sales office for details) to provide the best match possible to your 50Ω system. |
| $\overline{DATA}$, DATA | Differential Digital Inputs used to switch $V_{OUT}$ to the $V_{HIGH}$ or $V_{LOW}$ level. Intersil recommends this input pair be driven by complementary ECL signals to provide optimal switching speeds and timing accuracy. However a large Common Mode and Differential Voltage Range is provided to accommodate a variety of signals including single ended TTL and CMOS. When using single ended signals the other input must be tied to an appropriate threshold. |
| $\overline{HiZ}$, HiZ | Differential Digital Inputs used to switch $V_{OUT}$ from an Active to a High Impedance State. Intersil recommends that this input pair be driven by complementary ECL signals to provide optimal switching speeds and timing accuracy. However a large Common Mode and Differential Voltage Range is provided to accommodate a variety of signals including single ended TTL and CMOS. When using single ended signals the other input must be tied to an appropriate threshold. |

## Absolute Maximum Ratings

Supply Voltage . . . . . 17V
Differential Input Voltage (DATA and HiZ) . . . . . 5V
Output Current Continuous (Note 1) . . . . . 160mA
Input Voltage (Any pin except as specified) . . . . . $V_{CC}$ to $V_{EE}$
$V_{OUT}$ Voltage . . . . . 8V to -5.5V
$V_{HIGH}$ Voltage . . . . . $V_{CC}$ to -3V
$V_{LOW}$ Voltage . . . . . 8V to $V_{EE}$
$V_{HIGH}$ to $V_{LOW}$ Voltage . . . . . $V_{HIGH} > V_{LOW}$

## Thermal Information

Maximum Junction Temperature (Die) . . . . . $175^oC$
Maximum Storage Temperature Range . . . . . $-65^oC$ to $150^oC$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Electrical Specifications

$V_{CC}$ = +10V, $V_{EE}$ = -5.2V, $V_{IH}$ = -0.9V, $V_{IL}$ = -1.75V, Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP. ($^oC$) | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** ($V_{HIGH}$, $V_{LOW}$) | | | | | | |
| $V_{HIGH}$ Input Offset Voltage | $V_{OUT}$ = 0V | 25 | -150 | -50 | +50 | mV |
| $V_{LOW}$ Input Offset Voltage | $V_{OUT}$ = 0V | 25 | -150 | -50 | +50 | mV |
| $V_{HIGH}$ Input Bias Current | $V_{HIGH}$ = -2.25V to +7.5V | 25 | -50 | 110 | 300 | µA |
| $V_{LOW}$ Input Bias Current | $V_{LOW}$ = -2.5V to +7.25V | 25 | -300 | -110 | 50 | µA |
| $V_{HIGH}$ Voltage Range | | 25 | -2.25 | - | 7.5 | V |
| $V_{LOW}$ Voltage Range | | 25 | -2.5 | - | 7.25 | V |
| $V_{HIGH}$ to $V_{LOW}$ Differential Voltage Range | | 25 | 0.25 | - | 10 | V |
| $V_{HIGH}/V_{LOW}$ Interaction at 500mV (Note 11) | | 25 | - | 2 | 4 | mV |
| $V_{HIGH}/V_{LOW}$ Interaction at 250mV (Note 11) | | 25 | - | 20 | 40 | mV |
| **LOGIC INPUT CHARACTERISTICS** (DATA, $\overline{DATA}$, HiZ, $\overline{HiZ}$) | | | | | | |
| Logic Input Voltage Range | | 25 | -2 | - | 7 | V |
| Logic Differential Input Voltage | | 25 | 0.4 | - | 5 | V |
| DATA/$\overline{DATA}$ Logic Input High Current | $V_{IH}$ = 0V, $V_{IL}$ = -2V | 25 | -50 | 110 | 300 | µA |
| DATA/$\overline{DATA}$ Logic Input Low Current | $V_{IH}$ = 0V, $V_{IL}$ = -2V | 25 | -700 | -300 | 50 | µA |
| HiZ/$\overline{HiZ}$ Logic Input High Current | $V_{IH}$ = 0V, $V_{IL}$ = -2V | 25 | -50 | 70 | 200 | µA |
| HiZ/$\overline{HiZ}$ Logic Input Low Current | $V_{IH}$ = 0V, $V_{IL}$ = -2V | 25 | -300 | -80 | 50 | µA |
| **TRANSFER CHARACTERISTICS** | | | | | | |
| $V_{HIGH}$ Voltage Gain | $V_{HIGH}$ = -1V to 6.5V | 25 | 0.95 | - | 1 | V/V |
| $V_{LOW}$ Voltage Gain | $V_{LOW}$ = -1.5V to 6V | 25 | 0.95 | - | 1 | V/V |
| $V_{HIGH}/V_{LOW}$ Linearity Error (Note 7) | Fullscale = 5V | 25 | -0.5 | - | 0.5 | % |
| $V_{HIGH}/V_{LOW}$ Linearity Error (Note 8) | Fullscale = 8.5V | 25 | -0.75 | - | 0.75 | % |
| $V_{HIGH}/V_{LOW}$ End Point Gain Deviation (Notes 10, 13) | 0.5V Steps | 25 | -2.0 | - | 2.0 | % |
| $V_{HIGH}$ End Point Gain Error (Notes 10 and 14) | $V_{OUT}$ = 6.7V to 7.0V | 25 | -20 | - | 20 | mV |
| $V_{HIGH}/V_{LOW}$ -3dB Bandwidth | $200mV_{P-P}$ | 25 | - | 100 | - | MHz |
| **SWITCHING CHARACTERISTICS** ($Z_{LOAD}$ = 16 inches of RG-58 Terminated with 50Ω) | | | | | | |
| Propagation Delay (Notes 2, 17) | | 25 | 0.8 | - | 1.5 | ns |
| Propagation Delay Match (Notes 2, 17) | Rising to Falling Edge | 25 | -100 | - | 100 | ps |
| Rising Edge Propagation Delay vs Duty Cycle (Notes 12, 17) | | 25 | -120 | -20 | 80 | ps |
| Falling Edge Propagation Delay vs Duty Cycle (Notes 12, 17) | | 25 | -80 | 20 | 120 | ps |
| Active to HiZ Delay (Note 17) | | 25 | 1.2 | 1.7 | 2.2 | ns |
| HiZ to Active Delay (Note 17) | | 25 | 2.1 | 2.6 | 3.1 | ns |
| **TRANSIENT RESPONSE** ($Z_{LOAD}$ = 16 inches of RG-58 Terminated with 5pF) | | | | | | |
| Rise/Fall Time (20%-80%) | $1V_{P-P}$ | 25 | - | 450 | 500 | ps |
| Rise/Fall Time (10%-90%) | $3V_{P-P}$ | 25 | - | 890 | 1000 | ps |

**Electrical Specifications** $V_{CC}$ = +10V, $V_{EE}$ = -5.2V, $V_{IH}$ = -0.9V, $V_{IL}$ = -1.75V, Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP. ($^oC$) | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Rise/Fall Time (10%-90%) (Note 6) | $5V_{P-P}$ | 25 | - | 1.5 | 1.7 | ns |
| Rise/Fall Time Match (Note 6) | | 25 | - | 50 | 150 | ps |
| Minimum Pulse Width (Note 16) | $1V_{P-P}$ | 25 | - | 1.0 | - | ns |
| Minimum Pulse Width (Note 16) | $3V_{P-P}$ | 25 | - | 1.2 | - | ns |
| Minimum Pulse Width (Note 16) | $5V_{P-P}$ | 25 | - | 2.0 | - | ns |
| Overshoot/Undershoot/Preshoot | $3V_{P-P}$ | 25 | - | 5 | - | % |
| Data Settling Time to 1% (Note 3) | | 25 | - | 10 | - | ns |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output Voltage Swing (No Load) | $V_{CC}$ = 10V, $V_{EE}$ = -5.2V | 25 | -2 | - | 7 | V |
| | At Other Supplies | 25 | $V_{EE}$ +3.2 | - | $V_{CC}$ -3.0 | V |
| DC Output Resistance - Active (Note 18) | -2V to 7V | 25 | 45 | 47 | 49 | Ω |
| Output Leakage - HiZ | -2V to 7V | 25 | -100 | ±10 | 100 | nA |
| Output Capacitance - HiZ | | 25 | - | 5 | - | pF |
| Output Current - Active | | 25 | 70 | 100 | - | mA |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Rejection Ratio (Note 4) | $V_{HIGH}$ | 25 | - | 14 | 40 | mV/V |
| | $V_{LOW}$ | 25 | - | 14 | 40 | mV/V |
| Total Supply Current | | 25 | 90 | 94 | 96 | mA |
| Supply Current ($I_{CC1}$, $I_{EE1}$) | | 25 | - | 74 | - | mA |
| Supply Current ($I_{CC2}$, $I_{EE2}$) | | 25 | - | 20 | - | mA |
| Supply Voltage Range (Note 5) | $V_{CC}$ | 25 | 9.8 | 10 | 10.2 | V |
| Supply Voltage Range (Note 5) | $V_{EE}$ | 25 | -5.4 | -5.2 | -5.0 | V |
| Supply Voltage Differential | $V_{CC}$ - $V_{EE}$ | 25 | 12 | - | 15.6 | V |
| Power Dissipation | No Load At $V_{CC}$ = 10V, $V_{EE}$ = -5.2V | 25 | - | - | 1.46 | W |

NOTES:

1. Internal Power Dissipation may limit Output Current below 160mA.
2. 3V Step, 50% duty cycle, 200ns period.
3. 3V Step, measured from 50% of input to ±1% of reference value at 50ns.
4. $V_{HIGH}$ = 2.6V, $V_{LOW}$ = 2.3V, $V_{CC}$ = 9V to 10V, $V_{EE}$ = -4.2V to -5.2V
5. Minimum/maximum output swing will vary with supply voltage.
6. 5V Step, 50% duty cycle, 100ns period.
7. For $V_{HIGH}$ = 0V to 5V, For $V_{LOW}$ = 0V to 5V, Fullscale = 5V, 0.1% = 5mV.
8. For $V_{HIGH}$ = -1.5V to 7V, For $V_{LOW}$ = -2.0V to 6.5V, Fullscale = 8.5V, 0.1% = 8.5mV
9. Shorting the output to a voltage outside the specified range may damage the output.
10. $V_{CC}$ = 9.9V, $V_{EE}$ = -5.1V.
11. $V_{HIGH}$ to $V_{LOW}$ Interaction is measured as the change in $V_{OUT}$ (the active channel) due to a change in the inactive channel. $V_{HIGH}$ Interaction at 250mV is measured as the deviation from 1V as $V_{LOW}$ is changed from 0V to 750mV (Referred to $V_{OUT}$). $V_{Low}$ Interaction at 250mV is measured as the deviation from 0V as $V_{HIGH}$ is changed from 1V to 250mV (Referred to $V_{OUT}$).
12. 0V to 3V Step, 200ns period, Pulse Width is varied from 5ns to 195ns.
13. End Point Gain Deviation is the percent deviation of Gain calculated in 0.5V steps at the extremes of output voltage range. For example in the $V_{HIGH}$ range 5.7V to 6.7V, Gain is calculated for $V_{HIGH}$ = 5.7V to 6.2V (Note 15) and $V_{HIGH}$ = 6.2V to 6.7V (Note 15) the difference in gain is calculated and converted to a percentage. The voltage ranges tested are: $V_{HIGH}$ = -1.5V to -0.5V (Note 15) and 5.7V to 6.7V (Note 15), $V_{LOW}$ = -2.0V to -1.0V (Note 15) and 5.5V to 6.5V (Note 15).
14. $V_{HIGH}$ End Point Gain Error is the $V_{OUT}$ absolute error from ideal for a $V_{HIGH}$ change from 6.7V to 7.0V (Note 15).
15. Input voltages $V_{HIGH}$ and $V_{LOW}$ are corrected for Offset Voltage and 7.5V Full Scale Gain Error.
16. Minimum Pulse Width is measured 50% to 50% of specified amplitude with pulse peak at 90% of amplitude.
17. Test is performed into a 50Ω load with a 3V step. Measurement is made from the 50% of input to 50% of output.
18. Dynamic Output Resistance will be higher (typical 48.5Ω) than DC Output Resistance.

## Application Information

The HFA5251 is a pin driver designed for use in automatic test equipment (ATE) and high speed pulse generators. Pin drivers, especially those with very high-speed performance, have generally been implemented with discrete transistors (sometimes GaAs) on a circuit board or in a hybrid. Recent IC process improvements, specifically Intersil's UHF1 process [1], have enabled the manufacturing of this 800MHz silicon monolithic pin driver.

The ultra high speed performance of the HFA5251 is a result of UHF1 process leverages: low parasitic collector-to-substrate capacitance of the bonded wafer, low collector-to-base parasitic capacitance of the self-aligned base/emitter technology and ultra high $f_T$ NPN (8GHz) and PNP (5.5GHz) poly-silicon transistors.

## Functional Block Diagram

The HFA5251 functional block diagram is shown in Figure 1.

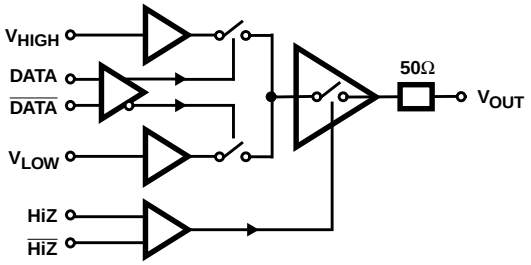



**FIGURE 1. BLOCK DIAGRAM**

The control inputs, DATA and $\overline{DATA}$, determine the output level. If DATA is at logic “1” and $\overline{DATA}$ is at logic “0”, the output level will be the same as $V_{HIGH}$. If DATA is at logic “0” and $\overline{DATA}$ is at logic “1”, the output will be the same as $V_{LOW}$. The control inputs, HiZ and $\overline{HiZ}$, make the output either active or high-impedance. If HiZ is at logic “1” and $\overline{HiZ}$ is at logic “0”, the output will be in high impedance mode. If HiZ is at logic “0” and $\overline{HiZ}$ is at logic “1”, the output will be enabled. The output impedance in the enabled mode is trimmed to 50Ω.

## Circuit Schematic

The Pin Driver circuit consists of a switch, an output buffer, and two differential control elements as shown in Figure 2.

A two stage approach, separating the switch from the output buffer, allows the speed and accuracy requirements of the switch to be de-coupled from the load driving capability of the buffer.

The patent pending switch circuitry[2] uses cascaded emitter followers as input buffers and also to switch the input $V_{HIGH}$ and $V_{LOW}$ to node VSO. Dual differential pairs controlled by the data timing (DATA and $\overline{DATA}$) direct current to select either the $V_{HIGH}$ or $V_{LOW}$ switch. Matching transistor types and transdiodes improve linearity and lowers the voltage offset and offset drift. Stacking two emitter-base junctions allows the $V_{HIGH}$ to $V_{LOW}$ range to be extended to two BVebo's of the process. The speed of the pin driver is largely determined by the current flowing through the switch stage and the collector-base capacitance of the output stage transistors connected to the node VSO.

The output stage consists of cascaded emitter followers constructed in a typical push-pull manner as shown in Figure 2. However, transdiodes are added to increase the voltage breakdown characteristics of the output during high impedance mode. HiZ and $\overline{HiZ}$ control the mode of the output stage. A trimmed, NiCr resistor is added to provide the 50Ω output impedance.

Overall, a symmetry of device types and paths is constructed to improve slew and delay symmetry. Both the $V_{HIGH}$ to $V_{OUT}$ path and the $V_{LOW}$ to $V_{OUT}$ path contain three NPN and three PNP transistors operating at similar collector currents. Thus the transient response of $V_{HIGH}$ to $V_{LOW}$ and $V_{LOW}$ to $V_{HIGH}$ are kept symmetrical. Also, a trimmable current reference (not shown) allows the AC parameters to be adjusted to maintain unit to unit consistency.

## Speed Advantage

Intersil Pin Drivers on bonded-wafer technology definitely have a speed advantage, coming from the low collector-to-substrate capacitance and the high $f_T$ of the transistors. In addition, the patent-pending switching stage which fits uniquely to Intersil's UHF1 process is another big contributor for the high speed. This switching circuitry requires low series-resistance NPN and PNP transdiodes available in UHF1. The rise and fall times of the pin driver are largely determined by the slew rate at the node VSO in Figure 2. The dominant mechanism for the slew rate is the charging/discharging of the collector-base capacitors of the transistors connected to the node VSO. The charging/discharging currents are coming from the switching stage current sources. The fast rise and fall times are achieved because of the negligible collector-to-substrate capacitance and the small base-collector capacitance due to the self-aligned recessed oxide [1].

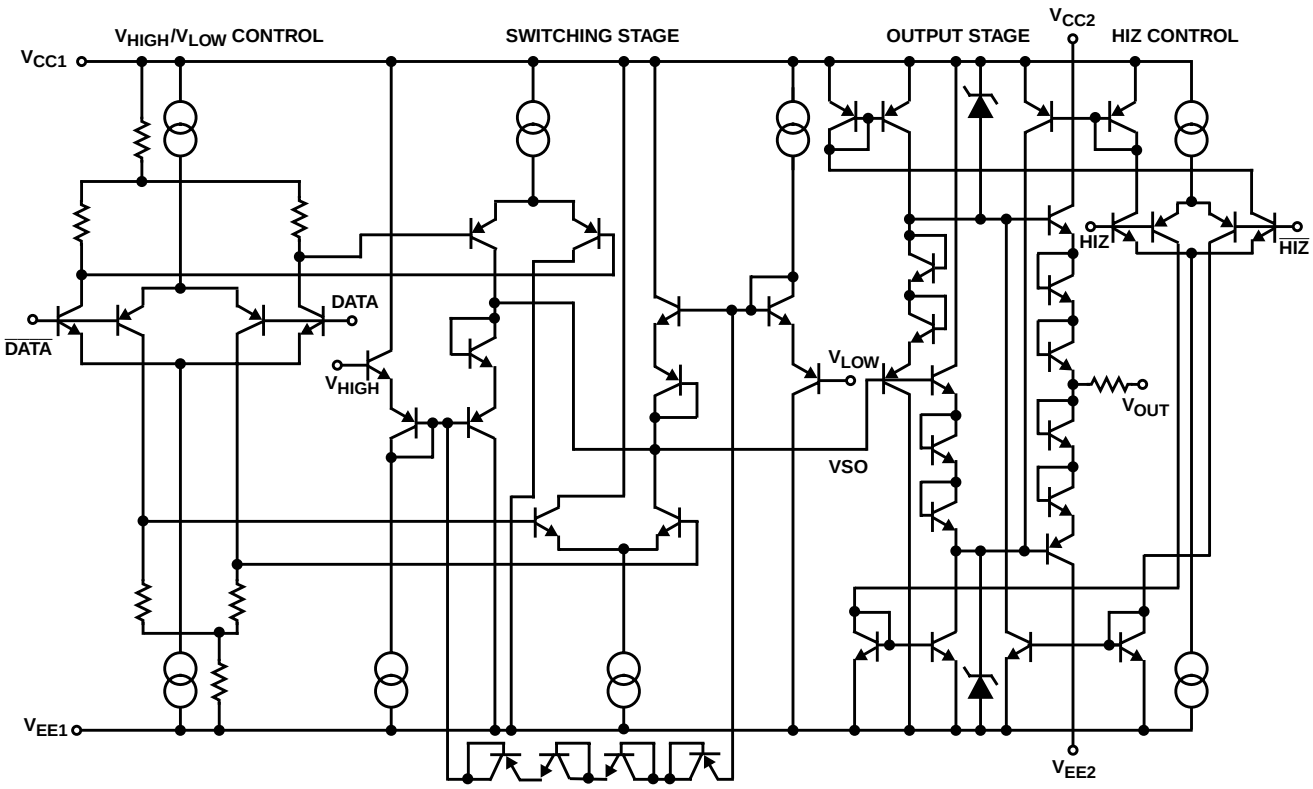



FIGURE 2. CIRCUIT SCHEMATIC

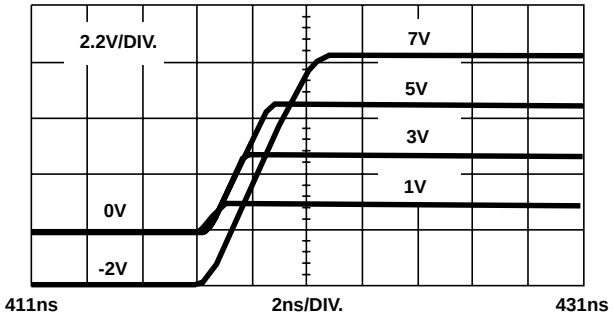



FIGURE 3. OUTPUT RESPONSE WITH VARIOUS $V_{LOW}$ AND $V_{HIGH}$ CONDITIONS

The DATA/$\overline{DATA}$ differential stage is not a factor for the speed if its current sources have enough current not to bottleneck the transient. However it should be noted that the propagation delay mismatch is determined by this stage. Sufficient current is allocated to the differential stage current sources to best match the low-to-high and high-to-low transient propagation delays.

Figure 3 shows various output responses, 0V to 1V, 0V to 3V, 0V to 5V, and -2V to 7V (full swing). The load condition is a 16 inch 50Ω SMA cable with a 5pF capacitor at the end of the cable. The rise/fall time with $5V_{P-P}$ is typically 1.45ns for the HFA5251. Pin drivers, built out of the same circuit structure as shown in Figure 2, can be made faster by trimming for a higher power supply current. Currently the pin driver has rise/fall times of less than 1ns (10% to 90% of $5V_{P-P}$) when $I_{CC}$ is trimmed to 125mA. Further speed enhancement will be made if there is a market demand.

## Basic ATE System Application

Figure 3 shows a pin driver in a typical per-pin ATE system. The pin driver works closely with the dual-level comparator and the active load. When the DUT pin acts as an input waiting for a series of digital signals, the pin driver becomes active with a logic “0” applied on the HiZ pin and provides the DUT pin with digital signals. When the DUT pin acts as an output, the pin driver output will be in high impedance mode (HiZ) with a logic “1” applied to the “HiZ” pin of the pin driver. During this high impedance mode the pin driver presents a capacitance of less than 5pF to the DUT. Special care has to be taken to match the impedance (to 50Ω) at the pin driver output to minimize reflections.

The dual level comparator detects the logic levels of the DUT pin when it acts as an output. The comparator has two threshold level inputs, VCH and VCL. The logic level information of DUT pin output is sent to the edge/window comparator through the dual level comparator. The edge/window comparator interprets this information in terms of corresponding transient performance in conjunction with the timing information. Thus it detects any possible failure transients.

The formatter sends a sequence of digital information to the pin driver which contains logic information over time. The active load is enabled when the DUT pin acts as an output. It simulates the load of the DUT pin by sinking or sourcing programmed current. Finally the sequencer controls the overall activities of the automatic testing.

## *Decoupling Circuit for Oscillation-Free Operation*

To insure the oscillation-free operation in ATE or pulse generator applications, the pin driver needs an appropriate decoupling circuit on a printed circuit board which consists of chip capacitors and chip resistors. Figures 5 and 6 refer to a proven decoupling circuit currently working in the lab and a 1X scale film of its associated PC board (metal level).

The control pins, DATA, $\overline{\text{DATA}}$, HiZ, and $\overline{\text{HiZ}}$ are fed ECL signals through 50Ω micro-strip lines terminated with 50Ω for impedance matching since the input impedance at these pins is much higher than 50Ω. At the end of the micro-strip lines there is usually a high-speed pulse generator with an output impedance of 50Ω. A 50Ω micro-strip line is connected to each of the pins, $\overline{\text{DATA}}$ and $\overline{\text{HiZ}}$ through a 50Ω chip resistor to monitor the pulse signals.

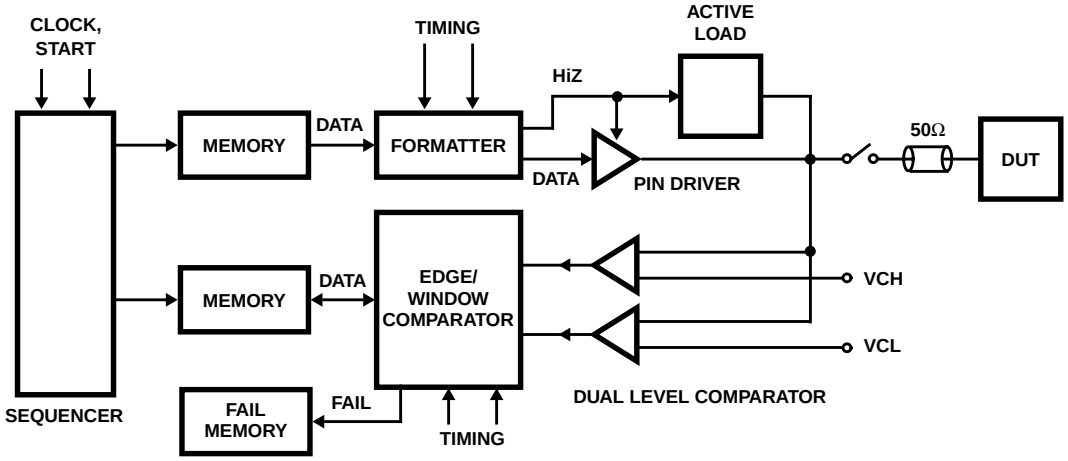



**FIGURE 4. TYPICAL ATE SYSTEM**

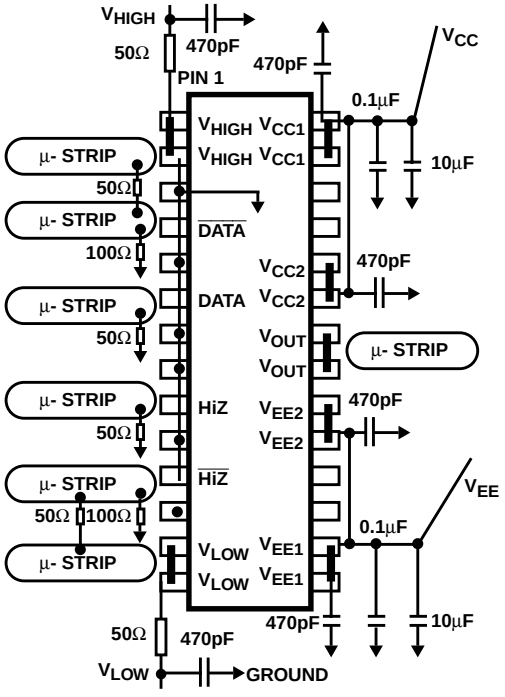



**FIGURE 5. DECOUPLING CIRCUIT OF 28 PIN SOIC HFA5251 FOR OSCILLATION-FREE OPERATION**

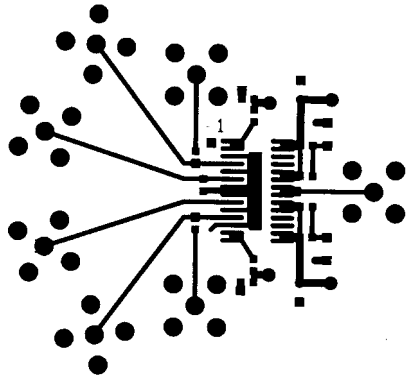


**FIGURE 6. 1X FILM OF THE EVALUATION BOARD METAL**

The two input voltage pins, $V_{HIGH}$ and $V_{LOW}$, need to be protected from any capacitively coupled AC noise. Normally this protection can be achieved by having a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this protection circuit the pin driver may oscillate due to signals fed back from the output through the PC board ground.

The power supply pins, $V_{CC1}$, $V_{CC2}$, $V_{EE1}$, and $V_{EE2}$, require decoupling chip capacitors of 470pF, 0.1μF, 10μF. Having decoupling capacitors close to $V_{CC2}$ and $V_{EE2}$ is

essential since large AC current will flow through either $V_{CC2}$ or $V_{EE2}$ during transients.

The output of the pin driver is usually connected to the device-under-test (DUT) through 50Ω micro-strip line and coaxial cable which carries the signal to a high input impedance DUT pin.

## References


1. Chris K. Davis et. al., “UHF1: A High Speed Complementary Bipolar Analog Process on SOI,” Bipolar Circuits and Technology Meeting Proceedings, pp260-263, October 1992.

2. Donald K. Whitney Jr., “Symmetrical, High Speed, Voltage Switching Circuit,” United States Patent Pending, Filed November 1991.


## Definition of Terms

### $V_{OH}$ and $V_{OL}$

Output High Voltage and Output Low Voltage. $V_{OH}$ is the voltage at $V_{OUT}$ when the HiZ input is Low and the DATA input is High. $V_{OL}$ is the voltage at $V_{OUT}$ when HiZ is Low and DATA is Low. The $V_{OH}$ and $V_{OL}$ levels are set with the $V_{HIGH}$ and $V_{LOW}$ inputs respectively.

### Offset Voltage

Offset Voltage is the DC error between the voltage placed on $V_{HIGH}$ or $V_{LOW}$ and the resulting $V_{OH}$ and $V_{OL}$. $V_{HIGH}$ Offset Voltage Error is obtained by measuring $V_{OH}$ with $V_{HIGH}$ set to 0V and $V_{LOW}$ set to -2.5V to minimize interaction effects. $V_{LOW}$ Offset Voltage Error is the measurement of $V_{OL}$ with $V_{LOW}$ set to 0V and $V_{HIGH}$ set to +7.5V.

### Gain

Gain is defined as the ratio of output voltage change to input voltage change for a defined range. $V_{HIGH}$ Gain is calculated with the following equation with $V_{LOW}$ fixed at -2.5V

$$V_{HIGH}GAIN = \frac{V_{OH}(V_{HIGH}\text{ at }6.5V) - V_{OH}(V_{HIGH}\text{ at }-1V)}{7.5}$$

$V_{LOW}$ Gain is calculated in a similar manner.

$$V_{LOW}GAIN = \frac{V_{OL}(V_{LOW}\text{ at }6V) - V_{OL}(V_{LOW}\text{ at }-1.5V)}{7.5}$$

$V_{HIGH}$ is held fixed at 7.5V. These Gain calculations minimize the effects of Interaction and End Point Nonlinearities.

### Linearity Error

Linearity Error is a measure of output voltage worst case deviation from a straight line that has been corrected for offset and 7.5V Gain. Linearity Error is given as a percentage of fullscale and is done in two ranges 5V and 8.5V. Data is measured at 0.5V steps from -1.5V to 7V for $V_{HIGH}$ and -2V to 6.5V for $V_{LOW}$. The Linearity Error equation is as follows for 8.5V fullscale:

$$V_{OUT}(IDEAL) = \frac{V_{OUT}}{GAIN} - OFFSET$$

$$LINEARITYERROR = \frac{V_{OUT} - V_{OUT}(IDEAL)}{8.5}$$

The Linearity Error equation is as follows for 5V fullscale:

$$LINEARITY\ ERROR = \frac{V_{OUT} - V_{OUT}(IDEAL)}{5}$$

Linearity Error is calculated for every data point in the range and the worst case value is recorded.

### End Point Deviation

End Point Deviation is the percent change of gain in the 1V range at the extremes of output voltage. Gain is calculated for each 0.5V step and then compared to the adjacent step for a percentage change. This specification is designed to quantify the amount of curvature present at the end points of output swing. $V_{HIGH}$ and $V_{LOW}$ inputs are corrected for gain and offset to provide more accurate $V_{OH}$ and $V_{OL}$ levels. For example $V_{OH}$ End Point Deviation is tested in the range 5.7V to 6.7V as shown below:

$$GAIN_{6.7-6.2} = \frac{V_{OH}(V_{HIGH}\text{ at }6.7V) - V_{OH}(V_{HIGH}\text{ at }6.2V)}{0.5}$$

$$GAIN_{6.2-5.7} = \frac{V_{OH}(V_{HIGH}\text{ at }6.2V) - V_{OH}(V_{HIGH}\text{ at }5.7V)}{0.5}$$

$$END\ POINT\ DEVIATION = \left|GAIN_{6.7-6.2} - GAIN_{6.2-5.7}\right| \times 100$$

### End Point Gain Error

End Point Gain Error (EPGE) is the $V_{OUT}$ absolute error in millivolts for a $V_{HIGH}$ change from 6.7V to 7V. The $V_{HIGH}$ input is corrected for gain and offset to provide a more accurate $V_{OH}$ level.

EPGE = $V_{OH}$ ($V_{HIGH}$ at 7V) - $V_{OH}$ ($V_{HIGH}$ at 6.7V) - 0.3

### $V_{HIGH}$ to $V_{LOW}$ Interaction

$V_{HIGH}$ to $V_{LOW}$ Interaction is the change in $V_{OUT}$ (the active channel) due to the inactive channel. $V_{HIGH}$ Interaction is measured as the change in $V_{OH}$ from 1V as $V_{LOW}$ is moved from 0V to 750mV ($V_{LOW}$ is corrected for gain and offset errors). $V_{LOW}$ Interaction is measured as the change in $V_{OL}$ from 0V as $V_{HIGH}$ is moved from 1V to 250mV (with $V_{HIGH}$ corrected for gain and offset errors). The minimum recommended difference between $V_{HIGH}$ and $V_{LOW}$ for the HFA5251 is 250mV.

## Typical Performance Curves

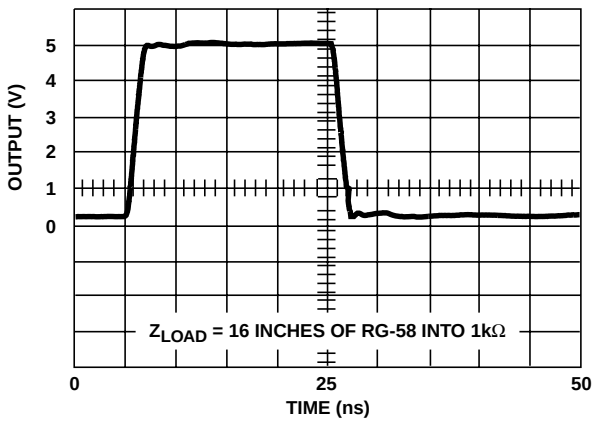



FIGURE 7. LARGE SIGNAL RESPONSE

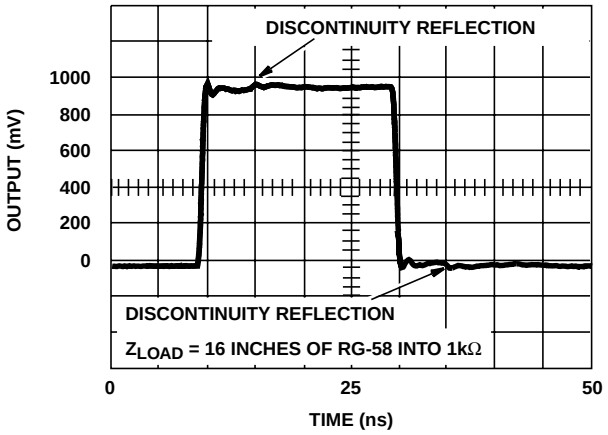



FIGURE 8. SMALL SIGNAL RESPONSE

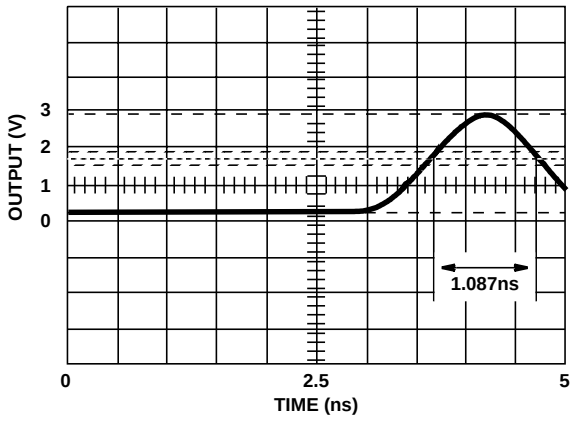



FIGURE 9. MINIMUM PULSE WIDTH

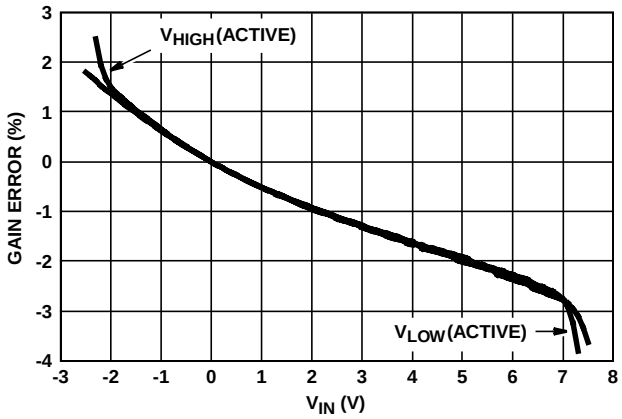



FIGURE 10. GAIN ERROR (FULLSCALE = 8.5V)

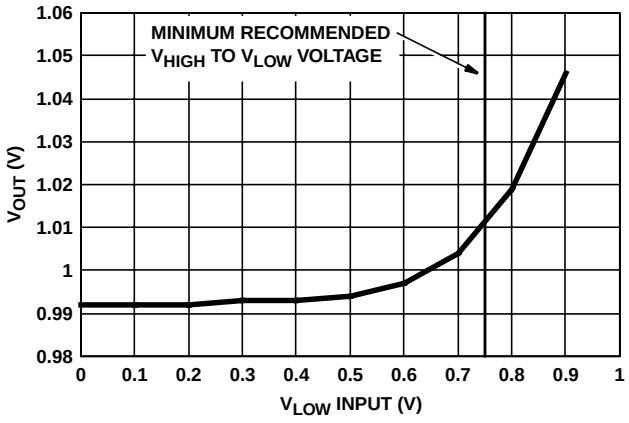



FIGURE 11. $V_{HIGH}/V_{LOW}$ INTERACTION, $V_{HIGH}$ ACTIVE (NOMINAL 1.0V)

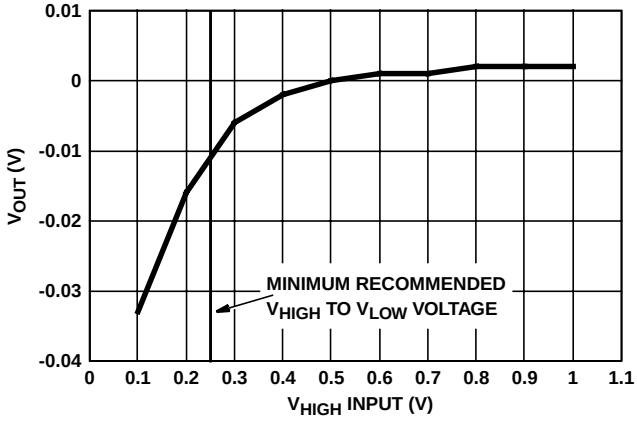



FIGURE 12. $V_{HIGH}/V_{LOW}$ INTERACTION, $V_{LOW}$ ACTIVE (NOMINAL 0.0V)

## Die Characteristics

**DIE DIMENSIONS:**

2670µm x 1730µm x 525µm

**METALLIZATION:**

Type: Metal 1: Cu (2%) SiAl/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Backside: Gold

Type: Metal 2: Cu (2%) Al

Thickness: Metal 2: 16kÅ ±0.8kÅ

**PASSIVATION:**

Nitride, 4kÅ ±0.5kÅ

**TRANSISTOR COUNT:**

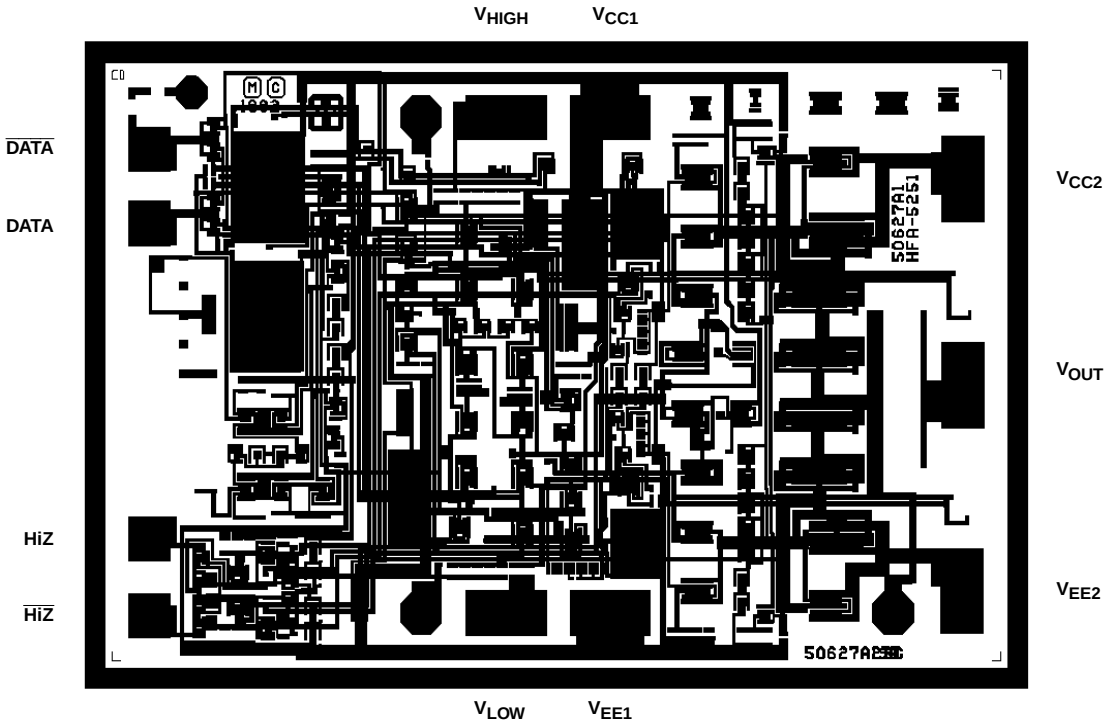
115

**SUBSTRATE POTENTIAL:**

Floating

## Metallization Mask Layout

**HFA5251**

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