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File Number 3126.2

### CMOS Analog Switches

The HI-381 thru HI-387 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

### Features

- Analog Signal Range ( $\pm 15V$  Supplies) . . . . .  $\pm 15V$
- Low Leakage . . . . .  $40pA$
- Low On Resistance . . . . .  $35\Omega$
- Break-Before-Make Delay . . . . .  $60ns$
- Charge Injection . . . . .  $30pC$
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power . . . . .  $1.0mW$

### Applications

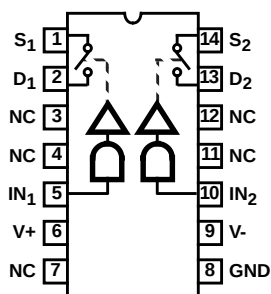
- Sample and Hold (i.e., Low Leakage Switching)
- Op Amp Gain Switching (i.e., Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

### Pinouts (Switch States are for a Logic "1" Input)

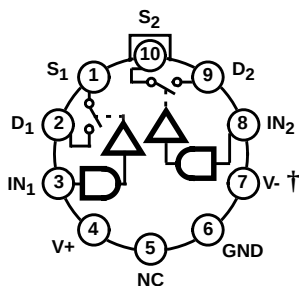
**DUAL SPST HI-381**

TOP VIEWS

(CERDIP, PDIP)



(METAL CAN)

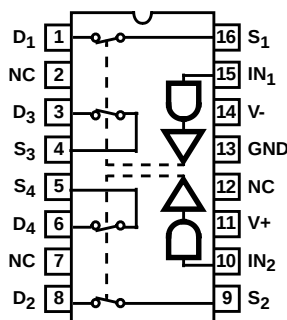


† The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

| LOGIC | SWITCH |
|-------|--------|
| 0     | ON     |
| 1     | OFF    |

**DUAL DPST HI-384 (CERDIP, PDIP)**

TOP VIEW

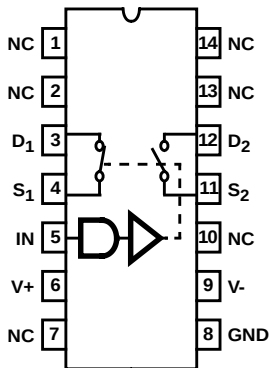


| LOGIC | SW 1 - 4 |
|-------|----------|
| 0     | OFF      |
| 1     | ON       |

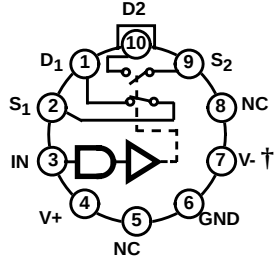
**Pinouts** (Switch States are for a Logic "1" Input) (Continued)

SPDT HI-387  
TOP VIEWS

(CERDIP, PDIP)



(METAL CAN)



† The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

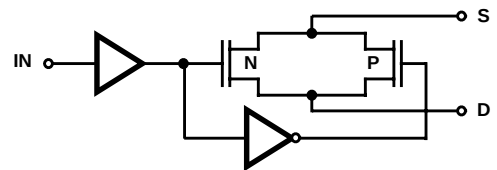
| LOGIC | SW1 | SW2 |
|-------|-----|-----|
| 0     | OFF | ON  |
| 1     | ON  | OFF |

**Part Number Information**

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE          | PKG. NO. |
|-------------|------------------|------------------|----------|
| HI1-0381-2  | -55 to 125       | 14 Ld CERDIP     | F14.3    |
| HI1-0381-5  | 0 to 75          | 14 Ld CERDIP     | F14.3    |
| HI2-0381-2  | -55 to 125       | 10 Pin Metal Can | T10.B    |
| HI2-0381-5  | 0 to 75          | 10 Pin Metal Can | T10.B    |
| HI3-0381-5  | 0 to 75          | 14 Ld PDIP       | E14.3    |
| HI1-0384-2  | -55 to 125       | 16 Ld CERDIP     | F16.3    |
| HI1-0384-5  | 0 to 75          | 16 Ld CERDIP     | F16.3    |
| HI3-0384-5  | 0 to 75          | 16 Ld PDIP       | E16.3    |
| HI1-0387-2  | -55 to 125       | 14 Ld CERDIP     | F14.3    |
| HI1-0387-5  | 0 to 75          | 14 Ld CERDIP     | F14.3    |
| HI2-0387-2  | -55 to 125       | 10 Pin Metal Can | T10.B    |
| HI2-0387-5  | 0 to 75          | 10 Pin Metal Can | T10.B    |
| HI3-0387-5  | 0 to 75          | 14 Ld PDIP       | E14.3    |

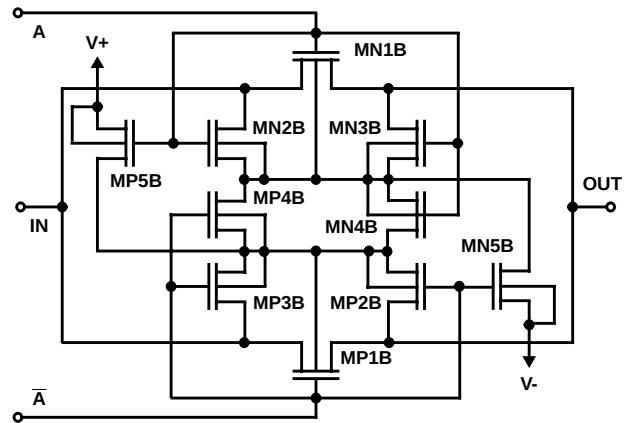
**Functional Block Diagram**

TYPICAL SWITCH SERIES

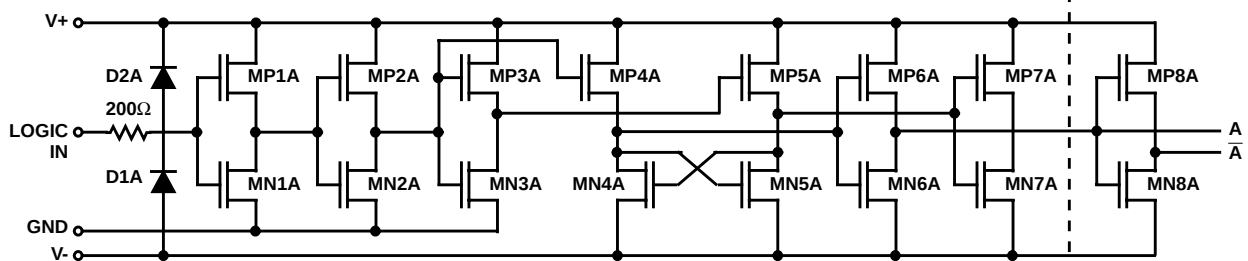


**Schematic Diagrams**

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



SWITCH CELL DRIVER  
(ONE PER SWITCH CELL)

## Absolute Maximum Ratings

|                                    |                                                          |
|------------------------------------|----------------------------------------------------------|
| Voltage Between Supplies . . . . . | 44V (±22V)                                               |
| Digital Input Voltage . . . . .    | +V <sub>SUPPLY</sub> +4V<br>-V <sub>SUPPLY</sub> -4V     |
| Analog Input Voltage . . . . .     | +V <sub>SUPPLY</sub> +1.5V<br>-V <sub>SUPPLY</sub> -1.5V |

## Operating Conditions

|                    |                |
|--------------------|----------------|
| Temperature Ranges |                |
| -2 . . . . .       | -55°C to 125°C |
| -5 . . . . .       | 0°C to 75°C    |

## Thermal Information

|                                                    |                      |                      |
|----------------------------------------------------|----------------------|----------------------|
| Thermal Resistance (Typical, Note 1)               | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
| 14 Ld CERDIP Package . . . . .                     | 95                   | 40                   |
| 16 Ld CERDIP Package . . . . .                     | 90                   | 36                   |
| PDIP Package . . . . .                             | 100                  | N/A                  |
| Metal Can Package . . . . .                        | 160                  | 75                   |
| Maximum Junction Temperature                       |                      |                      |
| Hermetic Package . . . . .                         |                      | 175°C                |
| Plastic Package . . . . .                          |                      | 150°C                |
| Maximum Storage Temperature Range . . . . .        |                      | -65°C to 150°C       |
| Maximum Lead Temperature (Soldering 10s) . . . . . |                      | 300°C                |

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

Supplies = +15V, -15V; V<sub>IN</sub> = Logic Input. V<sub>IN</sub> for Logic "1" = 4V, for Logic "0" = 0.8V,  
Unless Otherwise Specified

| PARAMETER                                                   | TEST CONDITIONS | TEMP<br>(°C) | -2  |      |     | -5  |      |     | UNITS |
|-------------------------------------------------------------|-----------------|--------------|-----|------|-----|-----|------|-----|-------|
|                                                             |                 |              | MIN | TYP  | MAX | MIN | TYP  | MAX |       |
| SWITCHING CHARACTERISTICS                                   |                 |              |     |      |     |     |      |     |       |
| Break-Before-Make Delay, t <sub>OPEN</sub><br>(HI-387 Only) |                 | 25           | -   | 60   | -   | -   | 60   | -   | ns    |
| Switch On Time, t <sub>ON</sub>                             |                 | 25           | -   | 210  | 300 | -   | 210  | 300 | ns    |
| Switch Off Time, t <sub>OFF</sub>                           |                 | 25           | -   | 160  | 250 | -   | 160  | 250 | ns    |
| “Off Isolation”                                             | (Note 5)        | 25           | -   | 60   | -   | -   | 60   | -   | dB    |
| Charge Injection                                            | (Note 6)        | 25           | -   | 3    | -   | -   | 3    | -   | mV    |
| Input Switch Capacitance, C <sub>S(OFF)</sub>               |                 | 25           | -   | 16   | -   | -   | 16   | -   | pF    |
| Output Switch Capacitance, C <sub>D(OFF)</sub>              |                 | 25           | -   | 14   | -   | -   | 14   | -   | pF    |
| Output Switch Capacitance, C <sub>D(ON)</sub>               |                 | 25           | -   | 35   | -   | -   | 35   | -   | pF    |
| Digital Input Capacitance (High), C <sub>IN</sub>           |                 | 25           | -   | 5    | -   | -   | 5    | -   | pF    |
| Digital Input Capacitance (Low), C <sub>IN</sub>            |                 | 25           | -   | 5    | -   | -   | 5    | -   | pF    |
| DIGITAL INPUT CHARACTERISTICS                               |                 |              |     |      |     |     |      |     |       |
| Input Low Level, V <sub>IL</sub>                            |                 | Full         | -   | -    | 0.8 | -   | -    | 0.8 | V     |
| Input High Level, V <sub>IH</sub>                           |                 | Full         | 4   | -    | -   | 4   | -    | -   | V     |
| Input Leakage Current (Low), I <sub>IL</sub>                | (Note 4)        | Full         | -   | -    | 1   | -   | -    | 1   | μA    |
| Input Leakage Current (High), I <sub>IH</sub>               | (Note 4)        | Full         | -   | -    | 1   | -   | -    | 1   | μA    |
| ANALOG SWITCH CHARACTERISTICS                               |                 |              |     |      |     |     |      |     |       |
| Analog Signal Range                                         |                 | Full         | -15 | -    | +15 | -15 | -    | +15 | V     |
| On Resistance, r <sub>ON</sub>                              | (Note 1)        | 25           | -   | 35   | 50  | -   | 35   | 50  | Ω     |
|                                                             |                 | Full         | -   | 40   | 75  | -   | 45   | 75  | Ω     |
| Off Input Leakage Current, I <sub>S(OFF)</sub>              | (Note 2)        | 25           | -   | 0.04 | 1   | -   | 0.04 | 5   | nA    |
|                                                             |                 | Full         | -   | 1    | 100 | -   | 0.2  | 100 | nA    |
| Off Output Leakage Current, I <sub>D(OFF)</sub>             | (Note 2)        | 25           | -   | 0.04 | 1   | -   | 0.04 | 5   | nA    |
|                                                             |                 | Full         | -   | 1    | 100 | -   | 0.2  | 100 | nA    |

**Electrical Specifications** Supplies = +15V, -15V;  $V_{IN}$  = Logic Input.  $V_{IN}$  for Logic "1" = 4V, for Logic "0" = 0.8V, Unless Otherwise Specified (Continued)

| PARAMETER                             | TEST CONDITIONS | TEMP<br>(°C) | -2  |      |     | -5  |      |     | UNITS   |
|---------------------------------------|-----------------|--------------|-----|------|-----|-----|------|-----|---------|
|                                       |                 |              | MIN | TYP  | MAX | MIN | TYP  | MAX |         |
| On Input Leakage Current, $I_{S(ON)}$ | (Note 3)        | 25           | -   | 0.03 | 1   | -   | 0.03 | 5   | nA      |
|                                       |                 | Full         | -   | 0.5  | 100 | -   | 0.2  | 100 | nA      |
| <b>POWER SUPPLY CHARACTERISTICS</b>   |                 |              |     |      |     |     |      |     |         |
| Current, $I_+$                        | (Note 7)        | 25           | -   | 0.09 | 0.5 | -   | 0.09 | 0.5 | mA      |
|                                       |                 | Full         | -   | -    | 1   | -   | -    | 1   | mA      |
| Current, $I_-$                        | (Note 7)        | 25           | -   | 0.01 | 10  | -   | 0.01 | 100 | $\mu$ A |
|                                       |                 | Full         | -   | -    | 100 | -   | -    | -   | $\mu$ A |
| Current, $I_+$                        | (Note 8)        | 25           | -   | 0.01 | 10  | -   | 0.01 | 100 | $\mu$ A |
|                                       |                 | Full         | -   | -    | 100 | -   | -    | -   | $\mu$ A |
| Current, $I_-$                        | (Note 8)        | 25           | -   | 0.01 | 10  | -   | 0.01 | 100 | $\mu$ A |
|                                       |                 | Full         | -   | -    | 100 | -   | -    | -   | $\mu$ A |

**NOTES:**

- $V_S = \pm 10V$ ,  $I_{OUT} = \pm 10mA$ . On resistance derived from the voltage measured across the switch under the above conditions.
- $V_S = \pm 14V$ ,  $V_D = \pm 14V$ .
- $V_S = V_D = \pm 14V$ .
- The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
- $V_S = 1V_{RMS}$ ,  $f = 500kHz$ ,  $C_L = 15pF$ ,  $R_L = 1K$ ,  $C_L = C_{FIXTURE} + C_{PROBE}$  "off isolation" = 20 Log  $V_S/V_D$ .
- $V_S = 0V$ ,  $C_L = 10nF$ , Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
- $V_{IN} = 4V$  (one input) (all other inputs = 0V).
- $V_{IN} = 0.8V$  (all inputs).

**Typical Performance Curves**

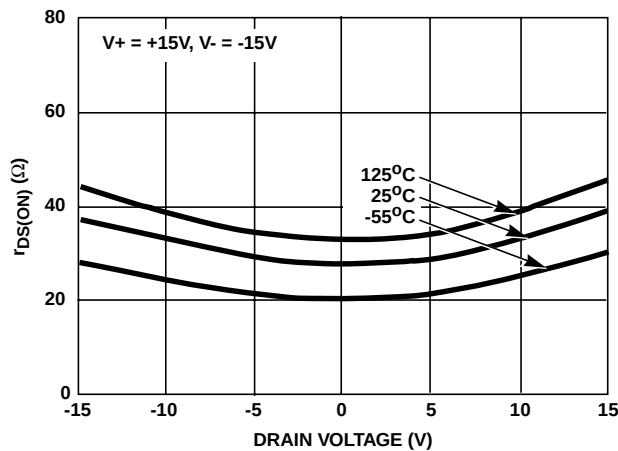


FIGURE 1.  $r_{DS(ON)}$  vs  $V_D$  AND TEMPERATURE

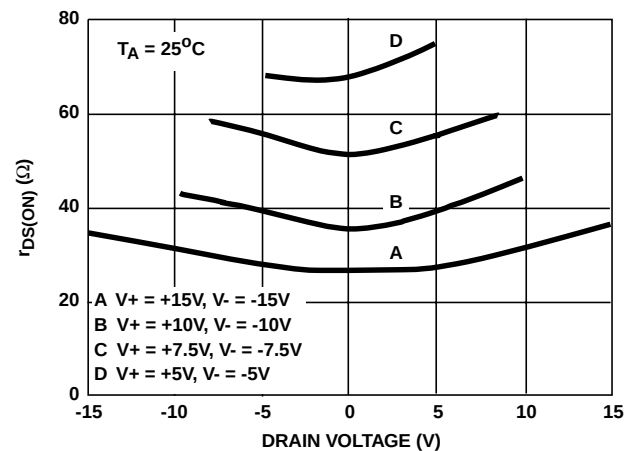


FIGURE 2.  $r_{DS(ON)}$  vs  $V_D$  AND POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

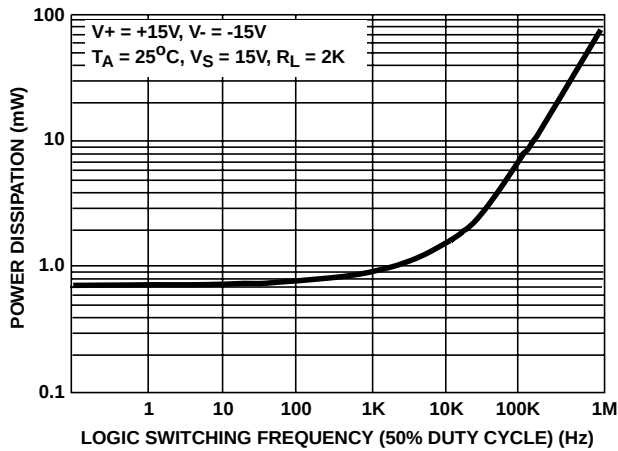


FIGURE 3. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY (SINGLE LOGIC INPUT)

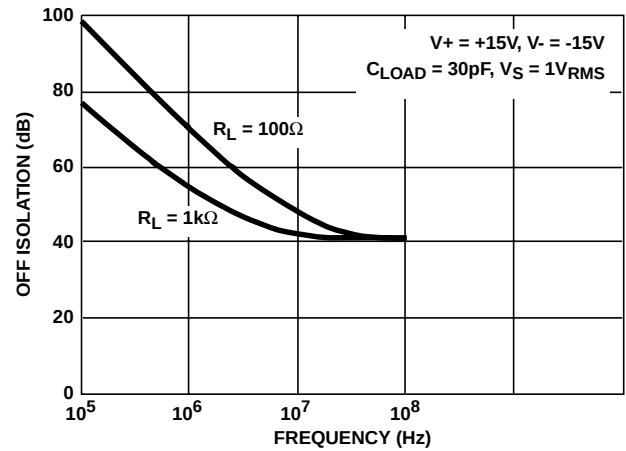


FIGURE 4. OFF ISOLATION vs FREQUENCY

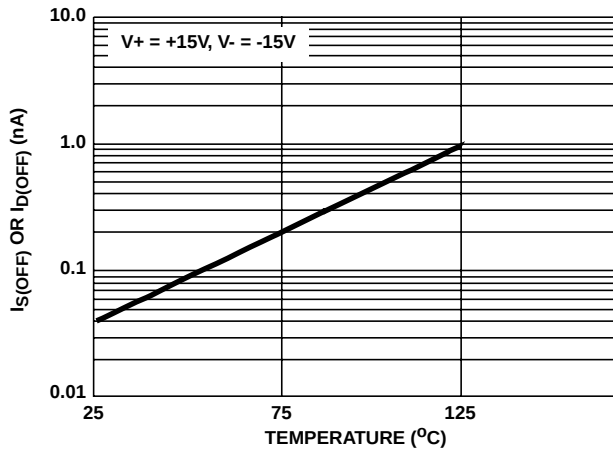


FIGURE 5.  $I_{S(OFF)}$  OR  $I_{D(OFF)}$  vs TEMPERATURE (NOTE)

NOTE: The net leakage into the source or drain is the N-Channel leakage minus the P-Channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

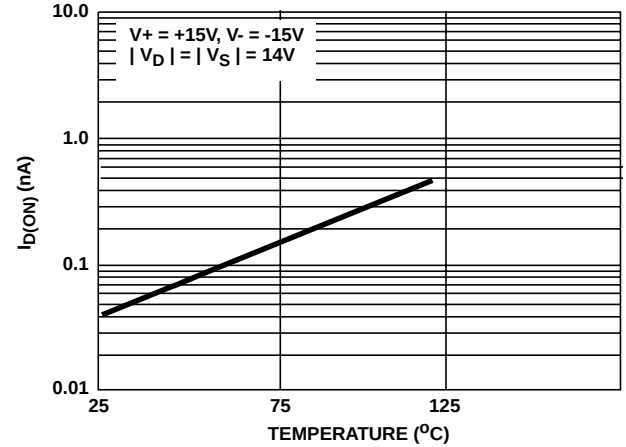


FIGURE 6.  $I_{D(ON)}$  vs TEMPERATURE (NOTE)

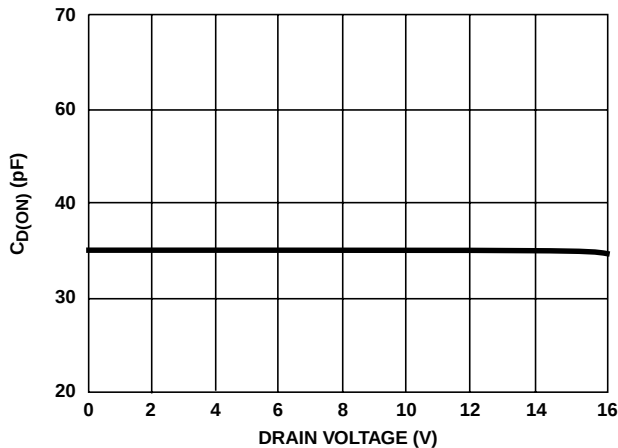


FIGURE 7. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

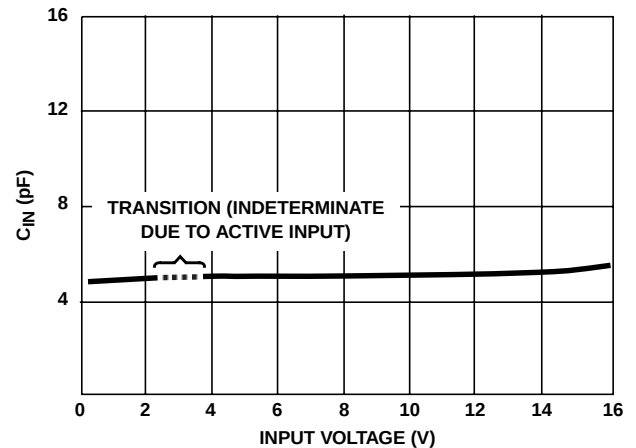


FIGURE 8. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

Typical Performance Curves (Continued)

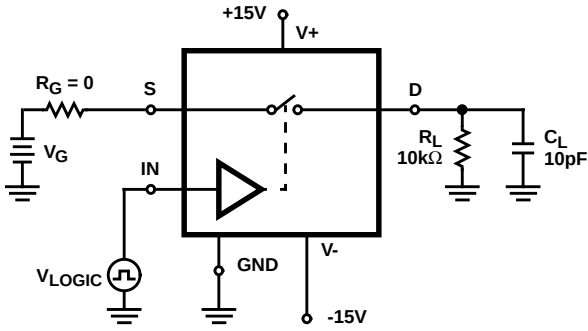


FIGURE 9A. TEST CIRCUIT

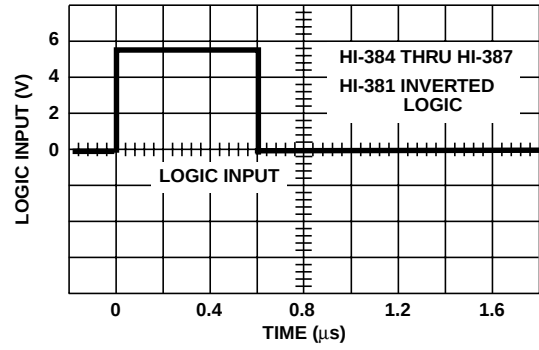


FIGURE 9B.  $V_{IN}$  LOGIC vs TIME

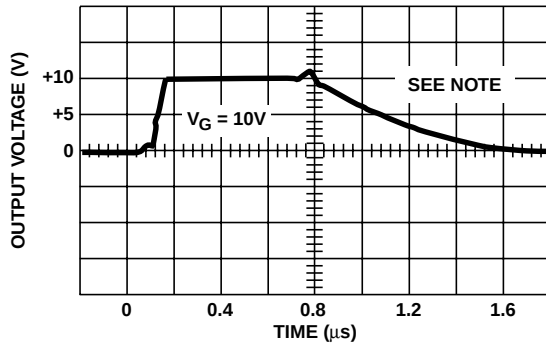


FIGURE 9C.  $V_{OUT}$  vs TIME

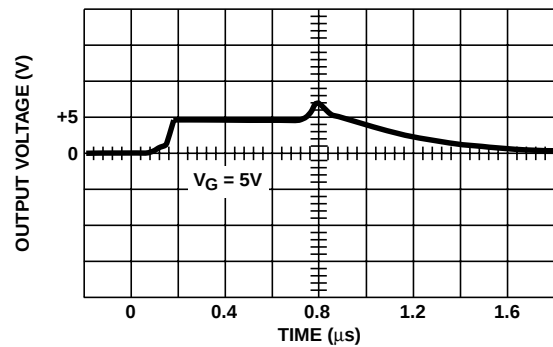


FIGURE 9D.  $V_{OUT}$  vs TIME

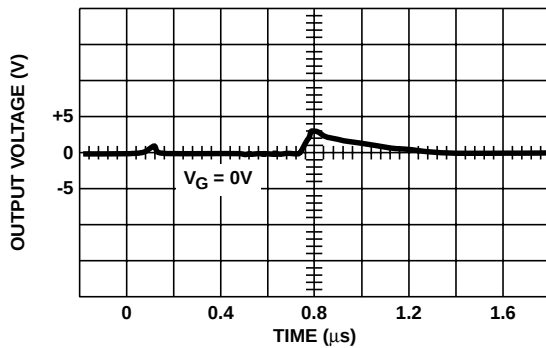


FIGURE 9E.  $V_{OUT}$  vs TIME

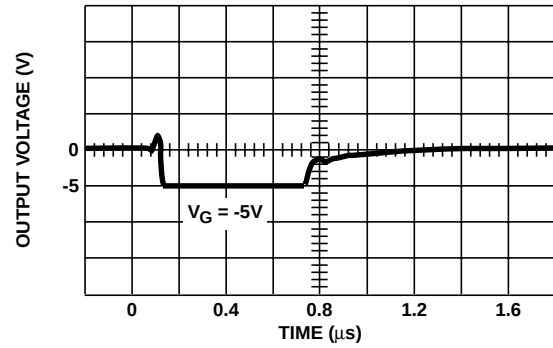


FIGURE 9F.  $V_{OUT}$  vs TIME

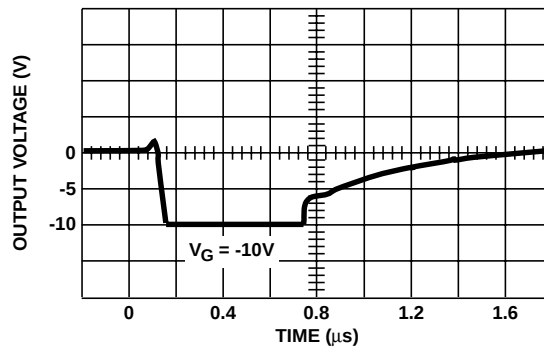


FIGURE 9G.  $V_{OUT}$  vs TIME

NOTE: If  $R_G$ ,  $R_L$  or  $C_L$  is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 9. TYPICAL DELAY, RISE, FALL, SETTLING TIMES AND SWITCHING TRANSIENTS

## Typical Performance Curves (Continued)

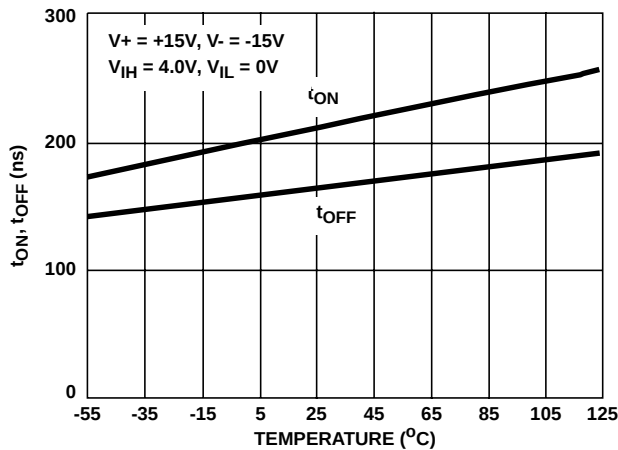


FIGURE 10. SWITCHING TIME vs TEMPERATURE

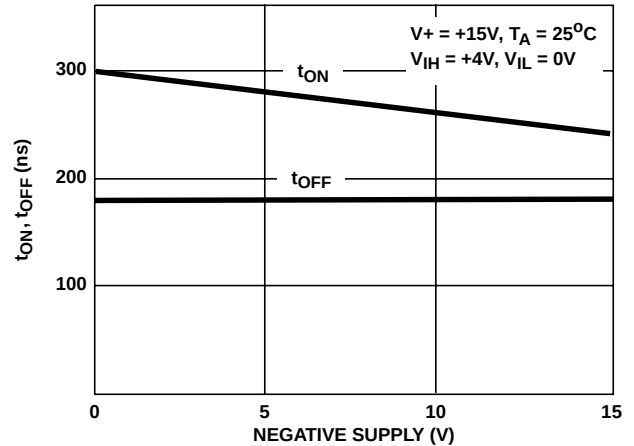


FIGURE 11. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

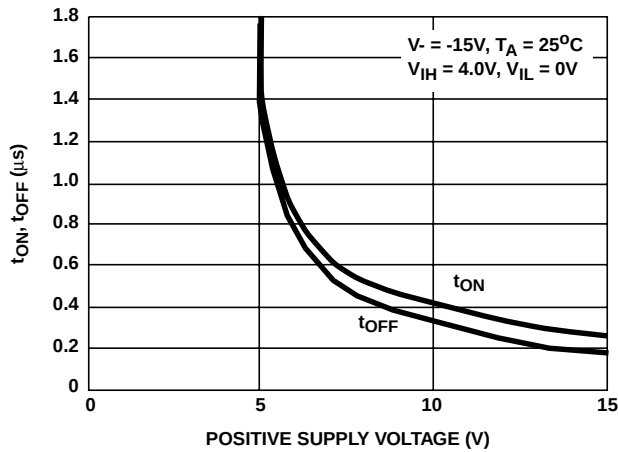


FIGURE 12. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

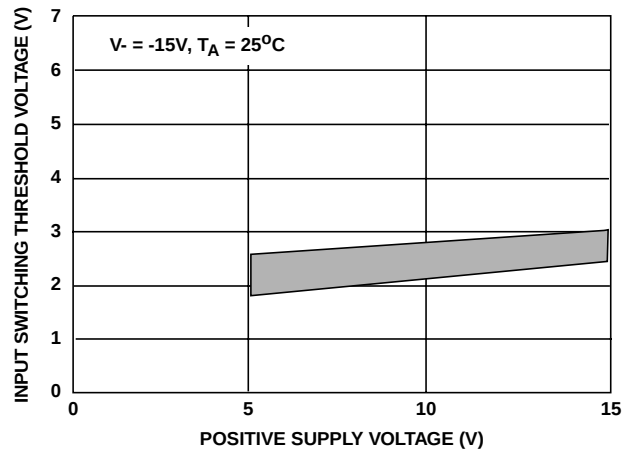


FIGURE 13. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE

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