HM-6508

March 1997

1024 x 1 CMOS RAM

Features

- **Low Power Standby . . . . . 50μW Max**
- **Low Power Operation . . . . . 20mW/MHz Max**
- **Fast Access Time. . . . . .180ns Max**
- **Data Retention . . . . . .2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 2 TTL Loads**
- **On-Chip Address Register**

Description

The HM-6508 is a 1024 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On-Chip latches are provided for address, allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

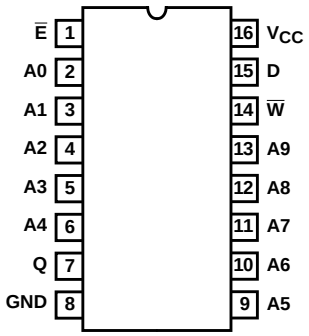
The HM-6508 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	180ns	250ns	PKG. NO.
PDIP	-40°C to +85°C	HM3-6508B-9	HM3-6508-9	E16.3
CERDIP	-40°C to +85°C	HM1-6508B-9	HM1-6508-9	F16.3

Pinout

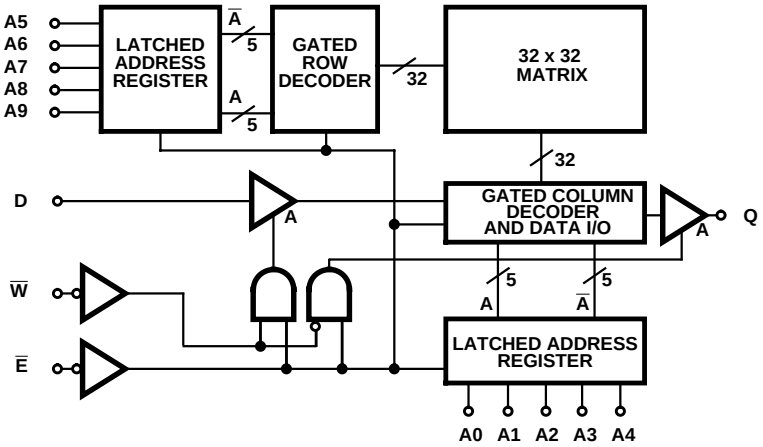
HM-6508
(PDIP, CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

File Number **2984.1**

Functional Diagram



NOTES:

1. All lines positive logic - active high.
2. Three-state buffers: A high $\rightarrow$ output active.
3. Address latches and gated decoders: latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 1.5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
HM-6508B-9, HM-6508-9 . . . . . -40^oC to $+85^oC$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}	θ_{JC}
PDIP Package	$90^oC/W$	N/A
CERDIP Package	$75^oC/W$	$15^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature . . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 1925 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40^oC to $+85^oC$ (HM-6508B-9, HM-6508-9)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		-	10	µA	IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.0V
ICCOP	Operating Supply Current (Note 1)		-	4	mA	$\overline{E}$ = 1MHz, IO = 0mA, VI = V_{CC} or GND, V_{CC} = 5.5V
ICCDR	Data Retention Supply Current	HM-6508B-9	-	5	µA	V_{CC} = 2.0V, IO = 0mA, VI = V_{CC} or GND, $\overline{E}$ = V_{CC}
		HM-6508-9	-	10	µA	
VCCDR	Data Retention Supply Voltage		2.0	-	V	
II	Input Leakage Current		-1.0	+1.0	µA	VI = V_{CC} or GND, V_{CC} = 5.5V
IOZ	Output Leakage Current		-1.0	+1.0	µA	VO = V_{CC} or GND, V_{CC} = 5.5V
VIL	Input Low Voltage		-0.3	0.8	V	V_{CC} = 4.5V
VIH	Input High Voltage		V_{CC} -2.0	V_{CC} +0.3	V	V_{CC} = 5.5V
VOL	Output Low Voltage		-	0.4	V	IO = 3.2mA, V_{CC} = 4.5V
VOH	Output High Voltage		2.4	-	V	IO = -0.4mA, V_{CC} = 4.5V

Capacitance T_A = $+25^oC$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	f = 1MHz, All measurements are referenced to device GND
CO	Output Capacitance (Note 2)	10	pF	

NOTES:

1. Typical derating 1.5mA/MHz increase in ICCOP.
2. Tested at initial design and after major design changes 1.

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40^oC to $+85^oC$ (HM-6508B-9, HM-6508-9)

SYMBOL	PARAMETER	HM-6508B-9		HM-6508-9		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
(1) TELQV	Chip Enable Access Time	-	180	-	250	ns	(Notes 1, 3)
(2) TAVQV	Address Access Time	-	180	-	250	ns	(Notes 1, 3, 4)
(3) TELQX	Chip Enable Output Enable Time	5	120	5	160	ns	(Notes 2, 3)

AC Electrical Specifications V_{CC} = 5V ±10%; T_A = -40°C to +85°C (HM-6508B-9, HM-6508-9) **(Continued)**

SYMBOL	PARAMETER	HM-6508B-9		HM-6508-9		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
(4) TWLQZ	Write Enable Output Disable Time	-	120	-	160	ns	(Notes 2, 3)
(5) TEHQZ	Chip Enable Output Disable Time	-	120	-	160	ns	(Notes 2, 3)
(6) TELEH	Chip Enable Pulse Negative Width	180	-	250	-	ns	(Notes 1, 3)
(7) TEHEL	Chip Enable Pulse Positive Width	100	-	100	-	ns	(Notes 1, 3)
(8) TAVEL	Address Setup Time	0	-	0	-	ns	(Notes 1, 3)
(9) TELAX	Address Hold Time	40	-	50	-	ns	(Notes 1, 3)
(10) TDVWH	Data Setup Time	80	-	110	-	ns	(Notes 1, 3)
(11) TWHDX	Data Hold Time	0	-	0	-	ns	(Notes 1, 3)
(12) TWLEH	Chip Enable Write Pulse Setup Time	100	-	130	-	ns	(Notes 1, 3)
(13) TELWH	Chip Enable Write Pulse Hold Time	100	-	130	-	ns	(Notes 1, 3)
(14) TWLWH	Write Enable Pulse Width	100	-	130	-	ns	(Notes 1, 3)
(15) TELEL	Read or Write Cycle Time	280	-	350	-	ns	(Notes 1, 3)

NOTES:

1. Input pulse levels: 0.8V to V_{CC} -2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. V_{CC} = 4.5V and 5.5V.
4. TAVQV = TELQV + TAVEL.

Timing Waveforms

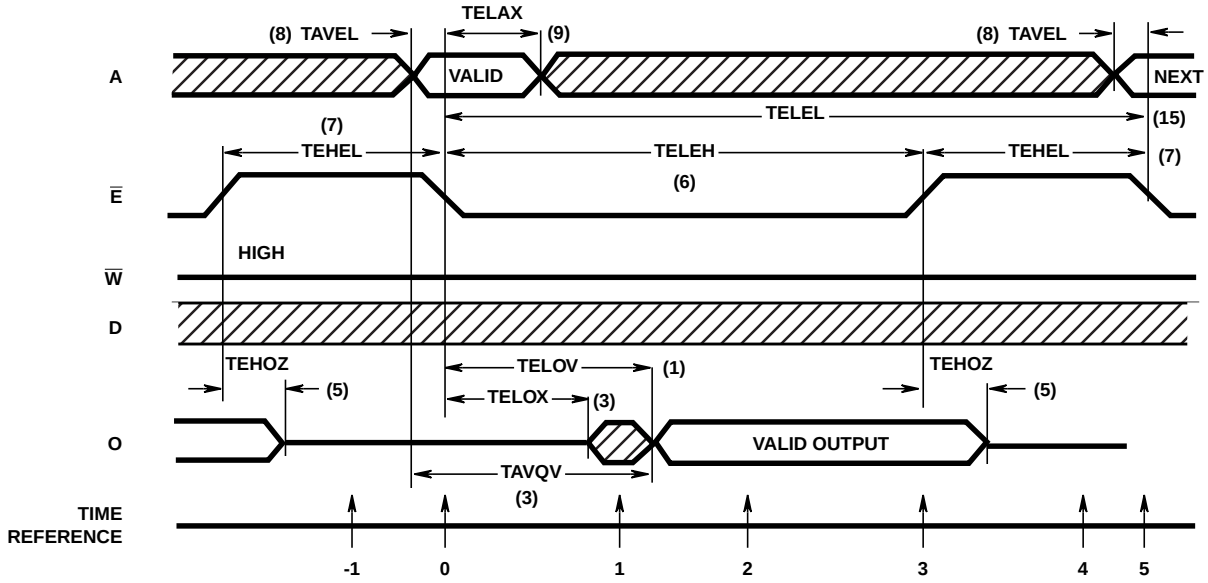


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	X	Output Enabled
2	L	H	X	X	V	Output Valid
3	↗	H	X	X	V	Read Accomplished
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

In the HM-6508 Read Cycle, the address information is latched into the On-Chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation.

During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Timing Wavforms (continued)

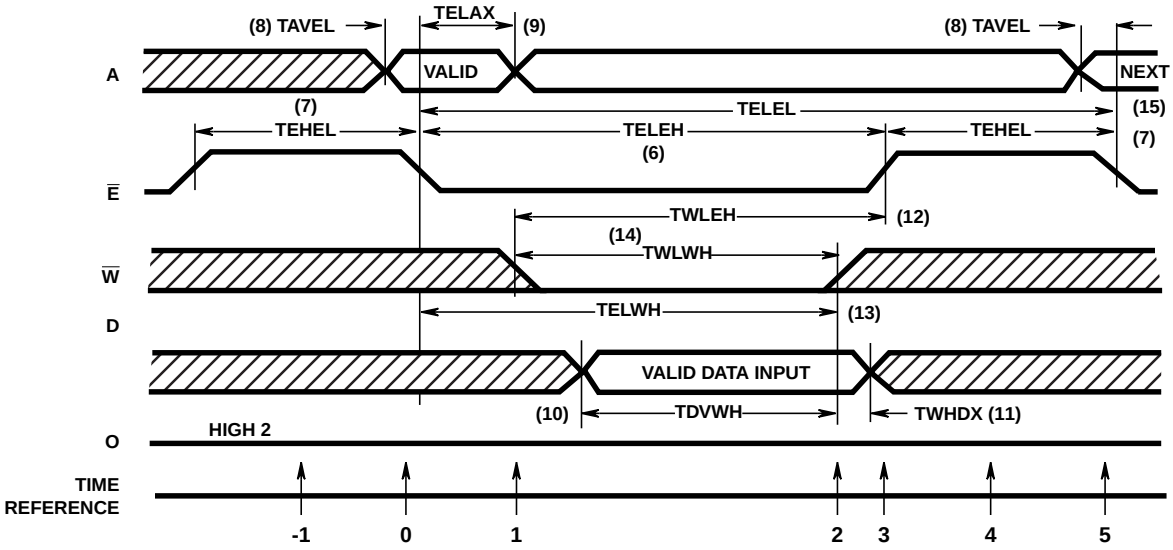


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUTS	FUNCTION
	$\overline{E}$	$\overline{W}$	A	D	Q	
-1	H	X	X	X	Z	Memory Disabled
0	↘	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↘	X	X	Z	Write Period Begins
2	L	↗	X	V	Z	Data is Written
3	↗	H	X	X	Z	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

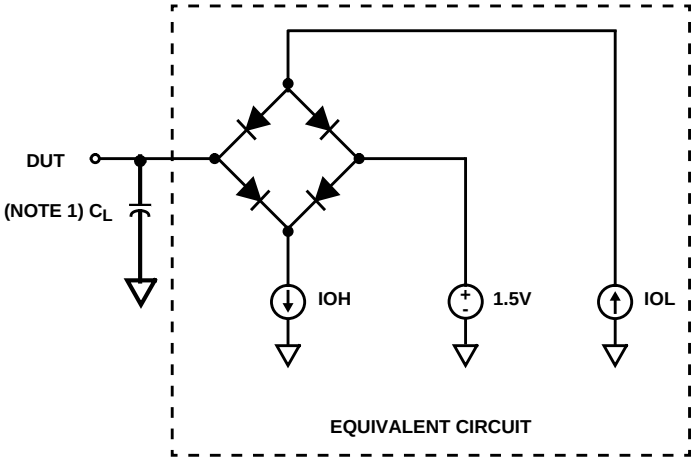
The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the On-Chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle, provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH), plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will ensure that the output buffers are not active.

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.