FM25640

64Kb FRAM Serial Memory

Features

64K bit Ferroelectric Nonvolatile RAM

- Organized as 8,192 x 8 bits
- High endurance 10 Billion (10^{10}) read/writes
- 10 year data retention at 85° C
- NoDelay™ write
- Advanced high-reliability ferroelectric process

Very Fast Serial Peripheral Interface - SPI

- Up to 5 MHz maximum bus frequency
- Direct hardware replacement for EEPROM
- SPI Mode 0 & 3 (CPOL, CPHA=0,0 & 1,1)

Sophisticated Write Protection Scheme

- Hardware protection
- Software protection

Low Power Consumption

- 10 µA standby current

Industry Standard Configuration

- Industrial temperature -40° C to +85° C
- 8-pin SOP or DIP

Description

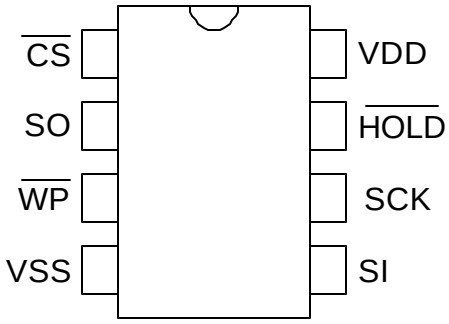
The FM25640 is a 64-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or FRAM is nonvolatile but operates in other respects as a RAM. It provides reliable data retention for 10 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

Unlike serial EEPROMs, the FM25640 performs write operations at bus speed. No write delays are incurred. Data is written to the memory array mere hundreds of nanoseconds after it has been successfully transferred to the device. The next bus cycle may commence immediately. In addition, the product offers substantial write endurance compared with other nonvolatile memories. The FM25640 is capable of supporting up to 1E10-read/write cycles -- far more than most systems will require from a serial memory.

These capabilities make the FM25640 ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss.

The FM25640 provides substantial benefits to users of serial EEPROM, in a hardware drop-in replacement. The FM25640 uses the high-speed SPI bus, which enhances the high-speed write capability of FRAM technology. It is guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration



Pin Names	Function
/CS	Chip Select
SO	Serial Data Output
/WP	Write Protect
VSS	Ground
SI	Serial Data Input
SCK	Serial Clock
/HOLD	Hold
VDD	5V

Ordering Information	
FM25640-P	8-pin plastic DIP
FM25640-S	8-pin SOP

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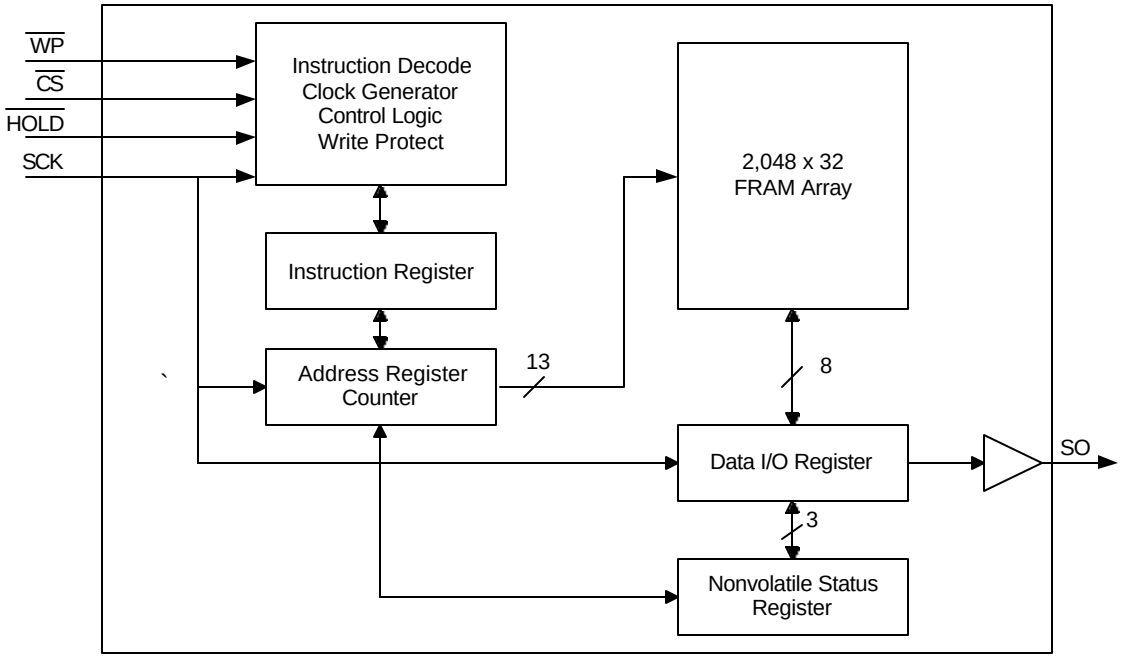
Figure 1. Block Diagram



Pin Description

Pin Name	Pin Number	I/O	Pin Description
/CS	1	I	Chip Select. Activates the device. When high, all outputs are tri-state and the device ignores other inputs. The part remains in a low-power standby mode. When low, the part recognizes activity on the SCK signal. A falling edge on /CS must occur prior to every op-code.
SO	2	O	Serial Output. SO is the data output pin. It is driven actively during a read and remains tri-state at all other times including when HOLD\ is low. Data transitions are driven on the falling edge of the serial clock. * SO can be connected to SI for a single pin data interface since the part communicates in half-duplex.
/WP	3	I	Write Protect. This pin prevents write operations to the status register. This is critical since other write protection features are controlled through the status register. A complete explanation of write protection is provided below. *Note that the function of /WP is different from the FM25040 where it prevents all writes to the part.
VSS	4	I	Ground
SI	5	I	Serial Input. All data is input to the device on this pin. The pin is sampled on the rising edge of SCK and is ignored at other times. It should always be driven to a valid logic level to meet IDD specifications. * SI may be connected to SO for a single pin data interface.
SCK	6	I	Serial Clock. All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. The part is static so the clock frequency may be any value between 0 and 5 MHz and may be interrupted at any time.
/HOLD	7	I	Hold. The /HOLD signal is used when the host CPU must interrupt a memory operation for another task. Taking the /HOLD signal to a low state pauses the current operation. The part ignores any transition on SCK or /CS. All transitions on /HOLD must occur while SCK is low.
VDD	8	I	Supply Voltage. 5V

Overview

The FM25640 is a serial FRAM memory. The memory array is logically organized as 8,192 x 8 and is accessed using an industry standard Serial Peripheral Interface or SPI bus. Functional operation of the FRAM is similar to serial EEPROMs. The major difference between the FM25640 and a serial EEPROM with the same pin-out relates to its superior write performance.

Memory Architecture

When accessing the FM25640, the user addresses 8,192 locations each with 8 data bits. These data bits are shifted serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an op-code and a two-byte address. The upper 3 bits of the address range are 'don't care' values. The complete address of 13-bits specifies each byte address uniquely.

Most functions of the FM25640 either are controlled by the SPI interface or are handled automatically by on-board circuitry. The access time for memory operation essentially is zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. That is, by the time a new bus transaction can be shifted into the part, a write operation will be complete. This is explained in more detail in the interface section below.

Users expect several obvious system benefits from the FM25640 due to its fast write cycle and high endurance as compared with EEPROM. However there are less obvious benefits as well. For example in a high noise environment, the fast-write operation is less susceptible to corruption than an EEPROM since it is completed quickly. By contrast, an EEPROM requiring milliseconds to write is vulnerable to noise during much of the cycle.

Note that the FM25640 contains no power management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that VDD is within data sheet tolerances to prevent incorrect operation.

Serial Peripheral Interface – SPI Bus

The FM25640 employs a Serial Peripheral Interface (SPI) bus. It is specified to operate at speeds up to 5 MHz. This high-speed serial bus provides high performance serial communication to a host microcontroller. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM25640 operates in SPI Mode 0 and 3.

The SPI interface uses a total of four pins: clock, data-in, data-out, and chip select. It is possible to connect the two data lines together. Figure 2 illustrates a typical system configuration using the FM25640 with a microcontroller that offers an SPI port. Figure 3 shows a similar configuration for a microcontroller that has no hardware support for the SPI bus.

Protocol Overview

The SPI interface is a synchronous serial interface using clock and data lines. It is intended to support multiple devices on the bus. Each device is activated using a chip select. Once chip select is activated by the bus master, the FM25640 will begin monitoring the clock and data lines. The relationship between the falling edge of /CS, the clock and data is dictated by the SPI mode. The device will make a determination of the SPI mode on the falling edge of each chip select. While there are four such modes, the FM25640 supports modes 0 and 3. Figure 4 shows the required signal relationships for modes 0 and 3. For both modes, data is clocked into the FM25640 on the rising edge of SCK and data is expected on the first rising edge after /CS goes active. If the clock begins from a high state, it will fall prior to beginning data transfer in order to create the first rising edge.

The SPI protocol is controlled by op-codes. These op-codes specify the commands to the part. After /CS is activated the first byte transferred from the bus master is the op-code. Following the op-code, any addresses and data are then transferred.

Certain op-codes are commands with no subsequent data transfer. The /CS must go inactive after an operation is complete and before a new op-code can be issued. There is one valid op-code only per active chip select.

Figure 2. System Configuration with SPI port

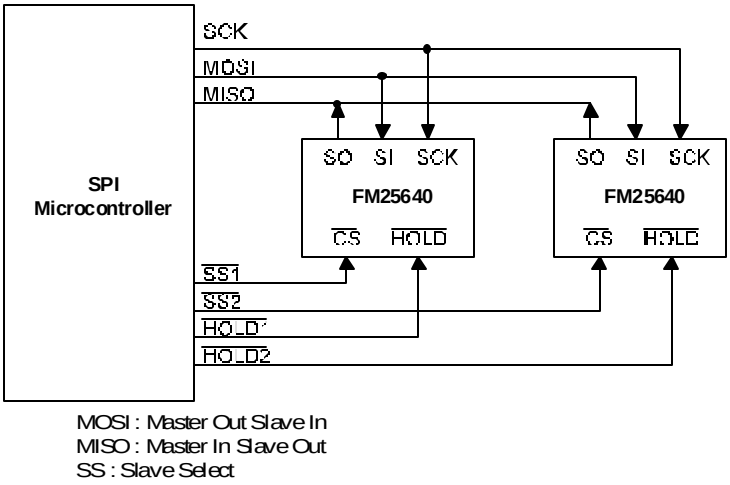


Figure 3. System Configuration without SPI port

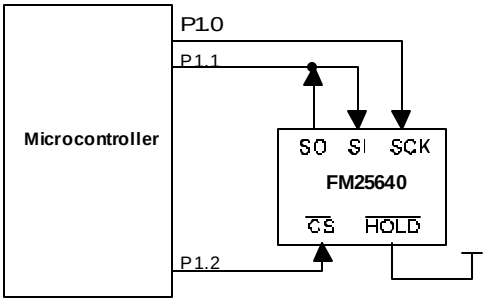
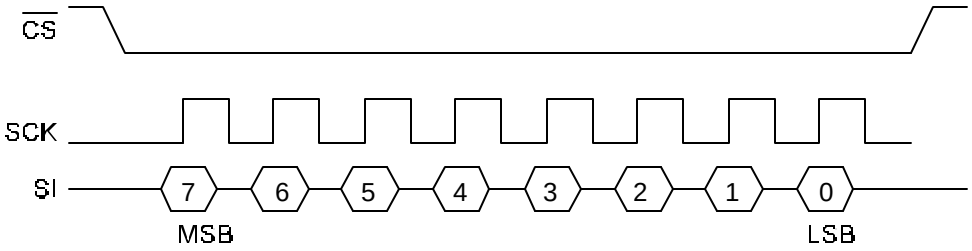
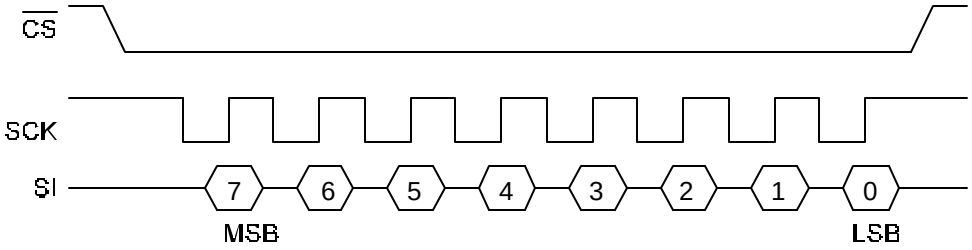


Figure 4. SPI Modes 0 & 3

SPI Mode 0: CPOL=0, CPHA=0



SPI Mode 3: CPOL=1, CPHA=1



Data Transfer

All data transfers to and from the FM25640 occur in 8-bit groups. They are synchronized to the clock signal (SCK) and they transfer most significant bit (MSB) first. Serial inputs are clocked in on the rising edge of SCK. Outputs are driven on the falling edge of SCK.

Command Structure

There are six commands called op-codes that can be issued by the bus master to the FM25640. They are listed in the table below. These op-codes control the functions performed by the memory. They can be divided into three categories. First, are commands that have no subsequent operations. They perform a single function such as to enable a write operation. Second are commands followed by one byte, either in or out. They operate on the status register. Last are commands for memory transactions followed by address and one or more bytes of data.

Table 1. Op-code Commands

Name	Description	Op-code value
WREN	Set Write Enable Latch	00000110b
WRDI	Write Disable	00000100b
RDSR	Read Status Register	00000101b
WRSR	Write Status Register	00000001b
READ	Read Memory Data	00000011b
WRITE	Write Memory Data	00000010b

WREN - Set Write Enable Latch

The FM25640 will power up with writes disabled. The WREN command must be issued prior to any write operation. Sending the WREN op-code will allow the user to issue subsequent op-codes for write operations. These include writing the status register and writing the memory.

Sending the WREN op-code causes the internal Write Enable Latch to be set. A flag bit in the status register, called WEL, indicates the state of the latch. WEL=1 indicates that writes are permitted. Attempting to write the WEL bit in the status register has no effect. Completing any write operation will automatically clear the write-enable latch and prevent further writes without another WREN command. Figure 4 below illustrates the WREN command bus configuration.

WRDI - Write Disable

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the status register and verifying that WEL=0. Figure 5 below illustrates the WRDI command bus configuration.

Figure 5. WREN Bus Configuration

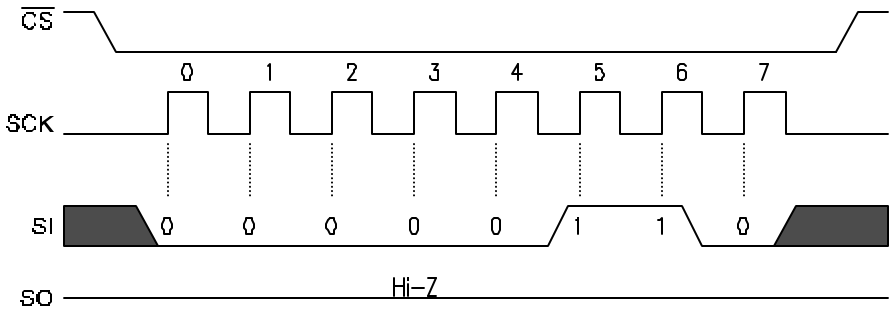
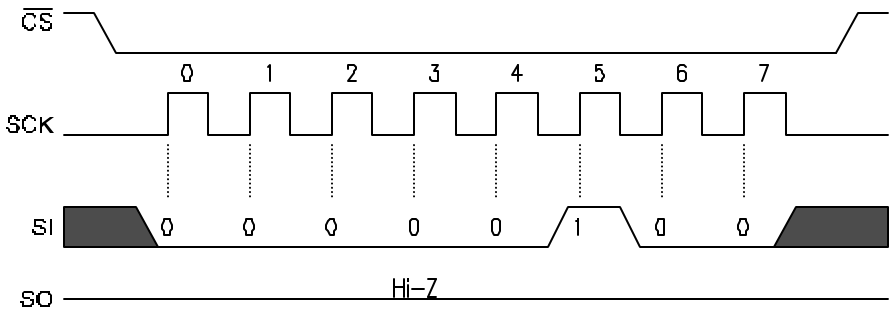


Figure 6. WRDI Bus Configuration



RDSR - Read Status Register

The RDSR command allows the bus master to verify the contents of the Status register. Reading Status provides information about the current state of the write protection features. Following the RDSR op-code, the FM25640 will return one byte with the contents of the Status register. The Status register is described in detail in a later section.

WRSR – Write Status Register

The WRSR command allows the user to select certain write protection features by writing a byte to the Status register. Prior to issuing a WRSR command, the /WP pin must be high or inactive. Note that on the FM25640, /WP only prevents writing to the Status register, not the memory array. Prior to sending the WRSR command, the user must send a WREN command to enable writes. Note that executing a WRSR command is a write operation and therefore clears the Write Enable Latch. The bus configuration of RDSR and WRSR are shown below.

Figure 7. RDSR Bus Configuration

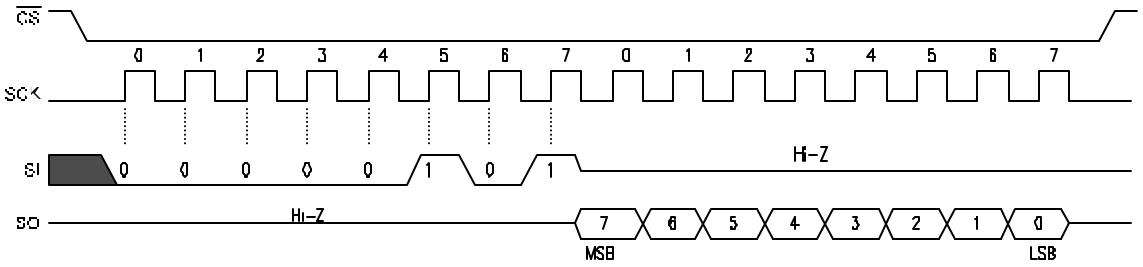
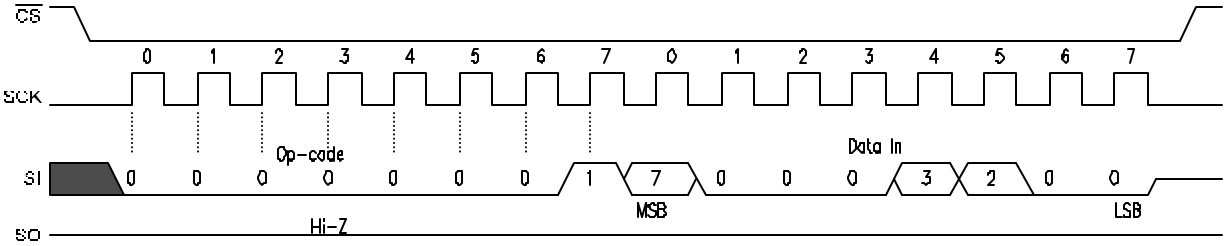


Figure 8. WRSR Bus Configuration



Status Register & Write Protection

The write protection features of the FM25640 are multi-tiered. First, a WREN op-code must be issued prior to any write operation. Assuming that writes are enabled using WREN, writes to memory are controlled by the Status register. As described above, writes to the status register are performed using the WRSR command and subject to the /WP pin. The Status register is organized as follows.

Table 2. Status Register

Bit	7	6	5	4	3	2	1	0
Name	WPEN	0	0	0	BP1	BP0	WEL	0

Bits 0 and 4-6 are fixed at 0 and can not be modified. Note that the Ready bit in many EEPROMs is unnecessary as the FRAM writes in real-time and is never busy. The WPEN, BP1 and BP0 control write protection features. They are nonvolatile! The WEL flag indicates the state of the Write Enable Latch. Writing the WEL bit in the status register has no effect.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write protected as shown in the following table.

Table 3. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	1800h to 1FFFh (upper ¼)
1	0	1000h to 1FFFh (upper ½)
1	1	0000h to 1FFFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The WPEN bit controls the effect of the hardware /WP pin. When WPEN is low, the /WP pin is ignored. When WPEN is high, the /WP pin controls write access to the status register. Thus the Status register is write protected if WPEN=1 and /WP=0.

This scheme provides a write protection mechanism, which can prevent software from writing the memory under any circumstances. This occurs if the BP1 and BP0 are set to 1, the WPEN bit is set to 1, and /WP is set to 0. This occurs because the block protect bits prevent writing memory and the /WP signal in hardware prevents altering the block protect bits (if WPEN is high). Therefore in this condition, hardware must be involved in allowing a write operation. The following table summarizes the write protection conditions.

Table 4. Write Protection

WEL	WPEN	/WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

Memory Operation

The SPI interface, with its relatively high maximum clock frequency, highlights the fast write capability of the FRAM technology. Unlike SPI-bus EEPROMs, the FM25640 can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory array begin with a WREN op-code. The next op-code is the WRITE instruction. This op-code is followed by a two-byte address value. The upper 3-bits of the address are don't care. In total, the 13-bits specify the address of the first byte of the write operation. Subsequent bytes are data and they are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 1FFFh is reached, the counter will roll over to 0000h. Data is written MSB first.

Unlike EEPROMs, any number of bytes can be written sequentially and each byte is written to memory immediately after it is clocked in (after the 8^{th} clock). The rising edge of /CS terminates a WRITE op-code operation.

Read Operation

After the falling edge of /CS, the bus master can issue a READ op-code. Following this instruction is a two-byte address value. The upper 3-bits of the address are don't care. In total, the 13-bits specify the address of the first byte of the read operation. After the op-code and address are complete, the SI line is ignored. The bus master issues 8 clocks, with one bit read out for each. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 1FFFh is reached, the counter will roll over to 0000h. Data is read MSB first. The rising edge of /CS terminates a READ op-code operation. The bus configuration for read and write operations is shown below.

Hold

The /HOLD pin can be used to interrupt a serial operation without aborting it. If the bus master takes the /HOLD pin low while SCK is low, the current operation will pause. Taking the /HOLD pin high while SCK is low will resume an operation. The transitions of /HOLD must occur while SCK is low, but the SCK pin can toggle during a hold state.

Figure 9. Memory Write

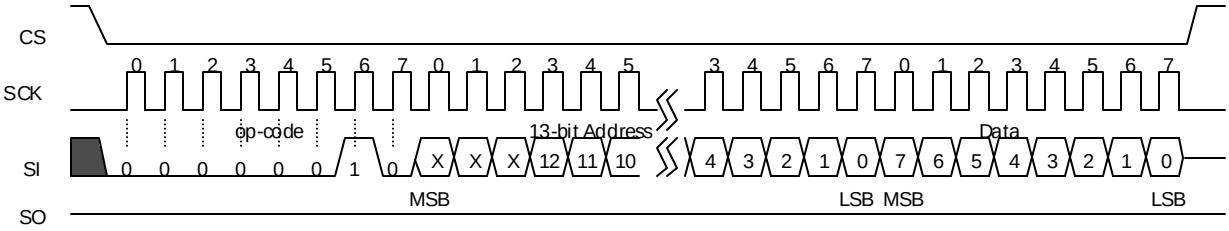
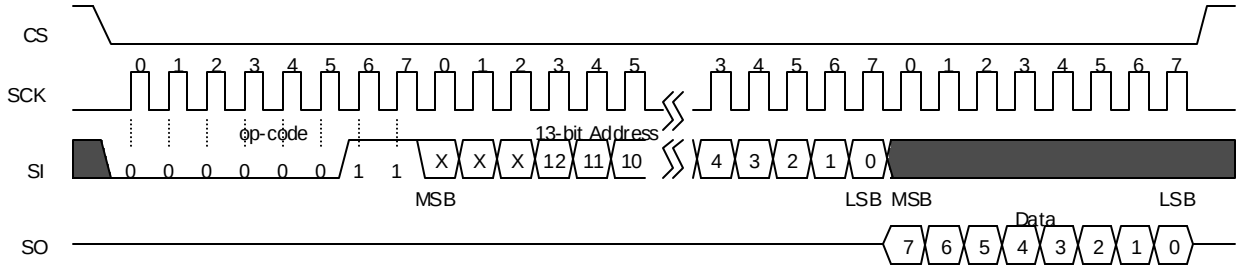


Figure 10. Memory Read



Data Retention and Endurance

Data retention is specified in the electrical specifications below. For purposes of clarity, this section contrasts the retention and endurance of FRAM with EEPROM. The retention performance of FRAM is very comparable to EEPROM in its characteristics. However, the effect of endurance cycles on retention is different.

A typical EEPROM has a write endurance specification that is fixed. Surpassing the specified level of cycles on an EEPROM usually leads to a hard memory failure. By contrast, the effect of increasing cycles on FRAM produces an increase in the soft error rate. That is, there is a higher likelihood of data loss but the memory continues to function properly. A hard failure would not occur by simply exceeding the endurance specification; simply a reduction in data retention reliability. While enough cycles would cause an apparent hard error, this is simply a very high soft error rate. This characteristic makes it problematic to assign a fixed endurance specification.

Endurance is a soft specification. Therefore, the user may operate the device with different levels of endurance cycling for different portions of the memory. For example, critical data needing the highest reliability level could be stored in memory locations that receive comparatively few cycles. Data with shorter-term use could be located in an area receiving many more cycles. A scratchpad area, needing little if any retention can be cycled until there is virtually no retention capability remaining. This would occur several orders of magnitude above the endurance spec.

Internally, a FRAM operates with a read and restore mechanism similar to a DRAM. Therefore, endurance cycles are applied for each access: read or write. The FRAM architecture is based on an array of rows and columns. Each access causes a cycle for an entire row. Therefore, data locations targeted for substantially differing numbers of cycles should not be located within the same row. In the FM25640, there are 2048 rows each 32 bits wide. Each 4 bytes in the address mark the beginning of a new row.

Applications

The versatility of FRAM technology fits into many diverse applications. Clearly the strength of higher write endurance and faster writes make FRAM superior to EEPROM in all but one-time programmable applications. The advantage is most obvious in data collection environments where writes are frequent and data must be nonvolatile.

The attributes of fast writes and high write endurance combine in many innovative ways. A short list of ideas is provided here.

1. Data collection. In applications where data is collected and saved, FRAM provides a superior alternative to other solutions. It is more cost effective than battery backup for SRAM and provides better write attributes than EEPROM.

2. Configuration. Any nonvolatile memory can retain a configuration. However, if the configuration changes and power failure is a possibility, the higher write endurance of FRAM allows changes to be recorded without restriction. Any time the system-state is altered, the change can be written. This avoids writing to memory on power-down when the available time is short and power scarce.

3. High noise environments. Writing to EEPROM in a noisy environment can be challenging. When severe noise or power fluctuations are present, the long write time of EEPROM creates a window of vulnerability during which the write can be corrupted. The fast write of FRAM is complete within a microsecond. This time is typically too short for noise or power fluctuations to disturb it.

4. Time to market. In a complex system, multiple software routines may need to access the nonvolatile memory. In this environment the time delay associated with programming EEPROM adds undue complexity to the software development. Each software routine must wait for complete programming before allowing access to the next routine. When time to market is critical, FRAM can eliminate this simple obstacle. As soon as a write is issued to the FM25640, it is effectively done -- no waiting.

5. RF/ID. In the area of contactless memory, FRAM provides an ideal solution. Since RF/ID memory is powered by an RF field, the long programming time and high current consumption needed to write EEPROM is unattractive. FRAM provides a superior solution. The FM25640 is suitable for multi-chip RF/ID products.

6. Maintenance tracking. In sophisticated systems, the operating history and system-state during a failure is important knowledge. Maintenance can be expedited when this information has been recorded. Due to the high write endurance, FRAM makes an ideal system log. In addition, the convenient interface of the FM25640 allows memory to be distributed throughout the system using minimal additional resources.

Electrical Specifications

Absolute Maximum Ratings

Description	*Ratings*
Ambient storage or operating temperature	-40°C to + 85°C
Voltage on any pin with respect to ground	-1.0V to +7.0V
D.C. output current on any pin	5 mA
Lead temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability

DC Operating Conditions TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	Notes
VDD	Main Power Supply	4.5	5.0	5.5	V	1
IDD	VDD Supply Current @ SCK = 1.0 MHz @ SCK = 2.0 MHz @ SCK = 5.0 MHz		 0.9 1.6 3.0	 1.2 2.5 4.5	mA	2
ISB	Standby Current		1	10	µA	3
ILI	Input Leakage Current			10	µA	4
ILO	Output Leakage Current			10	µA	4
VIL	Input Low Voltage	-0.3		VDD x 0.3	V	1,5
VIH	Input High Voltage	VDD x 0.7		VDD + 0.5	V	1,5
VOL	Output Low Voltage @ IOL = 2 mA			0.4	V	1,5
VOH	Output High Voltage @ IOH = -2 mA	VDD - 0.8			V	1,5
VHYS	Input Hysteresis	VDD x .05			V	1,5

Notes

1. Referenced to VSS.
2. SCK toggling between VDD-0.3V and VSS, other inputs VSS or VDD-0.3V
3. SCK = SI = /CS=VDD. All inputs VSS or VDD.
4. VIN or VOUT = VSS to VDD
5. Characterized but not 100% tested in production.

AC Parameters TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Min	Max	Units	Note
fCK	SCK Clock Frequency	0	5.0	MHz	
tCH	Clock High Time	90		ns	
tCL	Clock Low Time	90		ns	
tCSU	Chip Select Setup	90		ns	
tCSH	Chip Select Hold	90		ns	
tOD	Output Disable		100	ns	2
tODV	Output Data Valid		60	ns	
tOH	Output Hold	0		ns	
tD	Deselect Time	100		ns	
tR	Data In Rise Time		1	µs	1,2
tF	Data In Fall Time		1	µs	1,2
tH	Data Hold Time	30		ns	
tSU	Data Setup Time	20		ns	
tHS	/Hold Setup Time	70		ns	
tHH	/Hold Hold Time	40		ns	
tHZ	/Hold Low to Hi-Z		100	ns	2
tLZ	/Hold High to Data Active		50	ns	2

Notes
1. Rise and fall times measured between 10% and 90% of waveform.
2. Characterized but not 100% tested in production.

Capacitance TA = 25° C, f=1.0 MHz, VDD = 5V

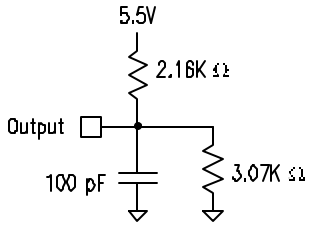
Symbol	Parameter	Max	Units	Notes
CO	Output capacitance (SDA)	8	pF	1
CI	Input capacitance	6	pF	1

Notes
1. This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	VDD * 0.1 to VDD * 0.9
Input rise and fall times	10 ns
Input and output timing levels	VDD*0.5

Equivalent AC Load Circuit

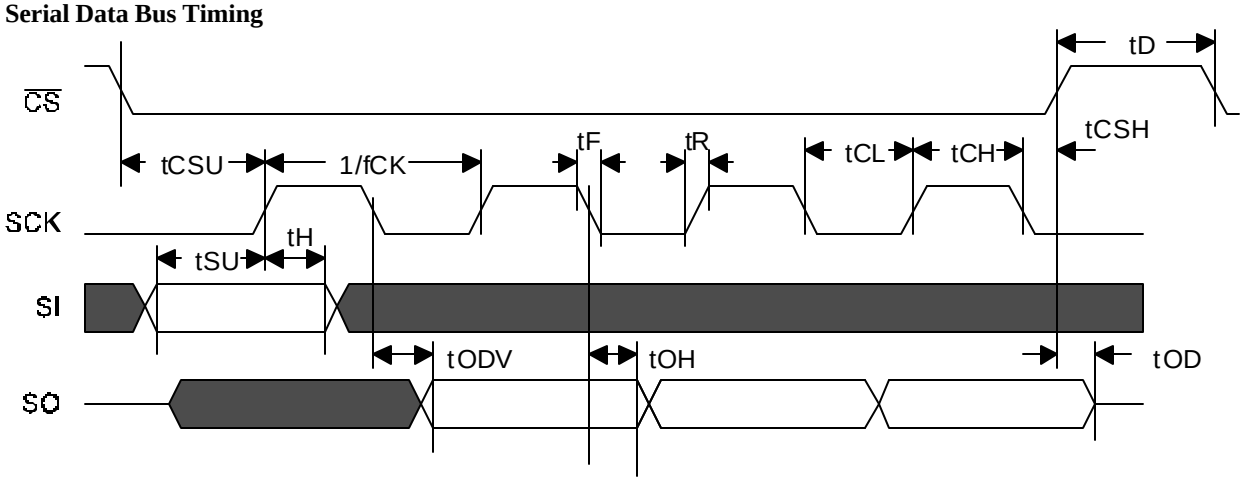


Data Retention TA = -40° C to + 85° C, VDD = 4.5V to 5.5V unless otherwise specified

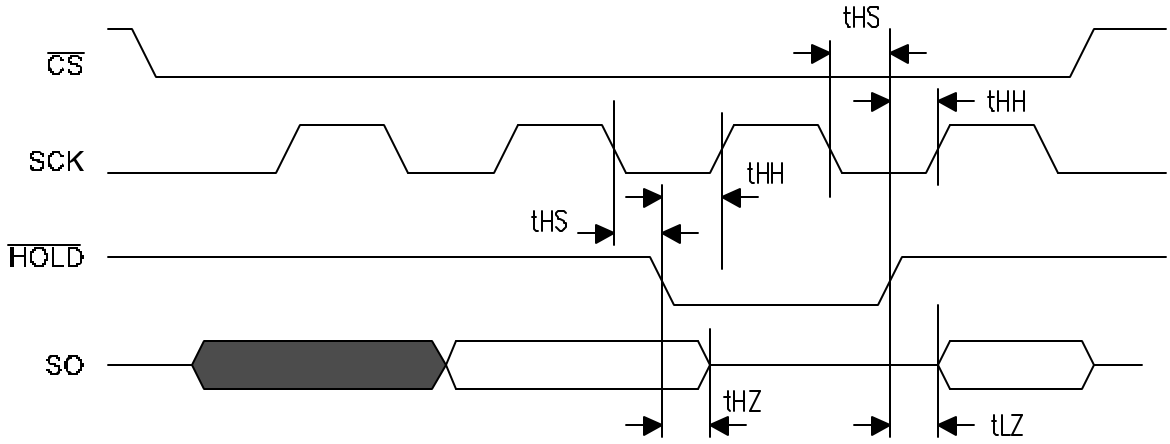
Parameter	Min	Units	Notes
Data Retention	10	Years	1

Notes
1. Data retention is specified at 85° C. The relationship between retention, temperature, and the associated reliability level is characterized separately.

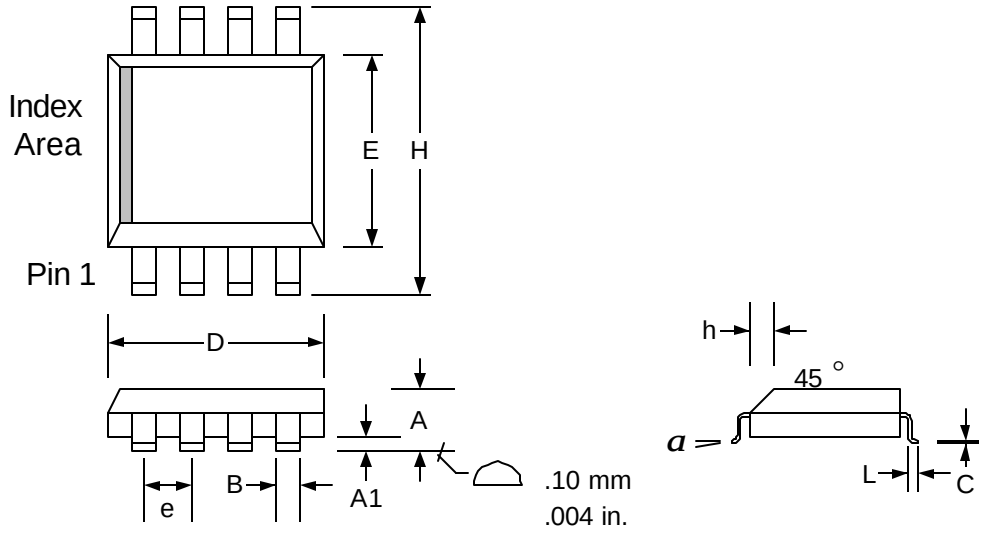
Serial Data Bus Timing



/Hold Timing



8-pin SOP JEDEC MS-012



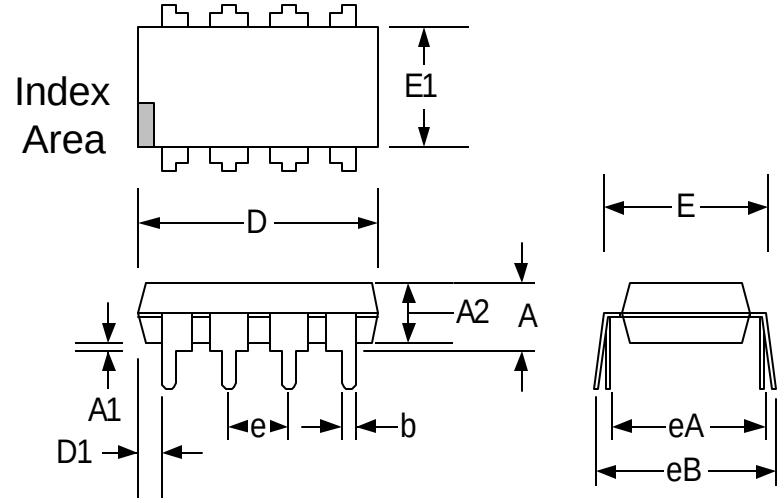
Selected Dimensions

Refer to JEDEC MS-012 for complete dimensions and notes.

Controlling dimensions is in millimeters. Conversions to inches are not exact.

Symbol	Dim	Min	Nom.	Max
A	mm in.	1.35 .053		1.75 .069
A1	mm in.	.10 .004		.25 .010
B	mm in.	.33 .013		.51 .020
C	mm in.	.19 .007		.25 .010
D	mm in.	4.80 .189		5.00 .197
E	mm in.	3.80 .150		4.00 .157
e	mm in.		1.27 BSC .050 BSC	
H	mm in.	5.80 .228		6.20 .244
h	mm in.	.25 .010		.50 .197
L	mm in.	.40 .016		1.27 .050
α		0°		8°

8-pin DIP JEDEC MS-001



Selected Dimensions
Refer to JEDEC MS-001 for complete dimensions and notes.
Controlling dimensions is in inches. Conversions to millimeters are not exact.

Symbol	Dim	Min	Nom.	Max
A	in. mm			.210 5.33
A1	in. mm	0.015 .381		
A2	in. mm	0.115 2.92	0.130 3.30	0.195 4.95
b	in. mm	0.014 .356	0.018 .457	0.022 .508
D	in. mm	0.355 9.02	0.365 9.27	0.400 10.2
D1	in. mm	0.005 .127		
E	in. mm	0.300 7.62	0.310 7.87	0.325 8.26
E1	in. mm	0.240 6.10	0.250 6.35	0.280 7.11
e	in. mm		.100 BSC 2.54 BSC	
eA	in. mm		.300 BSC 7.62 BSC	
eB	in. mm			0.430 10.92
L	in. mm	0.115 2.92	0.130 3.30	0.150 3.81