Errata Pertains to the EP7311-CV-B, EP7311-CV-B, EP7312-CB-B, EP7312-CV-B devices

Interfacing to SDRAM

Description

If cache is not turned on for all SDRAM bus cycles, an internal bus arbitration problem may occur. This condition will cause the executing code running out of SDRAM to abort.

Workaround

When interfacing to SDRAM, both MMU and cache must be enabled.

Interfacing to 32-bit External SDRAM

Description

When interfacing to a single 32-bit external SDRAM, the column address is never presented.

Workaround

Configure the SDRAM controller as two 16-bit SDRAM devices providing a total bus width of 32-bits. The memory controller will then allow access to all memory locations, however the memory will not be contiguous as the Bank select pins will be configure for two 16-bit external memory devices and not one 32-bit external memory device.

Using a debugger or the Angel monitor, access all memory locations to determine the physical location of the memory. Due to the internal bank selects, the physical memory may not be contiguous. If the memory is non-contiguous, program the MMU to translate the non-contiguous physical memory to contiguous virtual memory.

Interfacing to 16-bit External SDRAM

Description

When performing a load multiple or store multiple of two or more words using 16-bit SDRAM on a non-biword aligned address, the word data order will be swapped.

Workaround

For routines which use load or store multiple accesses, place that data array in on-chip memory (i.e. Place Stack Pointer in Internal SRAM).

Unique Device ID (UNIQID) and Random Device ID (RANDID[3:0])

Description

Some devices have not been assigned unique device IDs and random device IDs. The value of these registers when they are not assigned will be zero.

Workaround

Unique and random device IDs will be enabled in Rev. C of the silicon.

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LCD Frame Buffer Held 16-bit External SDRAM.

Description

When using 16-bit wide SDRAM for the frame buffer, the data may be rearranged.

Workaround

1) Do not perform any half-word or byte accesses.

2) Use two 16-bit SDRAM devices to generate a 32-bit wide bus.

For any questions regarding this Errata, please send email to: epdapps@crystal.cirrus.com