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Errata: CS89712 Rev. C

(Reference CS89712 Data Sheet revision DS502PP2 dated FEB '01)

1. CACHE AND SDRAM INTERACTION

Problem Description

If the cache is not turned on for all SDRAM bus cycles, an internal bus arbitration problem may occur. This condition will cause the executing code running out of SDRAM to abort.

Workaround

Both MMU and cache must be enabled for systems which include SDRAM.

Status

Correct operation will be documented in the next revision of the User's Manual.

Please email questions concerning this information to ethernet@crystal.cirrus.com