

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16543FT**LOW-VOLTAGE 16-BIT REGISTERED TRANSCEIVER WITH 3.6 V
TOLERANT INPUTS AND OUTPUTS**

The TC74VCX16543FT is a high performance CMOS 16-bit REGISTERED TRANSCEIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

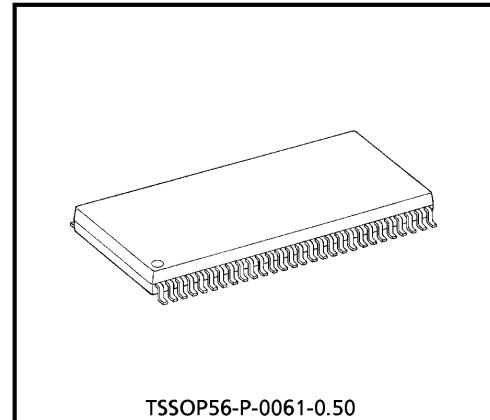
It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

The TC74VCX16543FT can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the Alatches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

When the \overline{OE} input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

Weight : 0.25 g (Typ.)

FEATURES

- Low Voltage Operation : $V_{CC} = 1.8\sim 3.6$ V
- High Speed Operation : $t_{pd} = 3.5$ ns (max) at $V_{CC} = 3.0\sim 3.6$ V
 : $t_{pd} = 4.0$ ns (max) at $V_{CC} = 2.3\sim 2.7$ V
 : $t_{pd} = 8.0$ ns (max) at $V_{CC} = 1.8$ V
- 3.6 V Tolerant inputs and outputs.
- Output Current : $I_{OH}/I_{OL} = \pm 24$ mA (min) at $V_{CC} = 3.0$ V
 : $I_{OH}/I_{OL} = \pm 18$ mA (min) at $V_{CC} = 2.3$ V
 : $I_{OH}/I_{OL} = \pm 6$ mA (min) at $V_{CC} = 1.8$ V
- Latch-up Performance : ± 300 mA
- ESD Performance : Human Body Model $> \pm 2000$ V
 : Machine Model $> \pm 200$ V
- Package : TSSOP
 (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 3).

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- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

(Note 1) : Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

(Note 2) : All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.

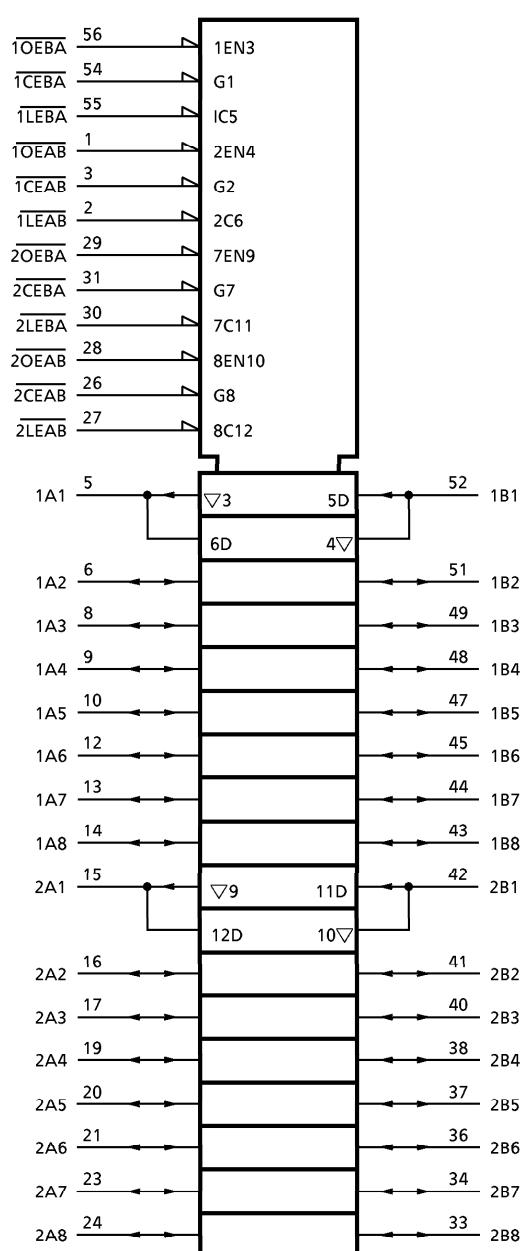
(Note 3) : To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

PIN ASSIGNMENT

\overline{OEAB}	1	56	\overline{OEBA}
\overline{LEAB}	2	55	\overline{LEBA}
\overline{CEAB}	3	54	\overline{CEBA}
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
\overline{CEAB}	26	31	\overline{CEBA}
\overline{LEAB}	27	30	\overline{LEBA}
\overline{OEAB}	28	29	\overline{OEBA}

(TOP VIEW)

SYMBOL



980910EBA2'

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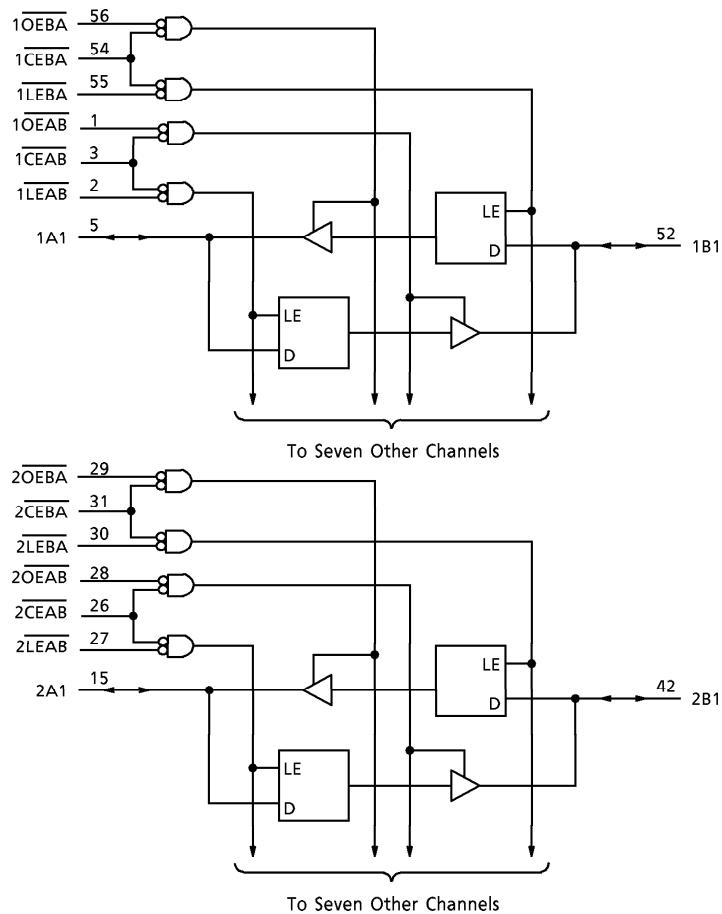
FUNCTION TABLE* (each 8-bit latch)

INPUTS				OUTPUTS B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ **
L	L	L	L	L
L	L	L	H	H

* A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

** Output level before the indicated steady-state input conditions were established.

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	-0.5~4.6	V
DC Input Voltage (OEAB, OEBA, LEAB, LEBA, CEAB, CEBA)	V_{IN}	-0.5~4.6	V
DC Bus I/O Voltage	$V_{I/O}$	-0.5~4.6 (Note 1)	V
		-0.5~ V_{CC} + 0.5 (Note 2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC}/I_{GND}	± 100	mA
Storage Temperature	T_{stg}	-65~150	°C

(Note 1) : Off-State

(Note 2) : High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage (OEAB, OEBA, LEAB, LEBA, CEAB, CEBA)	V_{IN}	-0.3~3.6	V
Bus I/O Voltage	$V_{I/O}$	0~3.6 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH}/I_{OL}	± 24 (Note 7)	mA
		± 18 (Note 8)	
		± 6 (Note 9)	
Operating Temperature	T_{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 10)	ns/V

(Note 4) : Data Retention Only

(Note 5) : Off-State

(Note 6) : High or Low State

(Note 7) : $V_{CC} = 3.0 \sim 3.6$ V(Note 8) : $V_{CC} = 2.3 \sim 2.7$ V(Note 9) : $V_{CC} = 1.8$ V(Note 10) : $V_{IN} = 0.8 \sim 2.0$ V, $V_{CC} = 3.0$ V

ELECTRICAL CHARACTERISTICSDC characteristics ($T_a = -40\sim85^\circ C$, $2.7 V < V_{CC} \leq 3.6 V$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT	
Input Voltage	"H" Level	V_{IH}				2.7~3.6	2.0	—	V
	"L" Level	V_{IL}			2.7~3.6	—	0.8	V	
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100 \mu A$	2.7~3.6	$V_{CC} - 0.2$	—	V	
				$I_{OH} = -12 mA$	2.7	2.2	—		
				$I_{OH} = -18 mA$	3.0	2.4	—		
				$I_{OH} = -24 mA$	3.0	2.2	—		
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	2.7~3.6	—	0.2	V	
				$I_{OL} = 12 mA$	2.7	—	0.4		
				$I_{OL} = 18 mA$	3.0	—	0.4		
				$I_{OL} = 24 mA$	3.0	—	0.55		
Input Leakage Current	I_{IN}	$V_{IN} = 0\sim3.6 V$		2.7~3.6	—	± 5.0	μA		
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL}		2.7~3.6	—	± 10.0	μA		
Power Off Leakage Current	I_{OFF}	$V_{IN}, V_{OUT} = 0\sim3.6 V$		0	—	10.0	μA		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		2.7~3.6	—	20.0	μA		
		$V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6 V$		2.7~3.6	—	± 20.0			
Increase In I_{CC} Per Input	ΔI_{CC}	$V_{IH} = V_{CC} - 0.6 V$		2.7~3.6	—	750	μA		

ELECTRICAL CHARACTERISTICSDC characteristics ($T_a = -40\sim85^\circ C$, $2.3 V \leq V_{CC} \leq 2.7 V$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT	
Input Voltage	"H" Level	V_{IH}				2.3~2.7	1.6	—	V
	"L" Level	V_{IL}			2.3~2.7	—	0.7	V	
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100 \mu A$	2.3~2.7	$V_{CC} - 0.2$	—	V	
				$I_{OH} = -6 mA$	2.3	2.0	—		
				$I_{OH} = -12 mA$	2.3	1.8	—		
				$I_{OH} = -18 mA$	2.3	1.7	—		
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	2.3~2.7	—	0.2	V	
				$I_{OL} = 12 mA$	2.3	—	0.4		
				$I_{OL} = 18 mA$	2.3	—	0.6		
				$I_{OL} = 24 mA$	2.3	—	0.8		
Input Leakage Current	I_{IN}	$V_{IN} = 0\sim3.6 V$		2.3~2.7	—	± 5.0	μA		
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL}		2.3~2.7	—	± 10.0	μA		
Power Off Leakage Current	I_{OFF}	$V_{IN}, V_{OUT} = 0\sim3.6 V$		0	—	10.0	μA		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND		2.3~2.7	—	20.0	μA		
		$V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6 V$		2.3~2.7	—	± 20.0			

ELECTRICAL CHARACTERISTICSDC characteristics ($T_a = -40\sim85^\circ C$, $1.8 V \leq V_{CC} < 2.3 V$)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	MIN	MAX	UNIT	
Input Voltage	"H" Level	V_{IH}				$1.8\sim2.3$	$0.7 \times V_{CC}$	—	
	"L" Level	V_{IL}				$1.8\sim2.3$	—	$0.2 \times V_{CC}$	
Output Voltage	"H" Level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100 \mu A$	1.8	$V_{CC} - 0.2$	—	V	
	"L" Level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \mu A$	1.8	1.4	—		
Input Leakage Current		I_{IN}	$V_{IN} = 0\sim3.6 V$		1.8	—	± 5.0	μA	
3-State Output Off-State Current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0\sim3.6 V$		1.8	—	± 10.0	μA	
Power Off Leakage Current		I_{OFF}	$V_{IN}, V_{OUT} = 0\sim3.6 V$		0	—	10.0	μA	
Quiescent Supply Current		I_{CC}	$V_{IN} = V_{CC}$ or GND		1.8	—	20.0	μA	
			$V_{CC} \leq (V_{IN}, V_{OUT}) \leq 3.6 V$		1.8	—	± 20.0		

AC characteristics ($T_a = -40\sim85^\circ C$, Input $t_r = t_f = 2.0 \text{ ns}$, $C_L = 30 \text{ pF}$, $R_L = 500 \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC} (\text{V})$	MIN	MAX	UNIT
			1.8	1.5	8.0	
Propagation Delay Time (An, Bn-Bn, An)	t_{pLH} t_{pHL}	(Fig.1, 2)	2.5 \pm 0.2	0.8	4.0	ns
			3.3 \pm 0.3	0.6	3.5	
			1.8	1.5	9.8	
Propagation Delay Time (LEAB, LEBA-Bn, An)	t_{pLH} t_{pHL}	(Fig.1, 2)	2.5 \pm 0.2	0.8	5.0	ns
			3.3 \pm 0.3	0.6	3.9	
			1.8	1.5	9.8	
3-State Output Enable Time (OEAB, OEBA, CEAB, CEBA)	t_{pZL} t_{pZH}	(Fig.1, 4)	2.5 \pm 0.2	0.8	4.9	ns
			3.3 \pm 0.3	0.6	3.8	
			1.8	1.5	7.6	
3-State Output Disable Time (OEAB, OEBA, CEAB, CEBA)	t_{pLZ} t_{pHZ}	(Fig.1, 4)	2.5 \pm 0.2	0.8	4.2	ns
			3.3 \pm 0.3	0.6	3.7	
			1.8	4.0	—	
Minimum Pulse Width (LEAB, LEBA, CEAB, CEBA)	$t_w (\text{L})$	(Fig.1, 2, 3)	2.5 \pm 0.2	1.5	—	ns
			3.3 \pm 0.3	1.5	—	
			1.8	2.5	—	
Minimum Set-up Time (An, Bn-LE, CE)	t_s	(Fig.1, 2, 3)	2.5 \pm 0.2	1.5	—	ns
			3.3 \pm 0.3	1.5	—	
			1.8	1.0	—	
Minimum Hold Time (An, Bn-LE, CE)	t_h	(Fig.1, 2, 3)	2.5 \pm 0.2	1.0	—	ns
			3.3 \pm 0.3	1.0	—	
			1.8	—	0.5	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 11)	2.5 \pm 0.2	—	0.5	ns
			3.3 \pm 0.3	—	0.5	

For $C_L = 50 \text{ pF}$, add approximately 300 ps to the AC maximum specification.

(Note 11) : Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic switching characteristics ($T_a = 25^\circ\text{C}$, Input $t_r = t_f = 2.0 \text{ ns}$, $C_L = 30 \text{ pF}$)

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC} (\text{V})$	TYP.	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (Note 12)	1.8	0.25	V
		$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (Note 12)	2.5	0.6	
		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (Note 12)	3.3	0.8	
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (Note 12)	1.8	-0.25	V
		$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (Note 12)	2.5	-0.6	
		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (Note 12)	3.3	-0.8	
Quiet Output Minimum Dynamic V_{OH}	V_{OHV}	$V_{IH} = 1.8 \text{ V}, V_{IL} = 0 \text{ V}$ (Note 12)	1.8	1.5	V
		$V_{IH} = 2.5 \text{ V}, V_{IL} = 0 \text{ V}$ (Note 12)	2.5	1.9	
		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$ (Note 12)	3.3	2.2	

(Note 12) : Parameter guaranteed by design.

Capacitive characteristics ($T_a = 25^\circ\text{C}$)

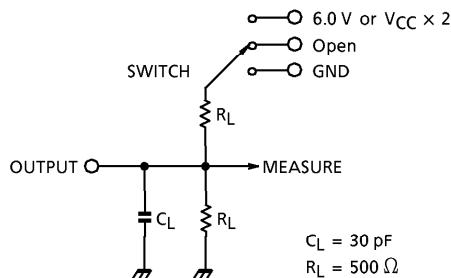
PARAMETER	SYMBOL	TEST CONDITION	$V_{CC} (\text{V})$	TYP.	UNIT
Input Capacitance	C_{IN}	—	1.8, 2.5, 3.3	6	pF
Bus I/O Capacitance	$C_{I/O}$	—	1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C_{PD}	$f_{IN} = 10 \text{ MHz}$ (Note 13)	1.8, 2.5, 3.3	20	pF

(Note 13) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC (\text{opr.})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16 \text{ (per bit)}$$

TEST CIRCUIT
Fig.1



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	6.0 V @ $V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} \times 2$ @ $V_{CC} = 2.5 \pm 0.2 \text{ V}$ @ $V_{CC} = 1.8 \text{ V}$
t_{pHZ}, t_{pZH}	GND

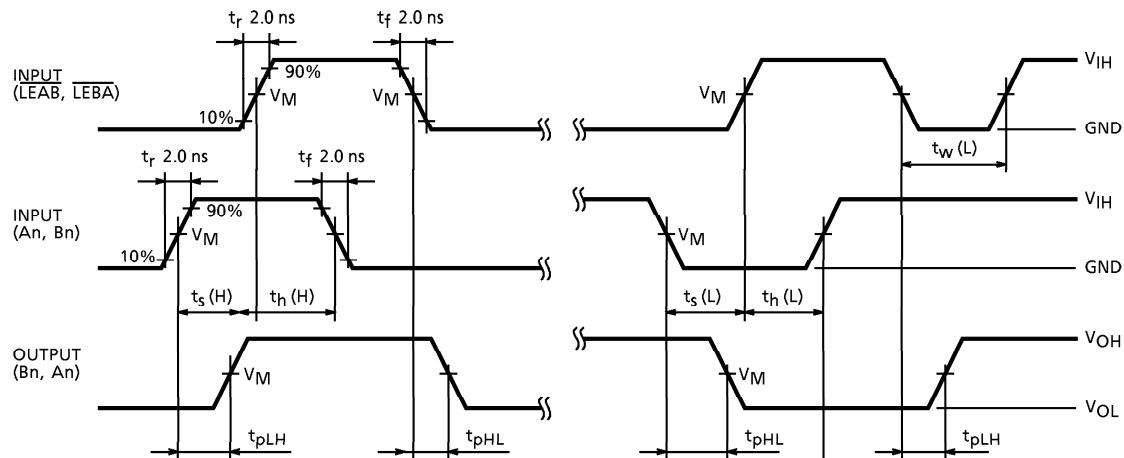
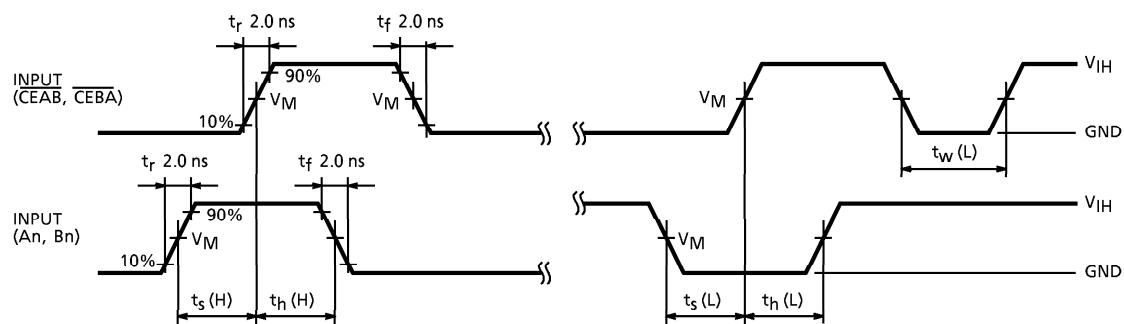
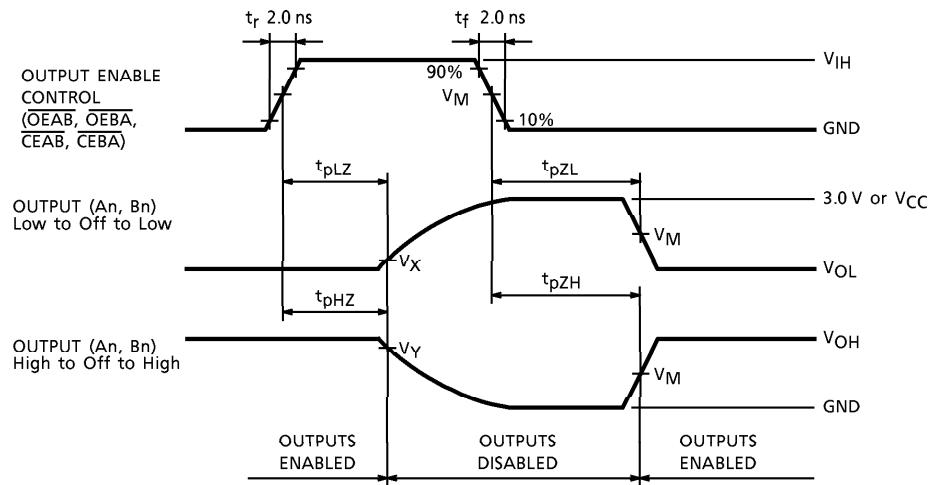
AC WAVEFORMFig.2 t_{pLH} , t_{pHL} , t_w , t_s , t_h Fig.3 t_w , t_s , t_h 

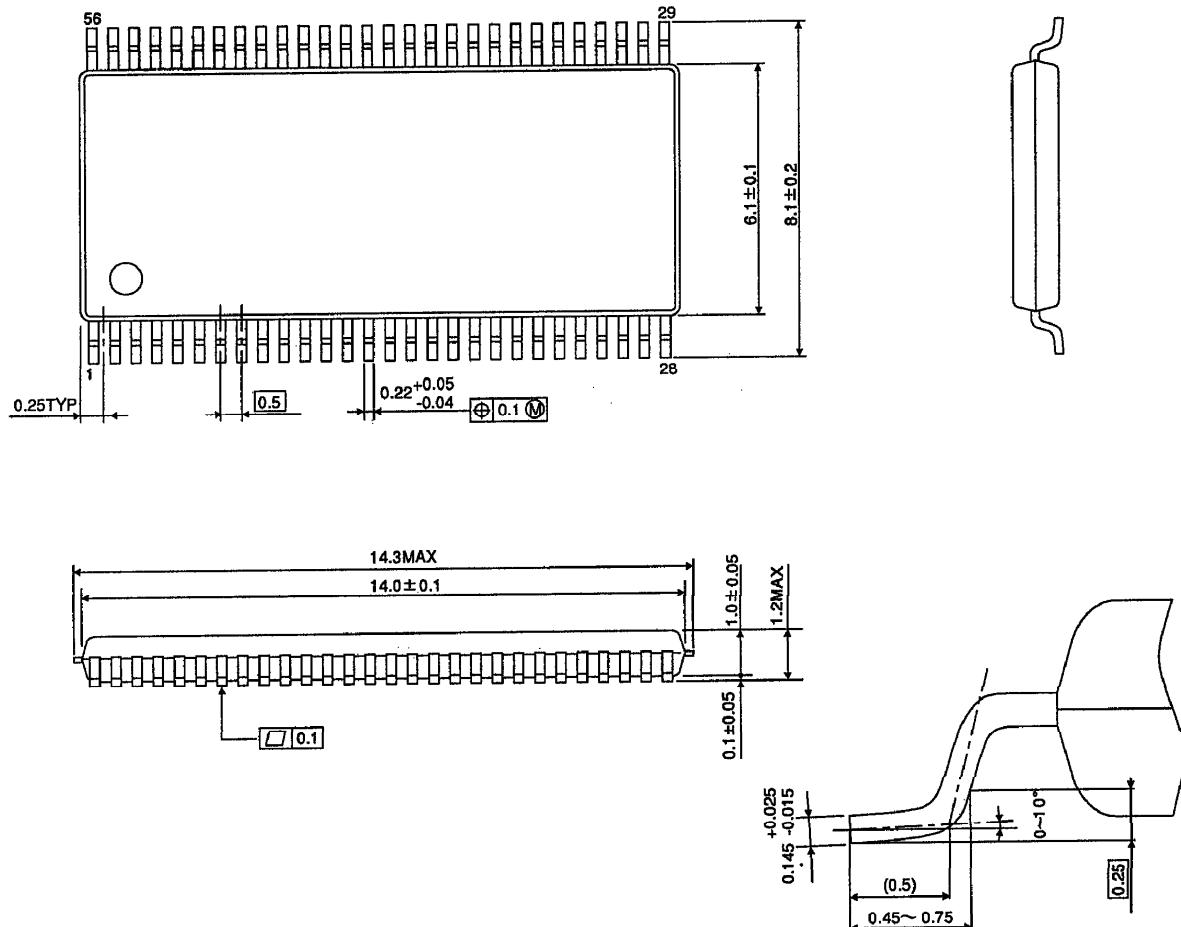
Fig.4 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH} 

SYMBOL	V_{CC}		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC} / 2$	$V_{CC} / 2$
V_X	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
V_Y	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

PACKAGE DIMENSIONS

TSSOP56-P-0061-0.50

Unit : mm



Weight : 0.25 g (Typ.)