

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WBD125FK

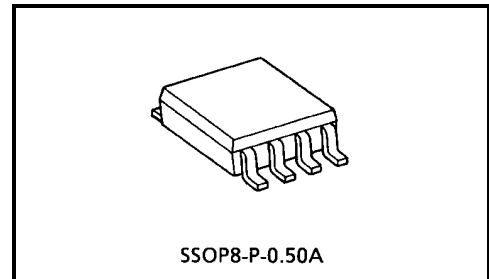
Dual Bus Switch with Level Shift

The TC7WBD125FK is a low on-resistance, high-speed CMOS dual-bit bus switch. This bus switch allows the connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

When output enable (\overline{OE}) is at low level, the switch is on; when at high level, the switch is off.

The internal diode which adds to power supply line is enable to realize the shift of signal level from 5 V to 3.3 V

All inputs are equipped with protector circuits to protect the device from static discharge.

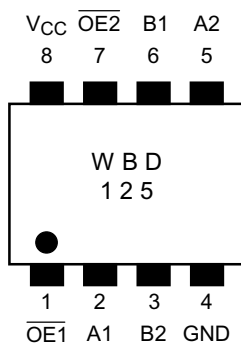


Weight: 0.01 g (typ.)

Features

- Operating voltage: $V_{CC} = 4.5\sim 5.5$ V
- High speed operation: $t_{pd} = 0.25$ ns (max)
- Ultra-low on resistance: $R_{ON} = 5 \Omega$ (typ.)
- Electro-static discharge (ESD) performance: ± 200 V or more (EIAJ)
 ± 2000 V or more (MIL)
- TTL level input (control input)
- Package: US8

Pin Assignment (top view)



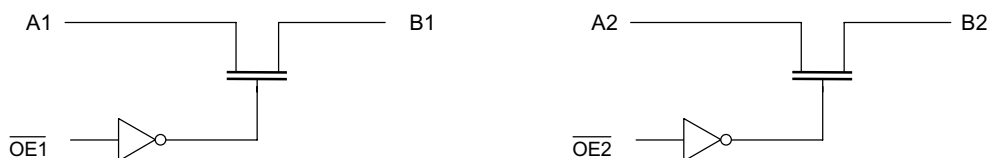
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Truth Table

Inputs	Function
$\overline{\text{OE}}$	
L	A port = B port
H	Disconnect

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5~7.0	V
Control pin input voltage	V_{IN}	-0.5~7.0	V
Switch terminal I/O voltage	V_S	-0.5~7.0	V
Clump diode current	I_{IK}	-50	mA
Switch I/O current	I_S	128	mA
Power dissipation	P_D	200	mW
DC V_{CC}/GND current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65~150	$^{\circ}\text{C}$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	4.5~5.5	V
Control pin input voltage	V_{IN}	0~5.5	V
Switch I/O voltage	V_S	0~5.5	V
Operating temperature	T_{opr}	-40~85	$^{\circ}\text{C}$
Control pin input rise/fall time	dt/dv	0~10	ns/V

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Typ. (Note1)	Max	Unit
Control pin input voltage	"H" level	V _{IH}	—		2.0	—	—	V
	"L" level	V _{IL}	—		—	—	0.8	
High-level output voltage		V _{OH}	Figure 4		—	—	—	—
Input leakage current		I _{IN}	V _{IN} = 0~5.5 V		5.5	—	±1.0	μA
Off-state leakage current (switch off)		I _{SZ}	A, B = 0~5.5 V, $\overline{OE} = V_{CC}$		5.5	—	±1.0	μA
ON resistance (Note2)	R _{ON}	V _{IS} = 0 V	I _{IS} = 64 mA	4.5	—	5	7	Ω
			I _{IS} = 30 mA	4.5	—	5	7	
		V _{IS} = 2.4 V, I _{IS} = 15 mA		4.5	—	35	50	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND I _{OUT} = 0	switch ON	5.5	—	—	1.5	mA
			switch OFF	5.5	—	—	10	μA
	ΔI _{CC}	V _{IN} = 3.4 V (one input)		5.5	—	—	2.5	mA

Note1: The typical values are at V_{CC} = 5 V, Ta = 25°C.

Note2: Apply the specified current to the switch, then measure the voltages on pins A and B. The on-resistance is the lower of the two.

AC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Max	Unit	
								V _{CC} (V)
Propagation delay time (bus to bus)		t _{pLH} t _{pHL}	Figure 1, Figure 2 (Note3)		4.5	—	0.25	ns
Output enable time		t _{pZL} t _{pZH}	Figure 1, Figure 3		4.5	—	4.5	ns
Output disable time		t _{pLZ} t _{pHZ}	Figure 1, Figure 3		4.5	—	5.0	ns

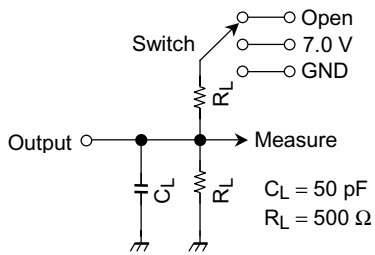
Note3: The propagation delay time is calculated by the RC (on-resistance and load capacitance) time constant.

Capacitive Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition		Typ.	Unit	
							V _{CC} (V)
Control pin input capacitance		C _{IN}	(Note4)		5.0	3	pF
Switch terminal capacitance		C _{I/O}	$\overline{OE} = V_{CC}$		5.0	10	pF

Note4: This parameter is guaranteed by design.

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	7.0 V
t_{pHZ}, t_{pZH}	Open

Figure 1

AC Waveform

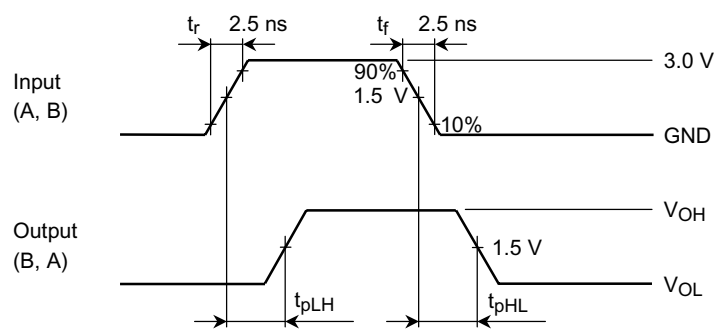


Figure 2 t_{pLH}, t_{pHL}

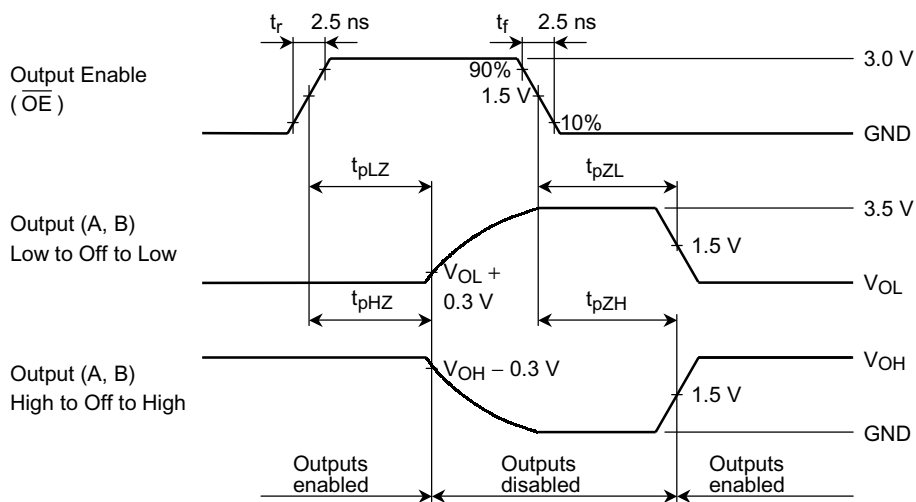


Figure 3 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$

$V_{OH} - V_{CC}$ Characteristics (typ.)

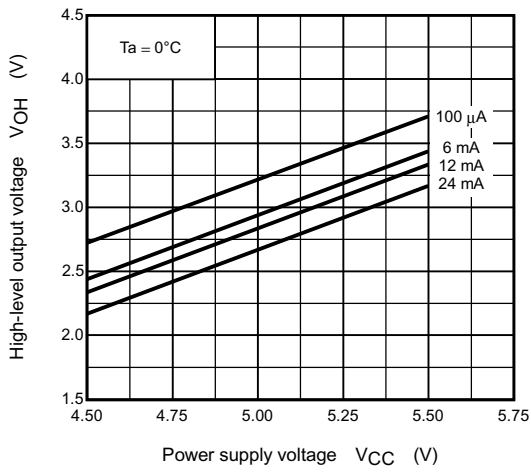
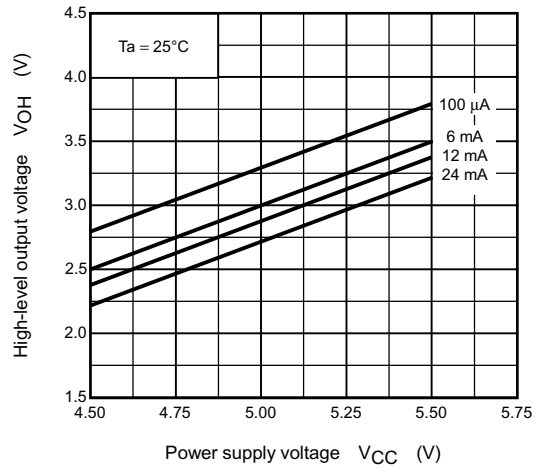
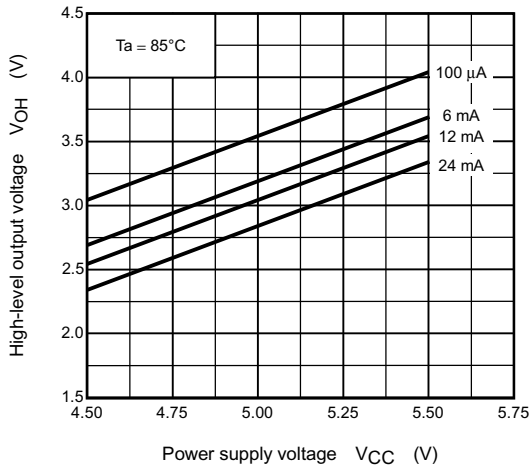
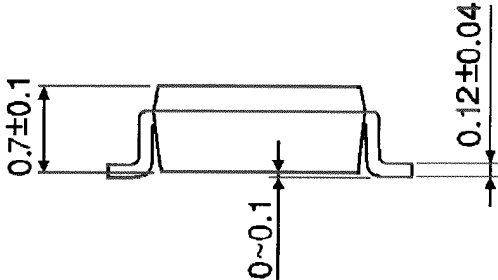
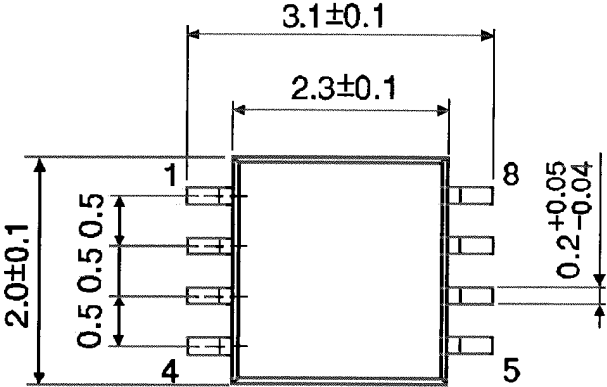


Figure 4

Package Dimensions

SSOP8-P-0.50A

Unit : mm



Weight: 0.01 g (typ.)