

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7SBD384FU

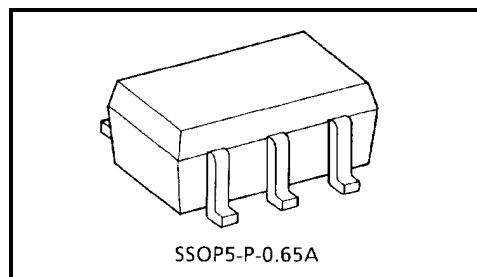
Single Bus Switch with Level Shifting

The TC7SBD384FU provides single bit of high-speed TTL-compatible switching. The low on resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as just 1-bit low-impedance switch with output-enable (\overline{OE}) input. When \overline{OE} is low, the switch is on and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

The internal diode which adds to power supply line is enable to realize the shift of signal level from 5 V to 3.3 V.

All inputs are equipped with protection circuits against static discharge.

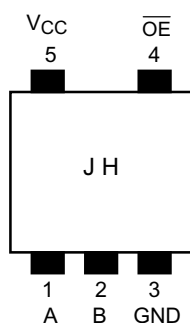


Weight: 0.006 g (typ.)

Features

- Operating voltage: $V_{CC} = 4.5 \sim 5.5$ V
- High speed operation: $t_{pd} = 0.25$ ns (max)
- Low on resistance: $R_{ON} = 5 \Omega$ (typ.)
- ESD performance: Machine model $> \pm 200$ V
Human body model $> \pm 2000$ V
- TTL level input (control input)
- Package: USV

Pin Assignment (top view)



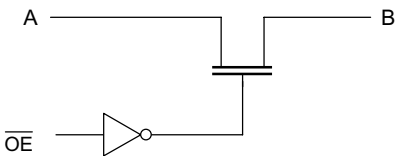
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Truth Table

Input	Function
$\overline{\text{OE}}$	
L	A port = B port
H	Disconnect

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply range	V_{CC}	-0.5~7.0	V
DC input voltage	V_{IN}	-0.5~7.0	V
DC switch voltage	V_S	-0.5~7.0	V
Input diode current	I_{IK}	-50	mA
Continuous channel current	I_S	128	mA
Power dissipation	P_D	200	mW
DC V_{CC} /GND current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65~150	$^{\circ}\text{C}$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5~5.5	V
Input voltage	V_{IN}	0~5.5	V
Switch voltage	V_S	0~5.5	V
Operating temperature	T_{opr}	-40~85	$^{\circ}\text{C}$
Input rise and fall time	dt/dv	0~10	ns/V

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Typ. (Note1)	Max	Unit
				V _{CC} (V)				
Input voltage	"H" level	V _{IH}	—	4.5~5.5	2.0	—	—	V
	"L" level	V _{IL}	—	4.5~5.5	—	—	0.8	
High-level output voltage		V _{OH}	Figure 4	—	—	—	—	—
Input leakage current		I _{IN}	V _{IN} = 0~5.5 V	5.5	—	—	±1.0	μA
Off-state leakage current (switch off)		I _{SZ}	A, B = 0~5.5 V, $\overline{OE} = V_{CC}$	5.5	—	—	±1.0	μA
ON resistance (Note2)	R _{ON}	V _{IS} = 0 V	I _{IS} = 30 mA	4.5	—	5	7	Ω
			I _{IS} = 64 mA	4.5	—	5	7	
		V _{IS} = 2.4 V, I _{IS} = 15 mA		4.5	—	35	50	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0	Switch ON	5.5	—	—	1.5	mA
			Switch OFF	5.5	—	—	10	μA
	ΔI _{CC}	V _{IN} = 3.4 V (one input)		5.5	—	—	2.5	mA

Note1: Typical values are at V_{CC} = 5 V and Ta = 25°C.

Note2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Max	Unit
				V _{CC} (V)			
Propagation delay time (bus to bus)	t _{pLH} t _{pHL}	Figure 1, Figure 2	(Note3)	4.5	—	0.25	ns
Output enable time	t _{pZL} t _{pZH}	Figure 1, Figure 3		4.5	—	4.5	ns
Output disable time	t _{pLZ} t _{pHZ}	Figure 1, Figure 3		4.5	—	4.5	ns

Note3: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition		Typ.	Unit
				V _{CC} (V)		
Control pin input capacitance		C _{IN}	(Note4)	5.0	3	pF
Switch terminal capacitance		C _{I/O}	$\overline{OE} = V_{CC}$ (Note4)	5.0	10	pF

Note4: This item is guaranteed by design.

Switch

Open

7.0 V

GND

Output

Measure

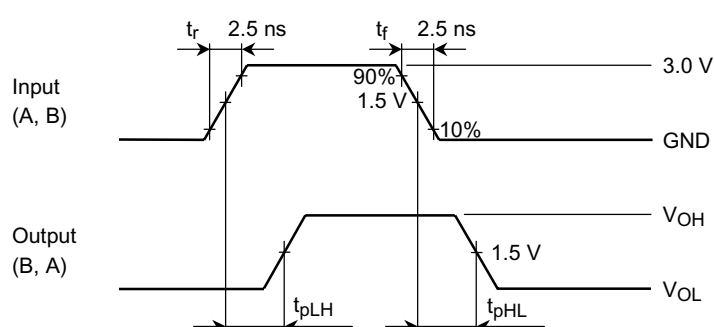
R_L

C_L

$C_L = 50 \text{ pF}$

$R_L = 500 \Omega$

Parameter	Switch
t_{pLH} , t_{pHL}	Open
t_{pLZ} , t_{pZL}	7.0 V
t_{pHZ} , t_{pZH}	Open



Timing diagram for the 74VHC125 showing the relationship between the Output Enable (OE) signal and the Output (A, B) signals during transitions to and from the high-impedance state (Off).

The diagram illustrates the following parameters and states:

- Output Enable (OE):** A square wave signal. The rise time (t_r) and fall time (t_f) are both 2.5 ns. The signal transitions from 3.0 V to GND.
- Output (A, B) Low to Off to Low:** Shows the output voltage during the transition from a low state to a high-impedance state (Off) and back to a low state. The output voltage is 1.5 V during the high-impedance state. The transition from low to off is labeled t_{PLZ} and from off to low is labeled t_{PZL} . The output voltage during the low state is $V_{OL} + 0.3\text{ V}$.
- Output (A, B) High to Off to High:** Shows the output voltage during the transition from a high state to a high-impedance state (Off) and back to a high state. The output voltage is 1.5 V during the high-impedance state. The transition from high to off is labeled t_{PHZ} and from off to high is labeled t_{PZH} . The output voltage during the high state is $V_{OH} - 0.3\text{ V}$.
- Timing Parameters:**
 - t_r : Rise time of OE (2.5 ns)
 - t_f : Fall time of OE (2.5 ns)
 - t_{PLZ} : Propagation delay from OE low to output low-to-off
 - t_{PHZ} : Propagation delay from OE low to output high-to-off
 - t_{PZL} : Propagation delay from OE high to output off-to-low
 - t_{PZH} : Propagation delay from OE high to output off-to-high
- Output States:**
 - Outputs enabled:** The output is in a low or high state.
 - Outputs disabled:** The output is in a high-impedance state (Off).
 - Outputs enabled:** The output is in a low or high state.

$V_{OH} - V_{CC}$ Characteristics (typ.)

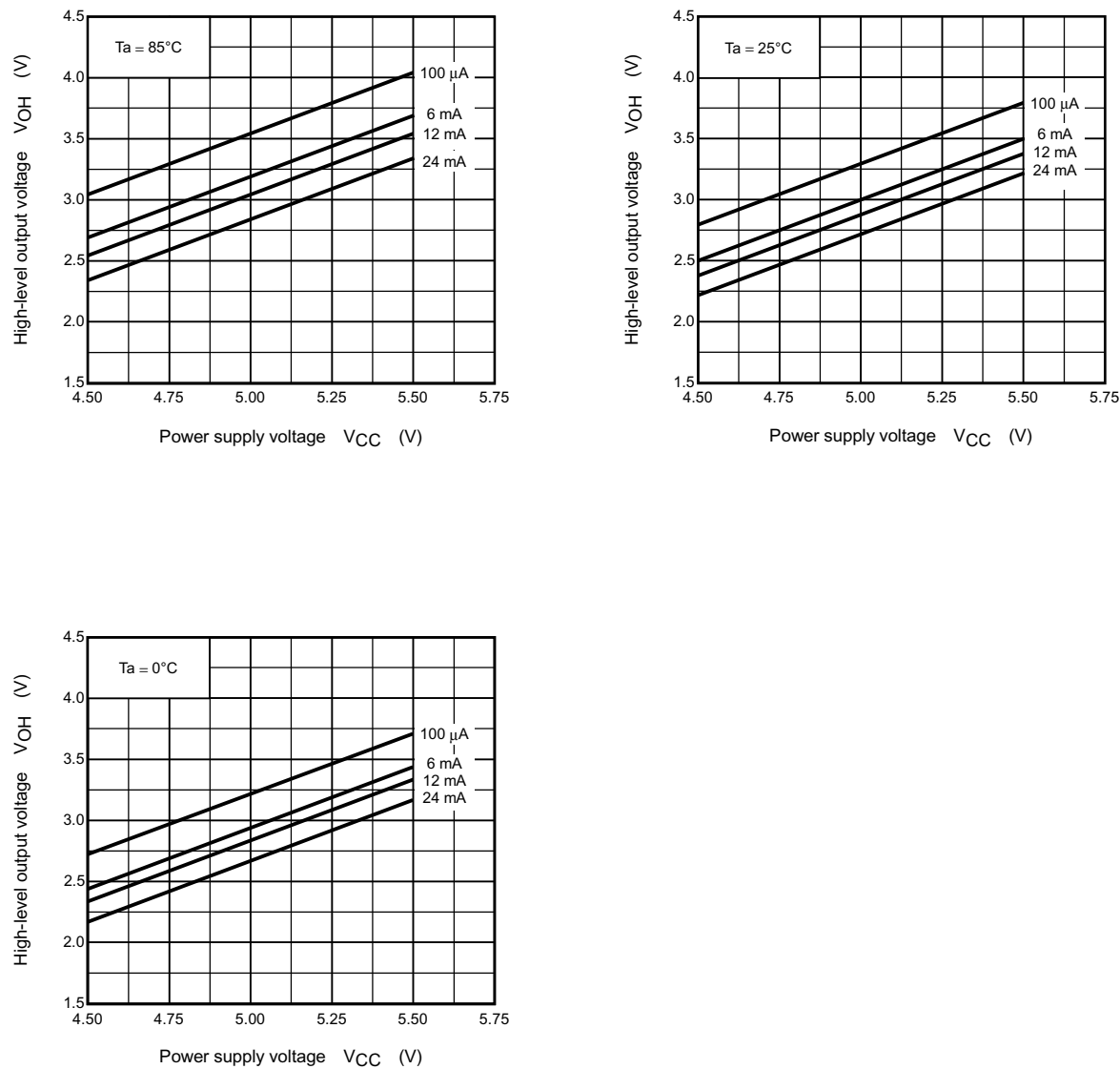
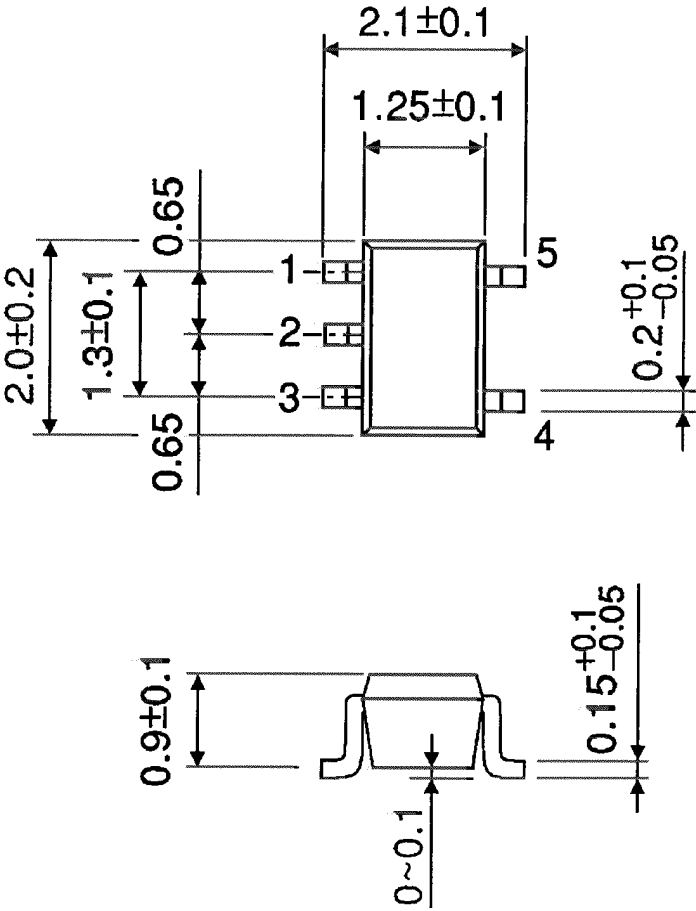


Figure 4

Package Dimensions

SSOP5-P-0.65A

Unit : mm



Weight: 0.006 g (typ.)