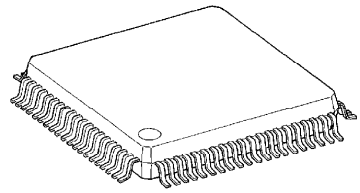
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9328AF

PORTABLE AUDIO DTS CONTROLLER (DTS-21)

The TC9328AF is a single-chip DTS microcontroller for portable audio incorporating 230 MHz prescaler, PLL, and LCD driver. In addition to a 20-bit IF counter, 6-bit A / D converter, serial interface, and buzzer function, the device supports an interrupt function, 8-bit timer / counter, and 8-bit pulse counter. The LCD driver features built-in 1 / 4 duty, 1 / 2 bias and a 3 V voltage doubler boosting circuit, implementing stable LCD.
The power supply voltage ranges from 0.9 to 1.8 V. Because of its low-current consumption (CPU : 80 μA (max)), the device is suitable for use in digital tuning systems in portable equipment such as headphone stereos.



LQFP80-P-1212-0.50A

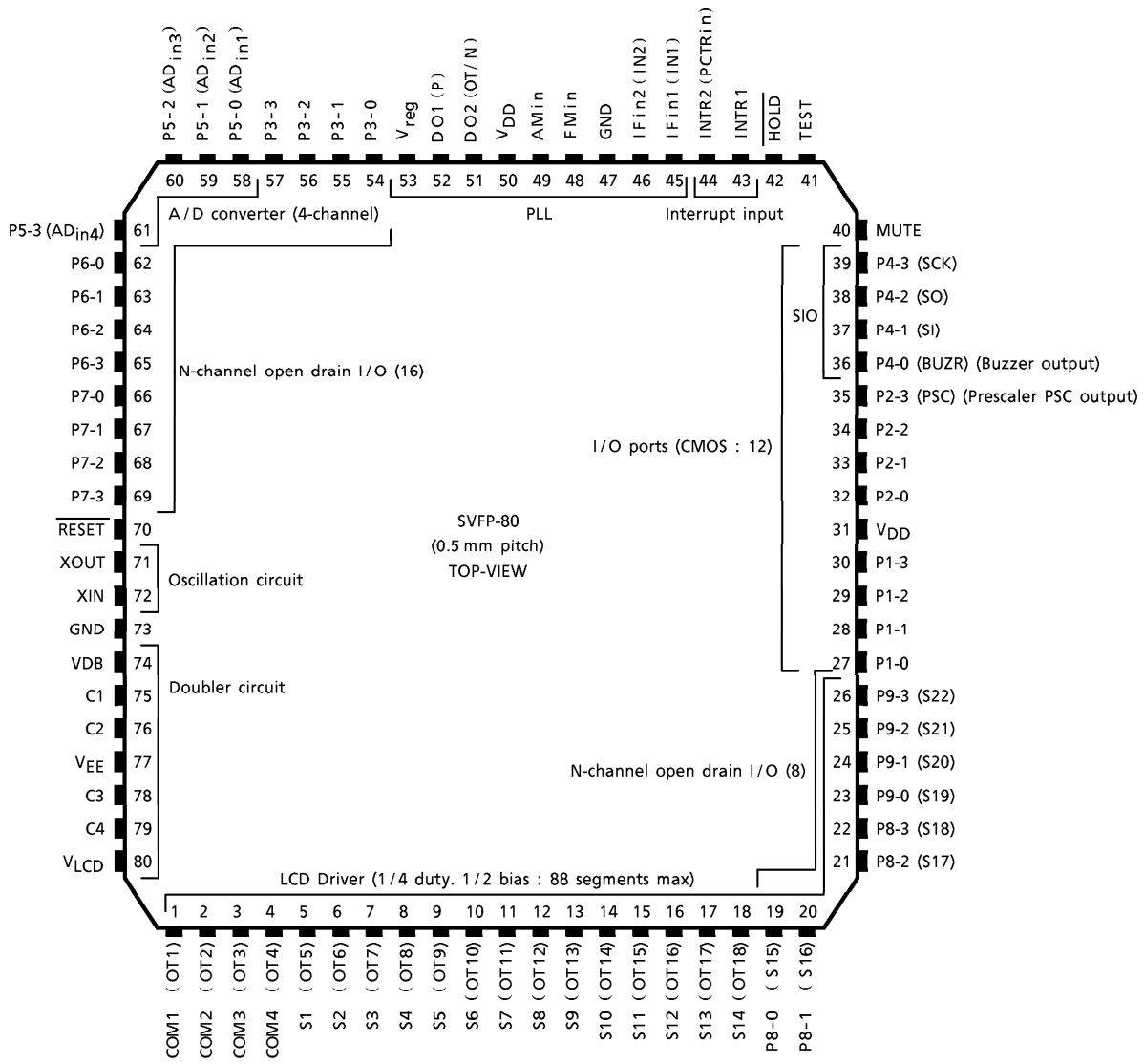
Weight : 0.45 g (Typ.)

FEATURES

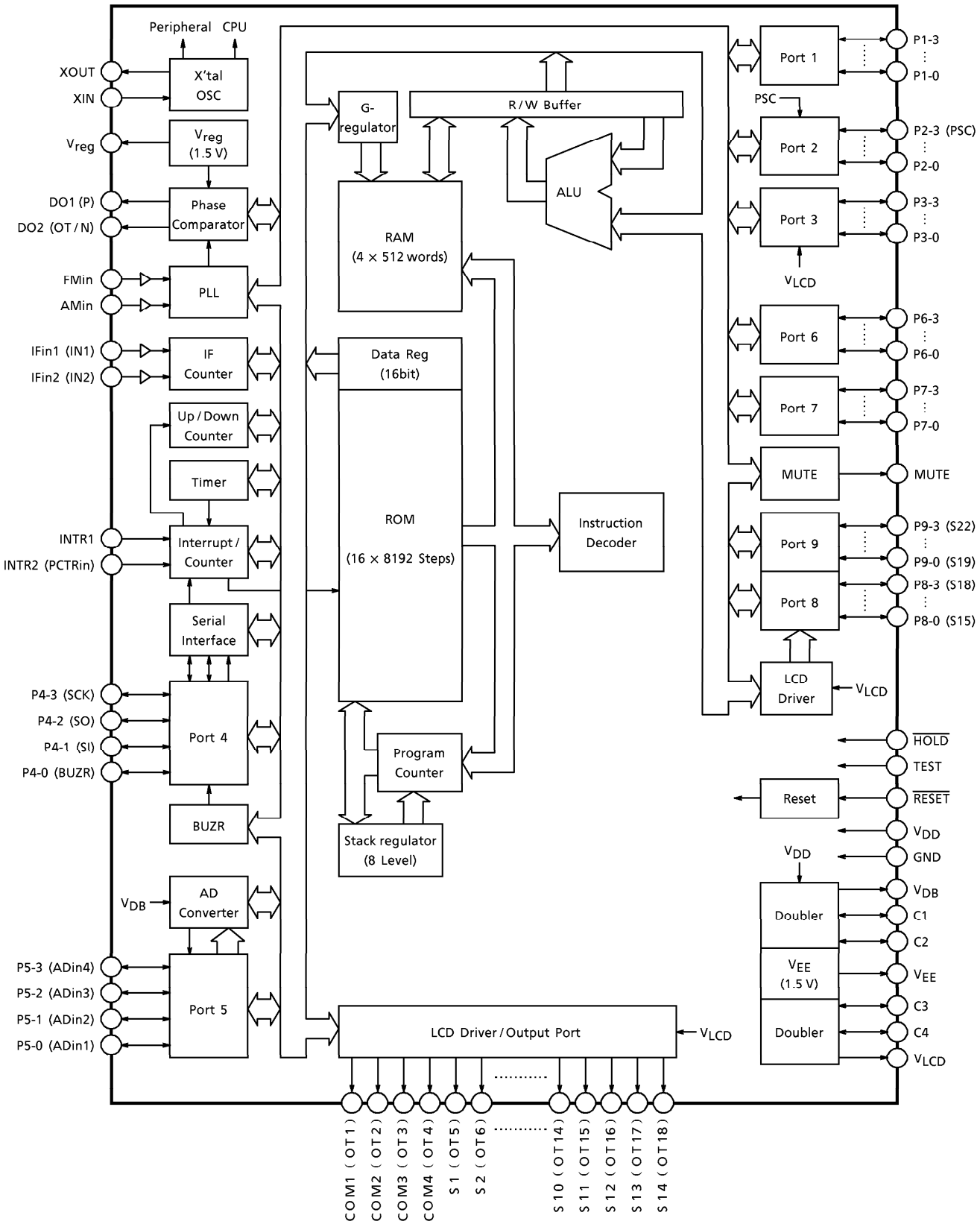
- CMOS DTS microcontroller LSI with built-in 230 MHz prescaler, PLL, and LCD driver
- Operating voltage : V_{DD} = 0.9 to 1.8 V (typ. : 1.5 V)
- Current dissipation : When CPU in operation : I_{DD} = 40 μA (typ.)
  When PLL in operation : I_{DD} = 6 mA (typ.) (VHF mode)
- Operating temperature range : Ta = – 10 to 60°C
- Program memory (ROM) : 16-bit × 8192 steps
- Data memory (RAM) : 4-bit × 512 words
- Instruction execution time : 40 μs
- Crystal oscillator frequency : 75 kHz
- Stack level : 8
- General-purpose IF counter : 20-bit (CMOS input supported)
- A / D converter : 6-bit × 4 channel
- LCD driver : 1 / 4 duty, 1 / 2 bias 88 segments (max.)
- I / O port : CMOS I / O ports : 12
  N-channel open drain I / O ports : 24 (max.)
  Output-only port : 1
  Input-only ports : 5 (max.)
- Timer / counter : 8-bit (as timer clock : INTR1 / INTR2, instruction cycle : 1 kHz selectable)
- Pulse counter : 8-bit up / down counter (input via INTR2 pin)
- Buzzer : Built-in four mode : 0.625 to 3 kHz (8 types), Continuous, Single-Shot, 10 Hz Intermittent, or 10 Hz Intermittent 1 Hz Interval
- Package : QFP-80 (0.5 mm pitch, 1.4 mm thick)

980910EBA2

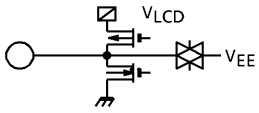
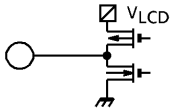
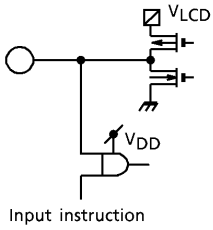
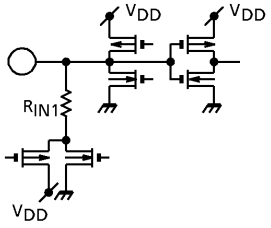
PIN ASSIGNMENT

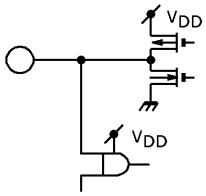
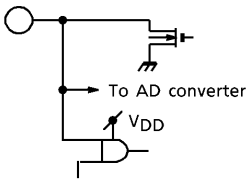


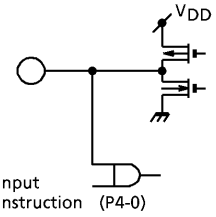
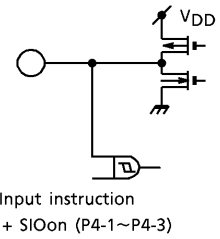
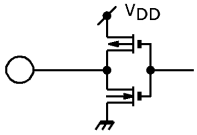
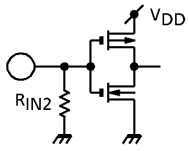
BLOCK DIAGRAM

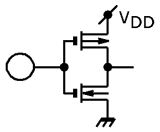


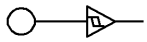
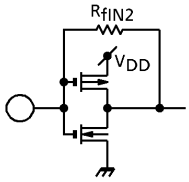
DESCRIPTION OF PIN FUNCTION

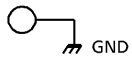
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	COM1 / OT1	LCD common output / Output port	Output common signals to LCD panels. Through a matrix with pins S1 to S22, a maximum 88 segments can be displayed. Three levels, V_{LCD}, V_{EE}, and GND, are output at 62.5 Hz every 2 ms. V_{EE} is output after system reset and CLOCK STOP are released, and a common signal is output after the DISP OFF bit is set to "0". These pins can be programmed as output ports (Note).	
2	COM2 / OT2			
3	COM3 / OT3			
4	COM4 / OT4			
5~18	S1 / OT5 ~ S14 / OT18	LCD segment output / Output port	Segment signal output terminals for LCD panel. Together with COM1 to COM4, a matrix is formed that can display a maximum of 88 segments. All pins from S1 to S14 can be programmed as output ports (Note), and all pins from S15 to S22 as I / O ports, in units of pins. When the pins function as output ports, V_{LCD} pin potential and GND potential are output to them. When the pins function as I / O ports, drain output is N-ch open. Because power is supplied from V_{LCD} for the I / O ports, up to V_{LCD} voltage (3 V) can be applied. These data ports (OT1 to OT18) are incremented by 1 by instruction every time data are accessed. Therefore, they can be used for external memory address signals, facilitating data access. (Note) : After system reset, the output port pins are set to LCD output, the I / O port pins to I / O port input.	
19~26	P8-0 / S15 ~ P9-3 / S22	LCD segment output / I / O port		
27~30	P1-0~P1-3	I / O port 1	The input and output of these 4-bit I / O ports can be programmed in 1-bit units. These pins can be programmed to be pulled up or down. Thus, they can be used as key input pins. By altering the input of I / O ports set to input, the CLOCK STOP mode or the WAIT mode can be released, and the MUTE bit of the MUTE pin can be set to "1".	

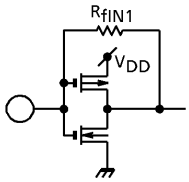
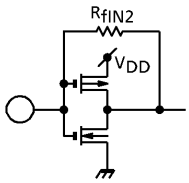
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
32~34	P2-0~P2-2	I/O port 2	The input and output of these 4-bit I/O ports can be programmed in 1-bit units. The P2-3 pin is also used as a PLL prescaler PSC signal output pin. A PLL can be configured using an external prescaler. In such a case, set the pin to I/O port output.	 Input instruction
35	P2-3 / PSC	I/O Port 2 / Prescaler / PSC Output		
54~57	P3-0~P3-3	I/O port 3	4-bit I/O ports, allowing input and output to be programmed in 1 bit units. Pins P5-0 to P5-3 can also be used for analog input to the built-in 6-bit, 4-channel AD converter. The conversion time of the built-in AD converter using the successive comparison method is 280 μs. The necessary pin can be programmed to AD analog input in 1-bit units. Up to the doubled voltage V_{DB} (V_{DD} × 2) can be input as the AD input voltage. The I/O ports are N-ch open drain output. Up to the V_{DB} voltage can be applied to the AD input pins, and up to 3.6 V can be applied to the I/O port pins. I/O port 3 can obtain N-ch high-output current (2 mA typ.) even at low voltage. The AD converter and all associated controls are performed via sortware.	 Input instruction
58~61	P5-0 / AD_{in1} ~ P5-3 / AD_{in4}	I/O port 5 / AD analog voltage input		
62~69	P6-0~P7-3	I/O port 6, 7		

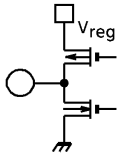
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
36~39	P4-0 / BUZR P4-1 / SI P4-2 / SO P4-3 / SCK	I / O port 4 / Buzzer output / Serial data input / Serial data output / Serial clock I / O	4-bit I / O ports, allowing input and output to be programmed in 1-bit units. The P4-0 pin is also used for buzzer output. P4-1 to P4-3 are also used as serial interface circuit (SIO) input / output pins. The buzzer output can select 8 kinds of 0.625 to 3 kHz frequencies with 4 modes : continuous output, single-shot output, 10 Hz intermittent output, and 10 Hz intermittent 1 Hz interval output. SIO functions for 4-bit or 8-bit serial data inputs from the SI pin and outputs from the SO pin at the SCK pin clock edge. The clock for serial operation (SCK) is capable of internal (SCK = 37.5 kHz) / external options and rise / fall shift options. The SO pin is also capable of switching to serial inputs (SI), facilitating the control of various LSI's and communication between controllers. When SIO interrupts are enabled, an interrupt is generated after SIO execution and the program jumps to address 4. This is useful for high-speed serial communications. All SIO inputs use built-in Schmitt circuits. P3-3 pins also functions as the output for a built-in buzzer. SIO, buzzer, and all associated controls can be programmed.	 
40	MUTE	Muting output port	1-bit output port, normally used for muting control signal output. This pin can set the internal MUTE bit to "1" according to a change in the input of I / O port 1 and $\overline{\text{HOLD}}$. MUTE bit output logic can be changed.	
41	TEST	Test mode control input	Input pin used for controlling TEST mode. "H" (high) level indicates TEST mode, while "L" (low) indicates normal operation. The pin is normally used at low level or in NC (no connection) state. (A pull-down resistor is builtin).	

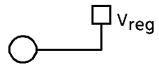
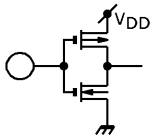
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
42	$\overline{HOLD}$	Hold mode control input	Input pin for request / release hold mode. Normally, this pin is used to input radio mode selection signals or battery detection signals. Hold mode includes CLOCK STOP mode (stops crystal oscillation) and WAIT mode (halts CPU). Setting is implemented with the CKSTP instruction or the WAIT instruction. To request Clock Stop mode, either L-level detection on the $\overline{HOLD}$ pin or forced execution can be programmed. The mode is released by H-level detection on the $\overline{HOLD}$ pin or input change, respectively. Executing the CKSTP instruction stops the clock generator and the CPU, entering memory backup state. In memory backup state, current dissipation becomes low (1 mA or less) and the display output / CMOS output ports automatically become L level and N-ch open drain output Off. Regardless of this input state, Wait mode is executed in order to lower power dissipation. Either crystal oscillator only in operation or CPU suspension can be programmed. For crystal oscillator only in operation, all displays are at L level and other pins are in hold state. For CPU suspension, the CPU stops and all others retain their states. Wait mode is released by changing $\overline{HOLD}$ input.	

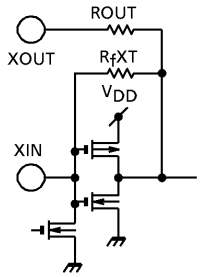
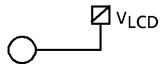
PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
43 44	INTR1 INTR2 / PCTRin	External interrupt input / Pulse counter input	External interrupt input pins. When interrupts are enabled and a 13.3~ 26.7 ms pulse or longer is input to the pin, interrupt INTR1 / 2 is generated and the program jumps to address 1 / 2. Input logic or rising / falling edge can be selected for each input interrupt. The internal 8-bit timer clock input can be selected as input to the pins. When the count value reaches the specified value, an interrupt is generated (address 3). The pin is also used for input of an 8-bit pulse counter. Input rising / falling or upcount / downcount can be selected for the counter. These inputs use built-in Schmitt circuits. The pins can also be used as input ports for input of remote control signals or a tape count.	
45 46	IFin1 / IN1 IFin2 / IN2	IF signal input / Input port	IF signal input pin for the IF counter to count the IF signals of the FM and AM bands and to detect the automatic stop position. The input frequency is between 0.3~ 12 MHz (0.2 $V_{p\text{-}p\ min}$). A built-in input amp. and C coupling allow operation at low-level input. The IF counter is a 20-bit counter with optional gate times of 1, 4, 16 and 64 ms. 20 bits of data can be readily stored in memory. In Manual mode, gate On / Off can be performed using instruction. The input pin can be programmed for use as an input port (IN port). (Note) : When a pin is set to IF input, the input is at high impedance in PLL Off mode or if the pins are not used for input.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
31, 50	V_{DD}	Power-supply pins	Pins to which power is applied. Normally, V_{DD} = 0.9~1.8 V is applied. For the PLL, power for the prescaler in the programmable counter block and IF input amp can be individually programmed. By switching to different modes depending on the power supply voltage and the frequency used, current dissipation can be lowered. In backup state (at execution of the CKSTP instruction), current dissipation drops (1 mA or less) and the power supply voltage can be reduced to 0.75 V. If more than 0.9 V is applied when the pin voltage is 0, the device system is reset and the program starts from address "0". (Power on reset) (Note) : To operate the power on reset, the power supply should start up in 10~100 ms. (Note) : The power-on reset function can be enabled / disabled using the AI switch.	
47, 73	GND			

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
48	FMin	FM local oscillation signal input	Programmable counter input pin for FM / AM band. For FM input, mode can be switched between 1 / 2 + Pulse Swallow VHF and FM mode. For AM input, mode can be switched between Pulse Swallow (HF) and Direct Dividing (LF) mode. Normally, local oscillation output (Voltage-Controlled Oscillator : VCO output) of 50~230 MHz is input in VHF mode ; 30~130 MHz in FM mode ; 1 to 30 MHz in HF mode ; 0.5~8 MHz in LF mode. A PLL can be configured using an external prescaler. In such a case, set the pin to LF, and connect the prescaler divider output to the AMin input pin and the PSC input to the P2-3 (PSC) output pin. With an input amp incorporated, capacitive-coupling, small-amplitude operation. (Note) : The input is at high impedance in PLL Off mode or if the pins are not used for input.	
49	AMin	AM local oscillation signal input		

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
52 51	DO1 / P DO2 / OT / N	Phase comparator output / output port / P output Phase comparator output / output port / N output	PLL phase comparator output pins. Tristate output. When the program counter divider output is higher than the reference frequency, H level is output ; when lower, L level ; and when they match, high impedance. For the phase comparator power supply, a 1.5 V constant voltage supply (Vreg pin) is used. Even if the power supply voltage drops, a stable PLL can be configured. Because DO1 and DO2 are output in parallel, a filter constant can be optimally designed for each FM / AM band. The DO2 pin can be programmed to high impedance or as an output port (OT). Therefore, using the DO1 and DO2 pins, lockup time can be improved or the pins can be effectively used as output ports. Also, the phase comparator charge pump control signal (P / N) can be output from the DO1 / 2 pin by program so a PLL using an external charge pump can be configured. In such a case, when the program counter divider output is higher than the reference frequency, P / N is output at H / L level ; when lower, L / H level ; and when they match, L / L level. When set to this mode, H level output becomes V_{DD} level. (Note) : For tristate output, the H level output uses a constant voltage supply. When H level output current is required, Toshiba recommend using an external power supply.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
53	V_{reg}	Phase comparator constant voltage supply	Phase comparator constant voltage supply. When the phase comparator output is tristate output, a constant voltage supply of 1.5 V (typ.) is output to the pin. For this output, connect a stabilizing capacitor (0.47 mF typ.). At constant voltage operation, the H level phase comparator output uses a constant voltage. Thus, when H level output current is required, Toshiba recommend using an external power supply. In such a case, externally apply 1.8~3.6 V to the pin. When the phase comparator output is output using the charge pump control signal (P / N), the pin becomes the V_{DD} level. Then, the phase comparator output operates using the power supply voltage.	
70	$\overline{RESET}$	Reset input	Input pin for system reset signals. $\overline{RESET}$ takes place while at low level; at high level, the program starts from address "0". Normally, if more than 0.9 V is supplied to V_{DD} when the voltage is 0, the system is reset (power on reset). Accordingly, this pin should be set to high level during operation. (Note) : When the power-on reset function is enabled / disabled using the AI switch, reset by pin.	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	
71	XOUT	Crystal oscillator pin	Crystal oscillator pins. A reference 75 kHz crystal resonator is connected to the X_{IN} and X_{OUT} pins. (Ci = Co = 15 pF) The oscillator stops oscillating during CKSTP instruction execution. The V_{XT} pin is the power supply for the crystal oscillator. A stabilizing capacitor (0.47 μF typ.) is connected.	
72	XIN			
74	V_{DB}	Voltage doubler boosting output pins	Voltage doubler boosting output pins. The V_{DB} pin doubles the V_{DD} pin voltage using the voltage doubler boosting capacitor between C1 and C2. The doubled voltage is used for the AD converter and constant voltage circuit (Vreg, V_{EE}) power supply. The V_{EE} pin supplies a constant voltage of 1.5 V from the V_{DB} voltage. The voltage is doubled (to 3 V) using the voltage doubler boosting capacitor between C3 and C4. The doubled voltage is then supplied to the V_{LCD} pin. The V_{EE} potential and the V_{LCD} potential are used to drive the LCD. Connect a stabilizing capacitor between the V_{DB} pin and GND (0. 1 mF, 10 mF typ.), and between the V_{LCD} pin and GND (0.1 mF typ.). Connect a voltage doubler boosting capacitor (0.1 mF typ.) between C1 and C2, and between C3 and C4. (Note 1)	
75	C1			
76	C2			
77	V_{EE}			
78	C3			
79	C4			
80	V_{LCD}			

(Note 1) : When the LCD pin is set as an output port, the H level output is the doubled voltage V_{LCD}. Therefore, disconnect the voltage doubler boosting capacitor but connect the V_{LCD} pin to the V_{DD} pin.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3~4.0	V
Voltage Doubler Boosting Voltage	V_{DB}	−0.3~4.0	V
Output Voltage 1 (N-channel Open Drain)	V_{O1} (Note)	−0.3~4.0	V
Output Voltage 2 (N-channel Open Drain)	V_{O2} (Note)	−0.3~V_{DB} + 0.3	V
Output Voltage 3 (N-channel Open Drain)	V_{O2} (Note)	−0.3~V_{LCD} + 0.3	V
Input Voltage	V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	P_D	100	mW
Operating Temperature	T_{opr}	−10~60	°C
Storage Temperature	T_{stg}	−65~150	°C

(Note) : V_{O1} : P3-0~P3-3, P6-0~P6-3, P7-0~P7-3 pin
V_{O2} : P5-0~P5-3 pin
V_{O3} : P8-0~P8-3, P9-0~P9-3 pin

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta = 25°C, V_{DD} = 3.0 V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Range Of Operating Supply Voltage	V_{DD1}	—	Under CPU operation (*)	0.9	~	1.8	V
	V_{DD2}		Under PLL operation (*)	0.9	~	1.8	
Range Of Memory Retention Voltage	V_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed) (*)	0.75	~	1.8	
Operating Current	I_{DD1}	—	PLL operation (VHF mode) at input FMin = 230 MHz	—	6	10	mA
	I_{DD2}	—	Under CPU operation only (PLL off, display turned on)	—	40	80	μA
	I_{DD3}	—	Hard Wait mode (crystal oscillator operating only)	—	20	40	
	I_{DD4}	—	Soft Wait mode (CPU stopped, PLL off)	—	30	—	
Memory Retention Current	I_{HD}	—	Crystal oscillation stopped (CKSTP instruction executed)	—	0.1	1.0	
Crystal Oscillation Frequency	f_{XT}	—	(*)	—	75	—	kHz
Crystal oscillation Start-up Time	t_{ST}	—	Crystal oscillation f_{XT} = 75 kHz	—	—	1.0	s

For conditions marked by an asterisk (*), guaranteed when V_{DD} = 0.9~1.8 V, Ta = −10~60°C

VOLTAGE DOUBLER BOOSTING CIRCUIT

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Doubled Voltage	V_{DB}	—	GND reference (V_{DB})	—	V_{DD} × 2	—	V
Doubled voltage output current	I_{DB}	—	V_{OH} = V_{DB} − 0.1 V (V_{DB})	− 50	− 200	—	μA
Doubled voltage reference voltage	V_{EE}	—	GND reference (V_{EE})	1.35	1.50	1.65	V
Constant voltage for phase comparator	V_{reg}	—	GND reference (V_{reg})	1.35	1.50	1.65	
Constant voltage temperature characteristic	Dv	—	GND reference (V_{DD}, V_{reg})	—	− 5	—	mV / °C
Power supply output current for phase comparator	I_{reg}	—	V_{OH} = V_{reg} − 0.1 V (V_{reg}) (Note 1)	− 50	− 200	—	μA
Doubled voltage	V_{LCD}	—	GND reference (V_{LCD})	2.7	3.0	3.3	V
Doubled voltage output current	I_{LCD}	—	V_{OH} = V_{LCD} − 0.1 V (V_{LCD}) (Note 1)	− 50	− 200	—	μA

(Note 1) : The "H" level output current of the pin using the V_{reg} / V_{LCD} power supply must not exceed the power supply (doubled voltage : V_{DB}) output current.

PROGRAMMABLE COUNTER / IF COUNTER OPERATING FREQUENCY RANGE

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
FMin (VHF mode)	f VHF	—	V_{IN} = 0.1 V_{p-p} (*)	50	~	230	MHz
FMin (FM mode)	f FM	—	V_{IN} = 0.1 V_{p-p} (*)	30	~	130	
AMin (HF mode)	f HF1	—	V_{IN} = 0.1 V_{p-p} (*)	3.0	~	30	
	f HF2	—	V_{IN} = 0.1 V_{p-p} (*)	1.0	~	10	
AMin (LF mode)	f LF	—	V_{IN} = 0.1 V_{p-p} (*)	0.5	~	8	
IFin1, IFin2	f IF	—	V_{IN} = 0.1 V_{p-p} (*)	0.3	~	12	
PSC transfer delay time	tpd	—	(PSC) C_L = 15 pF, V_{DD} = 1.1~1.8 V (*)	—	—	400	ns

PROGRAMMABLE COUNTER / IF COUNTER INPUT AMPLITUDE RANGE

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
FMin (VHF mode)	V VHF	—	Same as for f VHF (*)	0.1	~	0.6	V_{p-p}
FMin (FM mode)	V FM	—	Same as for f FM (*)	0.1	~	0.6	
AMin (HF mode)	V HF	—	Same as for fHF1~2 (*)	0.1	~	0.6	
AMin (LF mode)	V LF	—	Same as for f LF (*)	0.1	~	0.6	
IFin1, IFin2	V IF	—	Same as for f IF (*)	0.1	~	0.6	

(*) : Guaranteed when V_{DD} = 0.9~1.8 V, Ta = − 10~60°C.

LCD COMMON OUTPUT / SEGMENT OUTPUT (COM1~COM4, S1~S22)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Current	"H" Level	IOH1	—	V_{LCD} = 3 V, V_{OH} = V_{LCD} − 0.3 V (COM1~COM4)	−0.10	−0.20	—	mA
		IOH2	—	V_{LCD} = 3 V, V_{OH} = V_{LCD} − 0.3 V (S1~S22)	−0.05	−0.10	—	
	"L" Level	IOL1	—	V_{LCD} = 3 V, V_{OL} = 0.3 V (COM1~COM4)	0.10	0.30	—	
		IOL2	—	V_{LCD} = 3 V, V_{OL} = 0.3 V (S1~S22)	0.05	0.15	—	
Output Voltage 1/2 Level		VBS	—	No load (COM1~COM4)	1.35	1.5	1.65	V

OUTPUT PORT, I/O PORT (OT1~OT18, P8-0~P8-3, P9-0~P9-3)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Current	"H" Level	IOH3	—	V_{LCD} = 3 V, V_{OH} = V_{LCD} − 0.3 V (Note1, except I/O port)	−1.5	−3.0	—	mA
	"L" Level	IOL3	—	V_{LCD} = 3 V, V_{OL} = 0.3 V	1.5	3.0	—	
Input Leak Current		ILI	—	V_{IH} = V_{LCD} V_{IL} = 0 V (P8-0~P8-3, P9-0~P9-3)	—	—	±1.0	μA
Input Voltage	"H" Level	V_{IH}	—	(P8-0~P8-3, P9-0~P9-3)	V_{DD} × 0.8	~	V_{DD}	V
	"L" Level	V_{IL}	—	(P8-0~P8-3, P9-0~P9-3)	0	~	V_{DD} × 0.2	

I/O PORT (P1-0~P7-3)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Current	"H" level	IOH4	—	V_{DD} = 1.5 V, V_{OH} = V_{DD} − 0.2 V (I/O port P2, P4)	−0.4	−0.8	—	mA
		IOH5	—	V_{DD} = 0.9 V, V_{OH} = V_{DD} − 0.2 V (I/O port P2, P4)	−0.04	−0.2	—	
	"L" level	IOL4	—	V_{DD} = 1.5 V, V_{OL} = 0.2 V (except I/O port P3)	0.5	1.0	—	
		IOL5	—	V_{DD} = 0.9 V, V_{OL} = 0.2 V (except I/O port P3)	0.1	0.3	—	
		IOL6	—	V_{DD} = 0.9~1.8 V, V_{OL} = 0.2 V (I/O port P3)	1.0	2.0	—	
Input Leak Current		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V (I/O port P1, P2, P4)	—	—	±1.0	μA
			—	V_{IH} = 3.6 V, V_{IL} = 0 V (I/O port P3, P6, P7)	—	—	±1.0	
			—	V_{IH} = V_{DB}, V_{IL} = 0 V (I/O port P5)	—	—	±1.0	
Input Voltage	"H" level	V_{IH}	—	—	V_{DD} × 0.8	~	V_{DD}	V
	"L" level	V_{IL}	—	—	0	~	V_{DD} × 0.2	
Input Pull-down Resistor		RIN1	—	When P1-0~P1-3 are set to pull-down or pull-up	30	60	120	kΩ
SCK Clock External Input Frequency		f_{SIO}	—	When I/O port P4-3 are set to serial clock input	—	—	200	kHz

For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8~3.6 V, Ta = −10~60°C

(Note 1) : The "H" level output current is the current when the pin power supply is fixed. Make sure that pins using V_{reg}/V_{LCD} power supply do not exceed the power supply (doubled voltage : V_{DB}) output current.

MUTE OUTPUT

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Current	"H" level	IOH4	—	V_{DD} = 1.5 V, V_{OH} = V_{DD} − 0.2 V	−0.4	−0.8	—	mA
		IOH5	—	V_{DD} = 0.9 V, V_{OH} = V_{DD} − 0.2 V	−0.04	−0.2	—	
	"L" level	IOL4	—	V_{DD} = 1.5 V, V_{OL} = 0.2 V	0.5	1.0	—	
		IOL5	—	V_{DD} = 0.9 V, V_{OL} = 0.2 V	0.1	0.3	—	

$\overline{HOLD}$, INTR1 / 2, IN1 / 2 INPUT PORT, $\overline{RESET}$ INPUT

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Leak Current		ILI	—	V_{IH} = V_{DD}, V_{IL} = 0 V	—	—	±1.0	μA
Input Voltage	"H" level	VIH3	—	—	V_{DD} × 0.8	~	V_{DD}	V
	"L" level	VIL3	—	—	0	~	V_{DD} × 0.2	

AD CONVERTER (ADin1~ADin4)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Analog Input Voltage Range	VAD	—	ADin1~ADin4	0	~	VDB	V
Resolution	VRES	—	—	—	6	—	bit
Conversion Total Error	—	—	—	—	±0.5	±1.0	LSB
Analog Input Leak	ILI	—	V_{DD} = V_{DB}, V_{IH} = V_{DB}, V_{IL} = 0 V (ADin1~ADin4)	—	—	±1.0	μA

DO1, DO2 OUTPUT

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Output Current	"H" level	IOH4	—	V_{reg} = 1.5 V, V_{OH} = V_{reg} − 0.2 V (Note 1)	−0.4	−0.8	—	mA
	"L" level	IOL4	—	V_{reg} = 1.5 V, V_{OL} = 0.2 V	0.5	1.0	—	
Output Off Leak Current		ITL	—	V_{DD} = 1.5 V, V_{TLH} = 1.5 V, V_{TLL} = 0 V	—	—	±100	nA

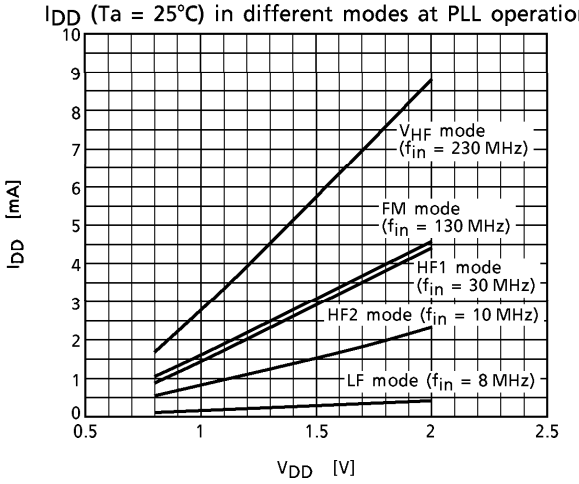
OTHERS

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Input Pull-down Resistance	RIN2	—	(TEST)	5	10	30	kΩ
X_{IN} Amp. Feedback Resistance	RfXT	—	(XIN-XOUT)	—	20	—	MΩ
X_{OUT} Output Resistance	ROUT	—	(XOUT)	—	4	—	kΩ
Input Amp. Feedback Resistance	Rf_{IN1}	—	(FMin)	100	200	400	
	Rf_{IN2}	—	(AMin, IFin1, IFin2)	300	600	1200	

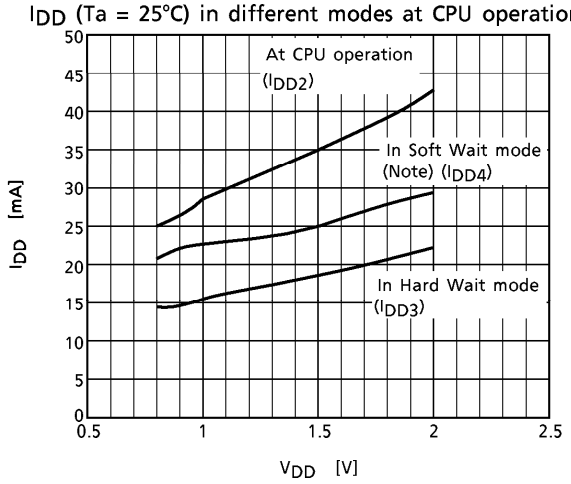
For conditions marked by an asterisk (*), guaranteed when V_{DD} = 1.8 ~ 3.6 V, Ta = – 10~60°C

(Note 1) : The "H" level output current is the current when the pin power supply is fixed. Make sure that pins using V_{reg} / V_{LCD} power supply do not exceed the power supply (doubled voltage : V_{DB}) output current.

Typical TC9328AF product
I_{DD} (Ta = 25°C) in different modes at PLL operation

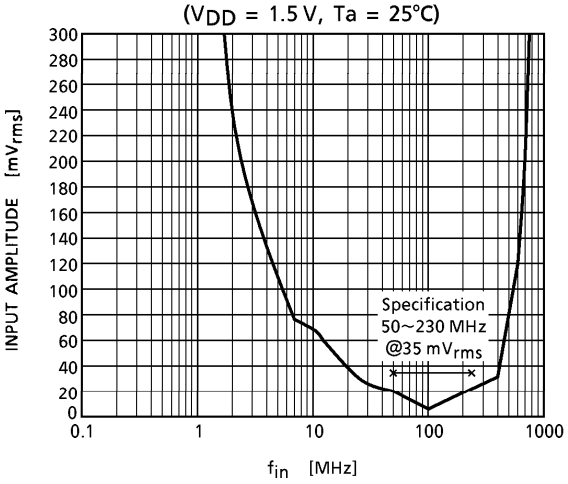


Typical TC9328AF product
I_{DD} (Ta = 25°C) in different modes at CPU operation

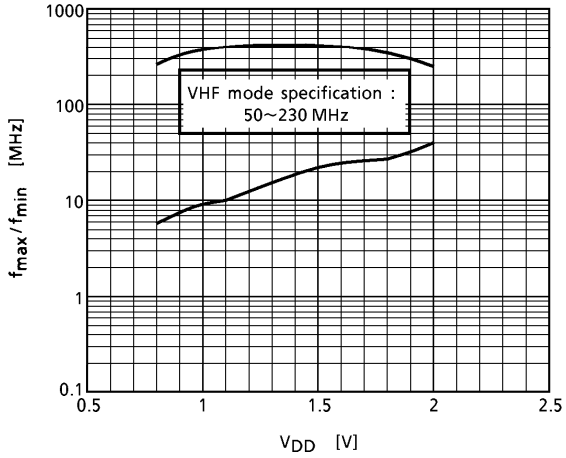


(Note) : The I_{DD} (operating current) in Soft Wait mode is the current dissipation value. The actual current dissipation value differs depending on the CPU execution state.

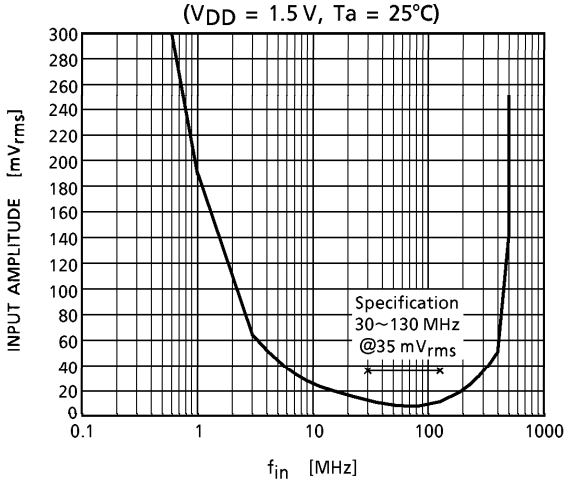
Typical TC9328AF product Input sensitivity VHF mode
(V_{DD} = 1.5 V, Ta = 25°C)



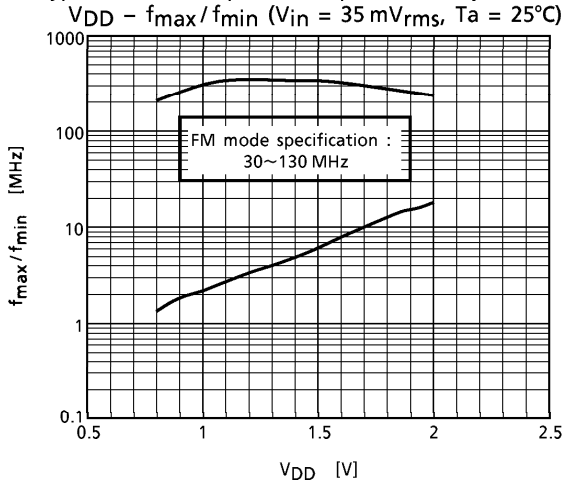
Typical TC9328AF product Input sensitivity VHF mode
V_{DD} – f_{max}/f_{min} (V_{in} = 35 mV_{rms}, Ta = 25°C)



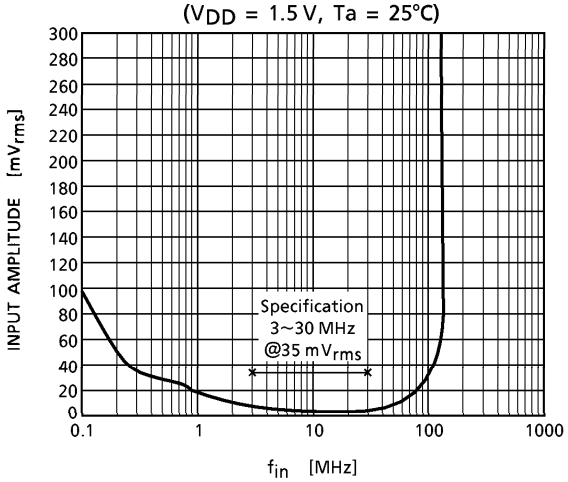
Typical TC9328AF product Input sensitivity FM mode
(V_{DD} = 1.5 V, Ta = 25°C)



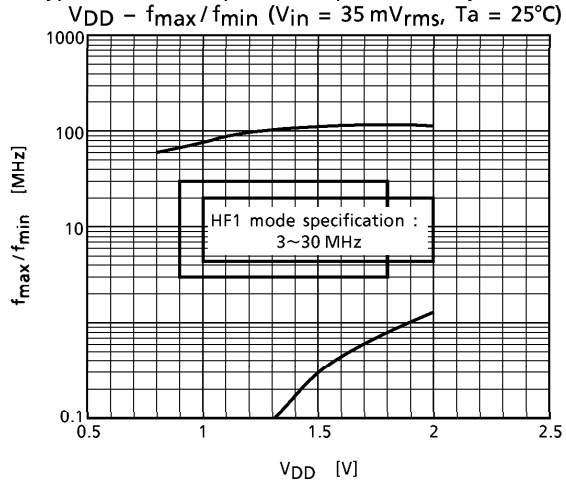
Typical TC9328AF product Input sensitivity FM mode
V_{DD} – f_{max}/f_{min} (V_{in} = 35 mV_{rms}, Ta = 25°C)



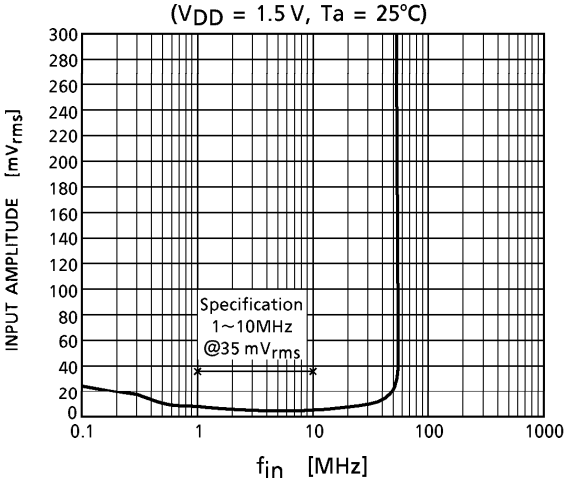
Typical TC9328AF product Input sensitivity HF1 mode
(V_{DD} = 1.5 V, Ta = 25°C)



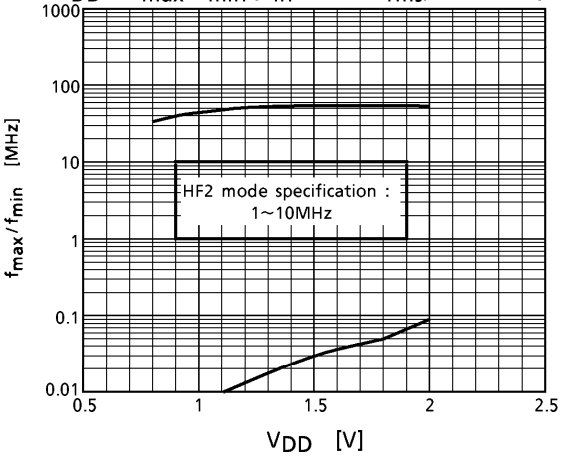
Typical TC9328AF product Input sensitivity HF1 mode
V_{DD} – f_{max}/f_{min} (V_{in} = 35 mV_{rms}, Ta = 25°C)



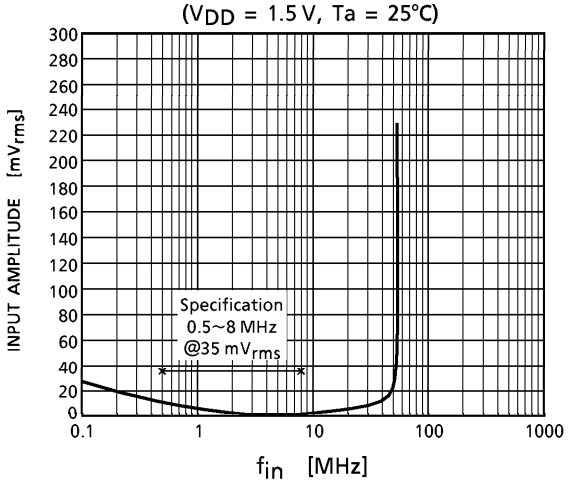
Typical TC9328AF product Input sensitivity HF2 mode
(V_{DD} = 1.5 V, Ta = 25°C)



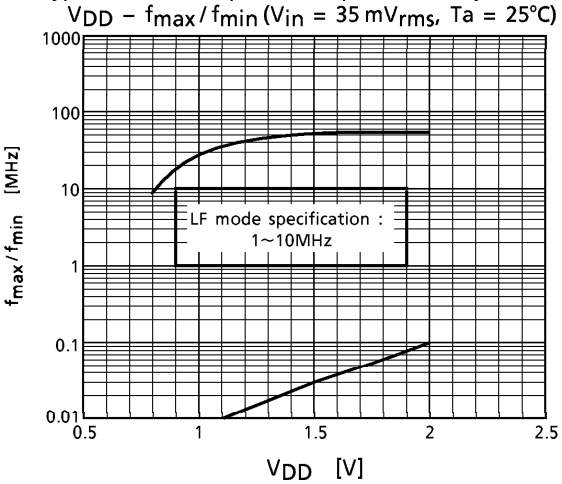
Typical TC9328AF product Input sensitivity HF2 mode
V_{DD} – f_{max} / f_{min} (V_{in} = 35 mV_{rms}, Ta = 25°C)



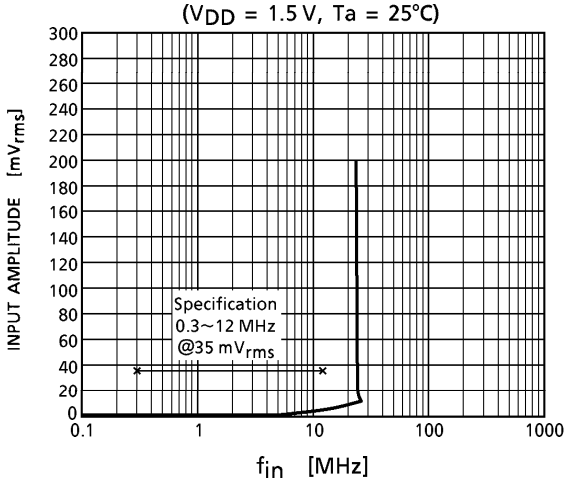
Typical TC9328AF product Input sensitivity LF mode
(V_{DD} = 1.5 V, Ta = 25°C)



Typical TC9328AF product Input sensitivity LF mode
V_{DD} – f_{max} / f_{min} (V_{in} = 35 mV_{rms}, Ta = 25°C)

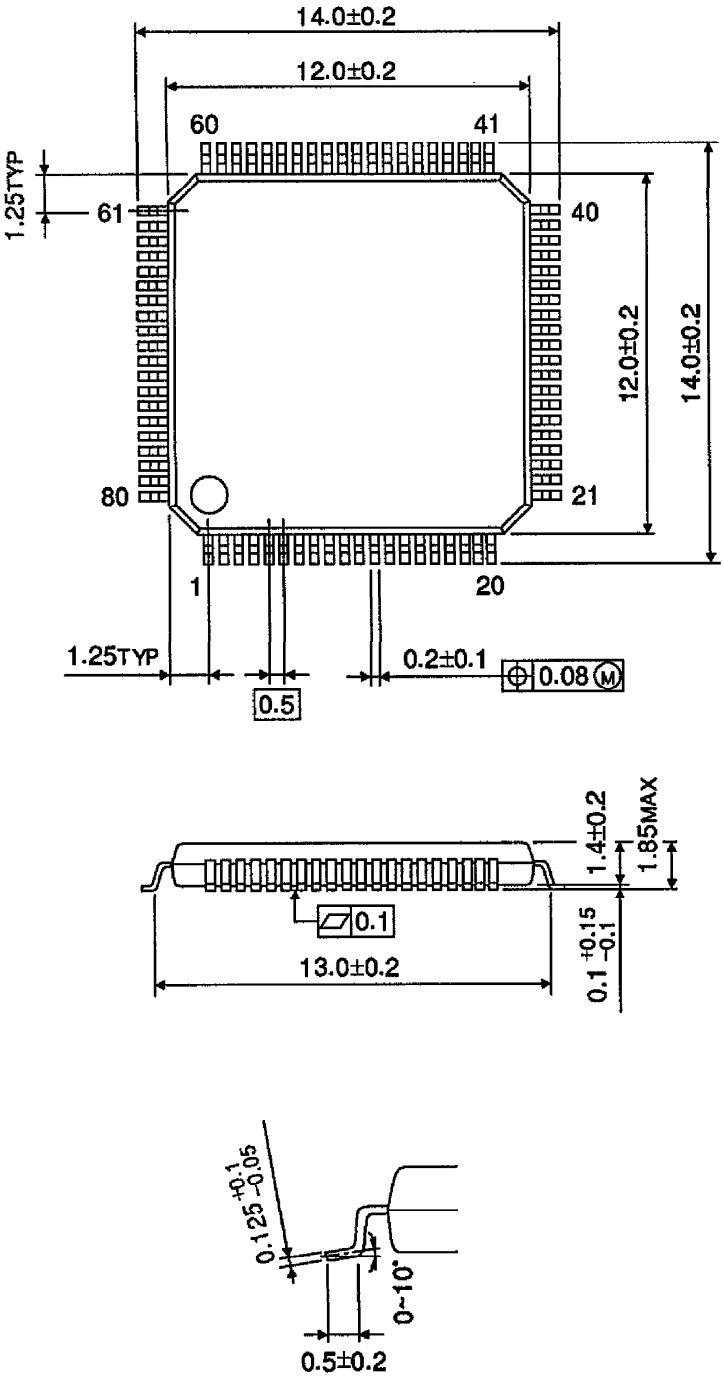


Typical TC9328AF product Input sensitivity IFin mode
(V_{DD} = 1.5 V, Ta = 25°C)



PACKAGE DIMENSIONS

LQFP80-P-1212-0.50A Unit : mm



Weight : 0.45 g (Typ.)