TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6K03A, T6K03B, T6K03C

COLUMN ROW DRIVER LSI FOR DOT MATRIX GRAPHIC LCD

The TOSHIBA T6K03A / B / C is a driver for a small or medium scale dot matrix graphic LCD, especially for reflecting color STN LCD.
This LSI incorporate 65 row output, 128 column output and 65 × 128 × 2bit bit-map display RAM. It has 4 gray-scale function out from 32 gray-scale level using palette function.
The display RAM of this driver is a 2 port RAM so that the access from MPU is as same as general SRAM and has no waiting timing.
It include various power circuit, voltage regulator, voltage divider, Op-amp. contrast control and DC-DC converter (×2, ×3, ×4, ×5).

Unit : mm

T6K03A / B / C	LEAD PITCH	
	IN	OUT
(UBW, 5NS)	0.60	0.23

Please contact with TOSHIBA Agents for each Packaging Outline Dimensions.

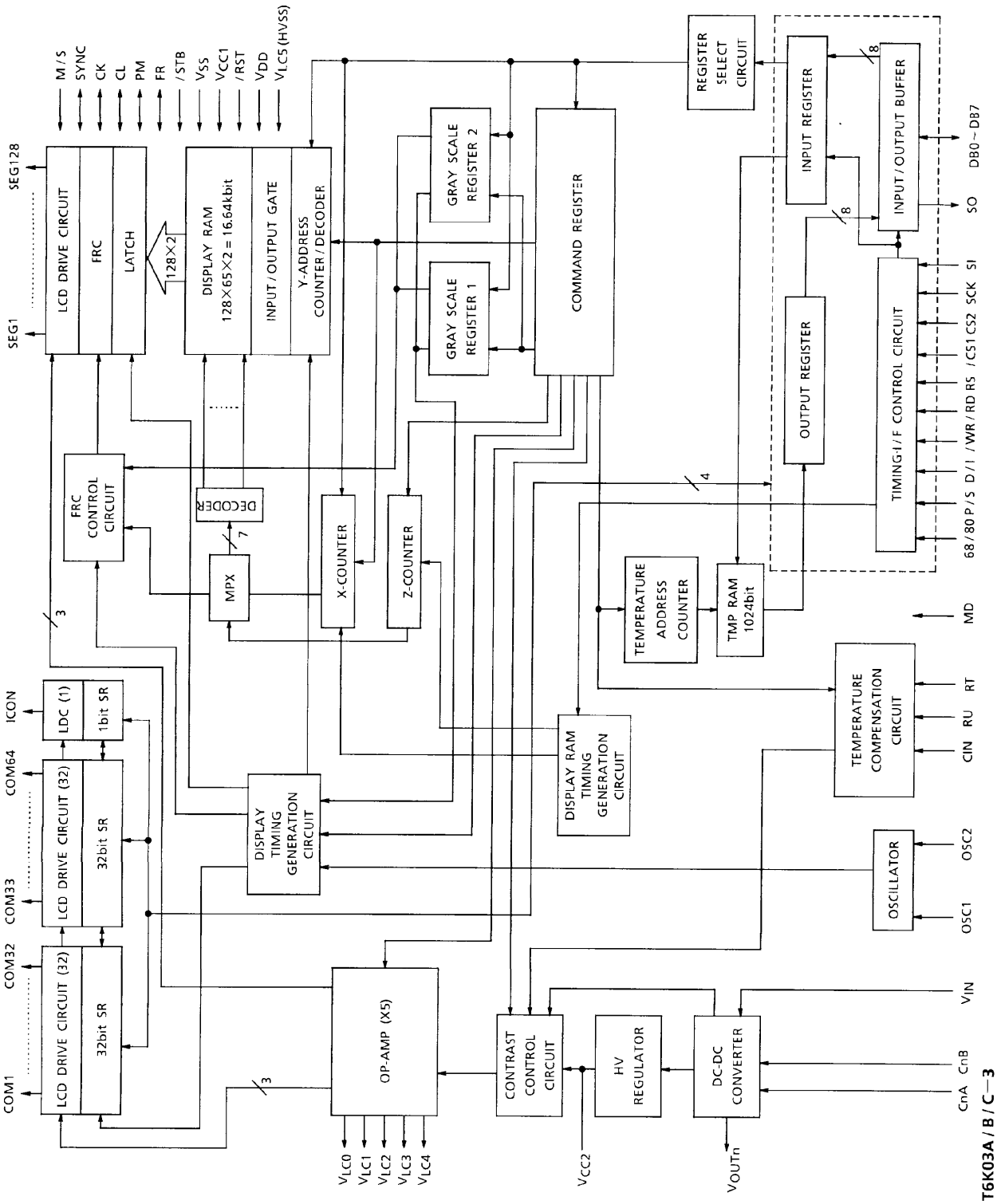
TCP (Tape Carrier Package)

FEATURES

- LCD driver output : 64 row (common) + 128 column (segment) + 128 icons
- Built in display RAM : 65 × 128 × 2 = 16640bit, 2 port RAM
- Gray scale : 4 gray scale selected from 32 gray scale level (palette function)
- Word length : 8bit / word
- Duty cycle : 1 / 2 duty (power save mode)
  1 / 35~1 / 65 duty selectable (normal display mode)

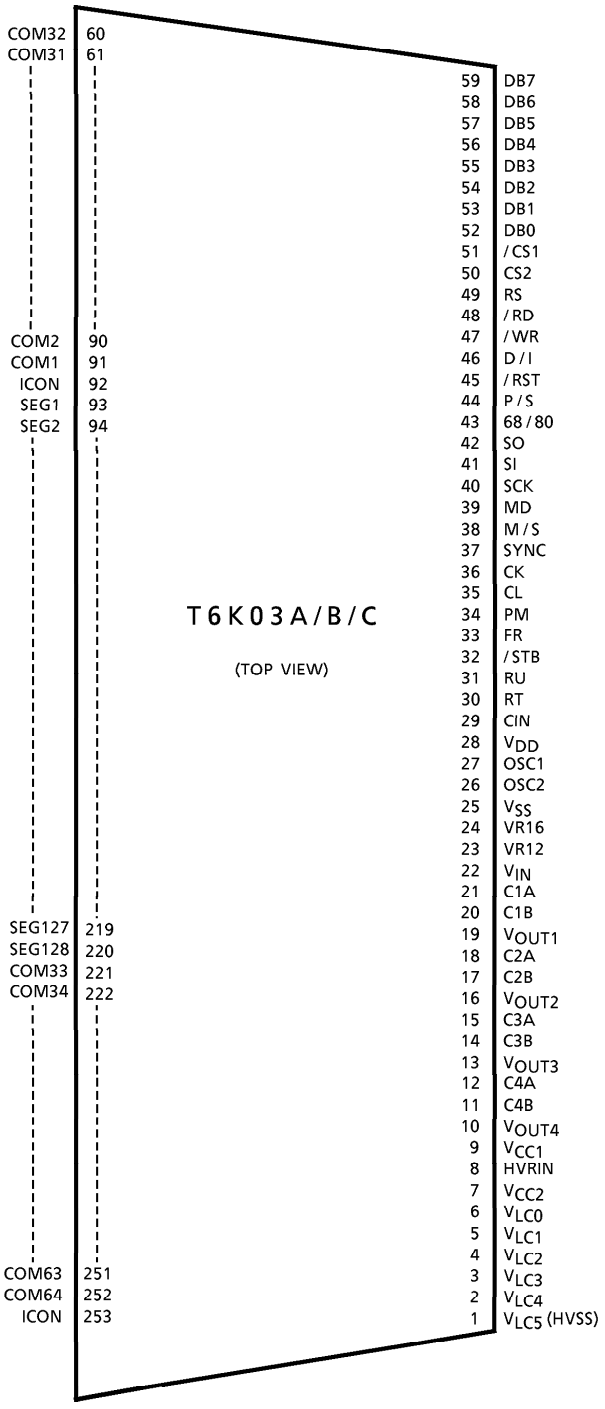
- Power management : Normal mode (Full display)
  Power save mode (Icon display)
  Stand by mode (Clock stop)
- Clock oscillator : CR oscillation
  Low frequency operation – 82kHz oscillation for FR frequency 70Hz (1 / 65 duty)
- Power circuit : Voltage regulator, Voltage divider, Voltage follower Op-amp.
  DC-DC converter (×2, ×3, ×4, ×5), Temperature compensation circuit, Contrast control circuit.
- CPU interface : Interfacing with 68 series and 80 series MPU and Serial Interface
- Logic operation voltage : $V_{DD} = 2.7 \sim 3.3V$
- LCD operation voltage : $V_{CC1, 2} = 6.0 \sim 16.5V$
- CMOS process
- Package : TCP
- Low power consumption: $I_{SS} = 460 \mu A$ (Typ.)
  Condition : $V_{DD} = 3.0V$, using the DC-DC converter (×5), no data access op-amp on, $f_{osc} = 82kHz$ (internal clock), no load, 1 / 65 duty

BLOCK DIAGRAM



T6K03A/B/C-3

PIN CONFIGURATION



(*) Above drawing describes pin configuration of the LSI Chip, it doesn't define the tape carrier package.

PIN FUNCTION (1)

PIN NAME	PIN No.	I/O	FUNCTION
SEG1~128	93~220	O	Column (segment) drive output
COM1~64	60~91 221~252	O	Row (common) driver output
ICON	92, 253	O	Row (common) drive output of icon
DB0~7	52~59	I/O	Data bus
/CS1	51	I	Input for chip select signal Data write : Data write enable at the rising edge of /CS1. Data read : Data read out while /CS1 is in "L" level.
CS2	50	I	Input for chip select signal Data write : Data write enable at the falling edge of CS2. Data read : Data read out while CS2 is in "H" level.
D/I	46	I	Input for Data/Instruction select signal ● D/I = "H" → Indicates that the data of DB0 to DB7 is the display data. ● D/I = "L" → Indicates that the data of DB0 to DB7 is the instruction data.
/WR	47	I	Input for write enable signal ● /WR = "L" → State of select
/RD	48	I	Input for read enable signal ● /RD = "L" → State of select
RS	49	I	Input for register/mode select signal
P/S	44	I	Input for parallel interface/serial interface select signal ● P/S = "H" → Parallel interface is selected. SI and SCK must be connected to V_{DD} or V_{SS}. ● P/S = "L" → Serial interface is selected. DB0 to DB7 must be open. /WR and /RD must connected to V_{DD} or V_{SS}.
68/80	43	I	Input for 68 series MPU/80 series MPU select signal ● 68/80 = "H" → 68 series MPU selected ● 68/80 = "L" → 80 series MPU selected
SO	42	O	Output for serial data
SI	41	I	Input for serial data
SCK	40	I	Input for serial clock
/RST	45	I	Input for reset signal ● /RST = "L" → State of select

PIN FUNCTION (2)

PIN NAME	PIN No.	I/O	FUNCTION
/STB	32	I	Input for standby signal ● Usually connected to V_{DD} ● /STB = "L" → T6K03A/B/C is the state of standby and it can't accept the command or data. Column drive signal and row drive signal is V_{SS} level, and on-chip oscillator is stop.
OSC1, OSC2	26, 27	I/O	When using a internal clock oscillator, connect a resistor between OSC1 and OSC2. When using a external clock, input the clock to OSC1.
V_{IN}	22	—	Power supply for DC-DC converter
CIN	29	I/O	Input for clock of temperature compensation
RU	31	—	Connect with variable resistor
RT	30	—	Connect with thermistor
C1A, C1B	20, 21	—	Connect with capacitance for ×2 mode
V_{OUT1}	19	—	DC-DC converter output terminal (×2 level)
C2A, C2B	17, 18	—	Connect with capacitance for ×3 mode
V_{OUT2}	16	—	DC-DC converter output terminal (×3 level)
C3A, C3B	14, 15	—	Connect with capacitance for ×4 mode
V_{OUT3}	13	—	DC-DC converter output terminal (×4 level)
C4A, C4B	11, 12	—	Connect with capacitance for ×5 mode
V_{OUT4}	10	—	DC-DC converter output terminal (×5 level)
VR12	23	—	LV regulator monitor (Note)
VR16	24	—	Do not connect (V_{DD} is outputted in this terminal)
HVRIN	8	—	Do not connect
V_{CC1}	9	—	Power supply for LCD driver circuit
V_{CC2}	7	—	Power supply for HV regulator monitor (Note)
V_{LC0}~V_{LC5}	1~6	—	Power supply for LCD driver circuit V_{LC5} terminal is connect to V_{SS}.
V_{SS}, V_{DD}	25, 28	—	Power supply for logic circuit. Ground : Reference

(Note) Connect the capacitance between this terminal and V_{SS}.

PIN FUNCTION (3)

PIN NAME	PIN No.	I/O	FUNCTION
MD	39	I	Mode detect pin for Status Read
M/S	38	I	Input for master/slave selects ● M/S = "H" → T6K03A/B/C is master chip ● M/S = "L" → T6K03A/B/C is slave chip
CL	35	I/O	Input/Output for shift clock pulse ● Master mode (M/S = "H") → output ● Slave mode (M/S = "L") → input
PM	34	I/O	Input/Output for frame signal ● Master mode (M/S = "H") → output ● Slave mode (M/S = "L") → input
FR	33	I/O	Input/Output for display synchronous signal ● Master mode (M/S = "H") → output ● Slave mode (M/S = "L") → input
SYNC	37	I/O	Input/Output for grayscale signal data ● Master mode (M/S = "H") → output ● Slave mode (M/S = "L") → input
CK	36	I/O	Input/Output for grayscale signal data ● Master mode (M/S = "H") → output ● Slave mode (M/S = "L") → input

PIN FUNCTION (4)

PS	68/80	INTERFACE TYPE	/CS1	CS2	D/I	RS	/WR	/RD	SO	SI	SCK	DB0 to DB7
H	L	80 series MPU (/CS1)	/CS1	H	A0	A1	/WR	/RD	Open	L/H	L/H	DB0 to DB7
		80 series MPU (CS2)	L	CS2	A0	A1	/WR	/RD	Open	L/H	L/H	DB0 to DB7
	H	68 series MPU	L	H	A0	A1	R/W	E	Open	L/H	L/H	DB0 to DB7
L	L/H	Serial interface	L	H	L/H	L/H	L/H	L/H	SO	SI	SCK	Open

FUNCTION OF EACH BLOCK

- Interface logic

  The T6K03A / B / C can be operated with 80 series MPUs or 68 series MPUs and Serial Interface. Fig.1 shows an example of interface.

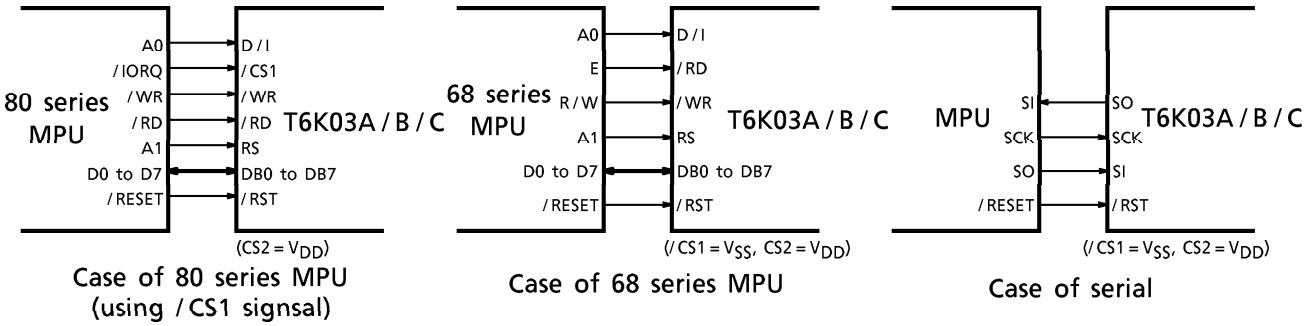


Fig.1

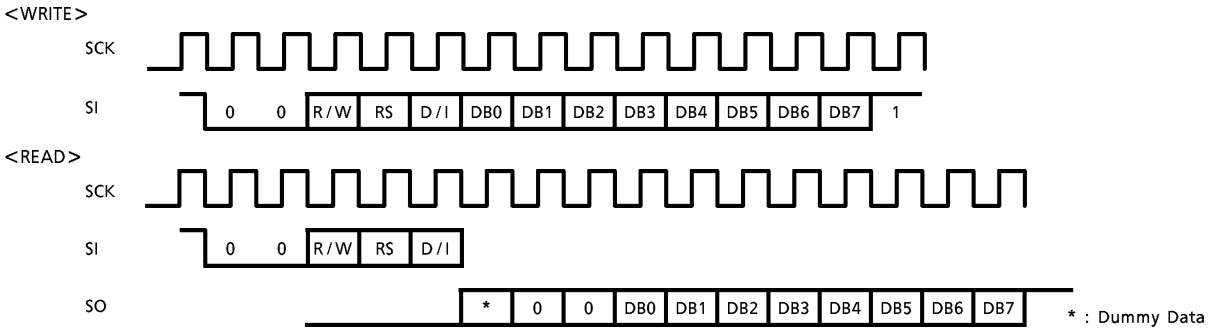


Fig.2

- Input register
  The register stores 8bit data from MPU. D / I signal discriminate between command data and display data.
- X-address counter
  X-address counter is 64-Up / Down counter. It holds the row address for the display RAM. Then it is selected by the command, writing to or reading the data of display RAM causes the X-address to automatically increment or decrement.
- Y (Page) -address counter
  The Y (Page) -address counter is 32-Up / Down counter. It holds the column address for the display RAM. This counter is selected by the command. Writing to or reading the display RAM causes the Y-address to automatically increment or decrement.
- Z-address counter
  The Z-address counter is 64-Up counter that provide the display RAM data for the LCD drive circuit. The data stored in Z-Address Register is send to Z-Address counter as Z start address.
  For instance, when Z start address is 16, the counter increment like this : 16, 17, 18···, 62, 63, 0, 1, 2···14, 15, 16. Therefore, the display start line is 16-line of the display RAM.

- Up / Down register

  The 1bit data stored in this register selects Up or Down mode of X and Y (Page) -address counter.

- Counter select register

  The 1bit data stored in this register selects X-address counter or Y (Page) -address counter.

- Display ON / OFF register

  This 1bit register holds the display ON or OFF state. In the OFF state, the output data from the display RAM is not selected. In the On state, the display data appears according to the display RAM data. The display ON or OFF state does not affect the data of display RAM.

- Z-address register

  This 6bit register holds the data that indicates the display start line.

- Oscillator

  The T6K03A / B / C has an on-chip oscillator. When using this oscillator, connect an external resistor between OSC1 and OSC2. When using external clock, input the clock to OSC1 and open OSC2, as shown in Fig.3.

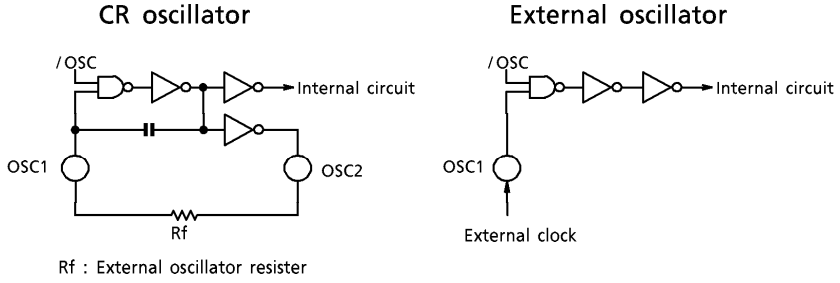


Fig.3

- Timing generation circuit

  The circuit divides the signals from the oscillator and generates display timing signals and operating clock.

- Shift-register

  The T6K03A / B / C has two 32bit shift-register and shift register of ICON. These shift-register construct 65 bits shift-register.

- Latch circuit

  This latch circuit latches the data from the display RAM.

- Column driver circuit

  Column driver circuit consists of 128 driver circuits. One of the four LCD driving level is selected by the combination of M (internal signal) and the display data transferred from the latch circuit. Details of column driver circuit are shown in Fig.4.

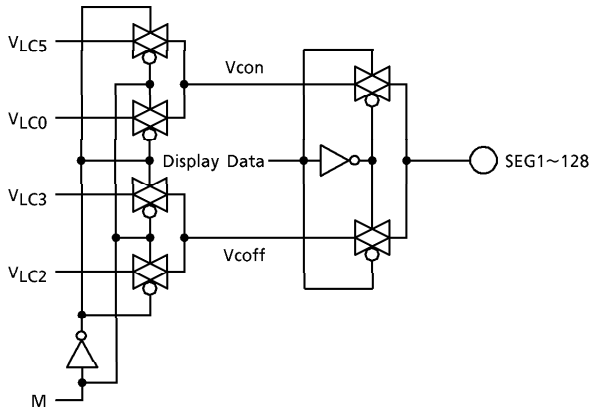


Fig.4

- Row driver circuit

  Row driver circuit consists of 65 drive circuits. One of the four LCD driving level is selected by the combination of M (internal signal) and the data from the sift register. Details of row driver circuit are shown in Fig.5.

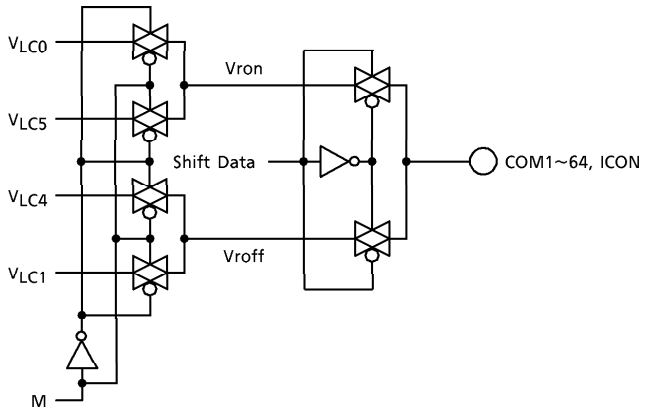
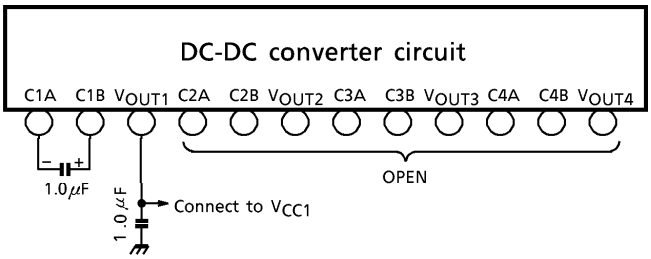


Fig.5

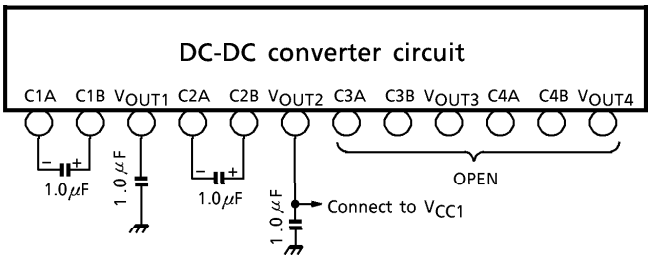
- DC-DC converter

  The T6K03A / B / C has an on-ship DC-DC converter. The DC-DC converter generates ×2 (V_{IN}×2 [V]) level, ×3 (V_{IN}×3 [V]), ×4 (V_{IN}×4 [V]) and ×5 (V_{IN}×5 [V]) level. When STB = L V_{OUTn} = 0 [V]. Recommended value of the capacitance is 1.0μF.

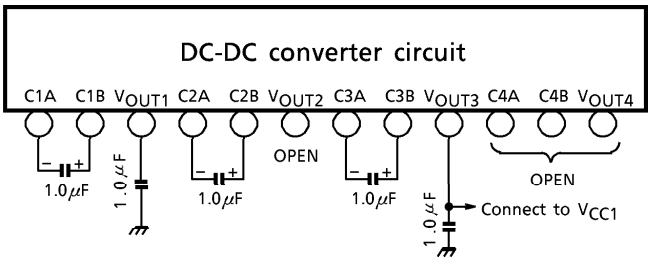
(1) X2 DC-DC converter



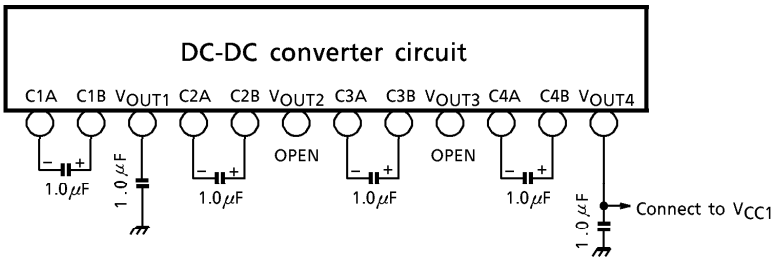
(2) X3 DC-DC converter



(3) X4 DC-DC converter



(4) X5 DC-DC converter

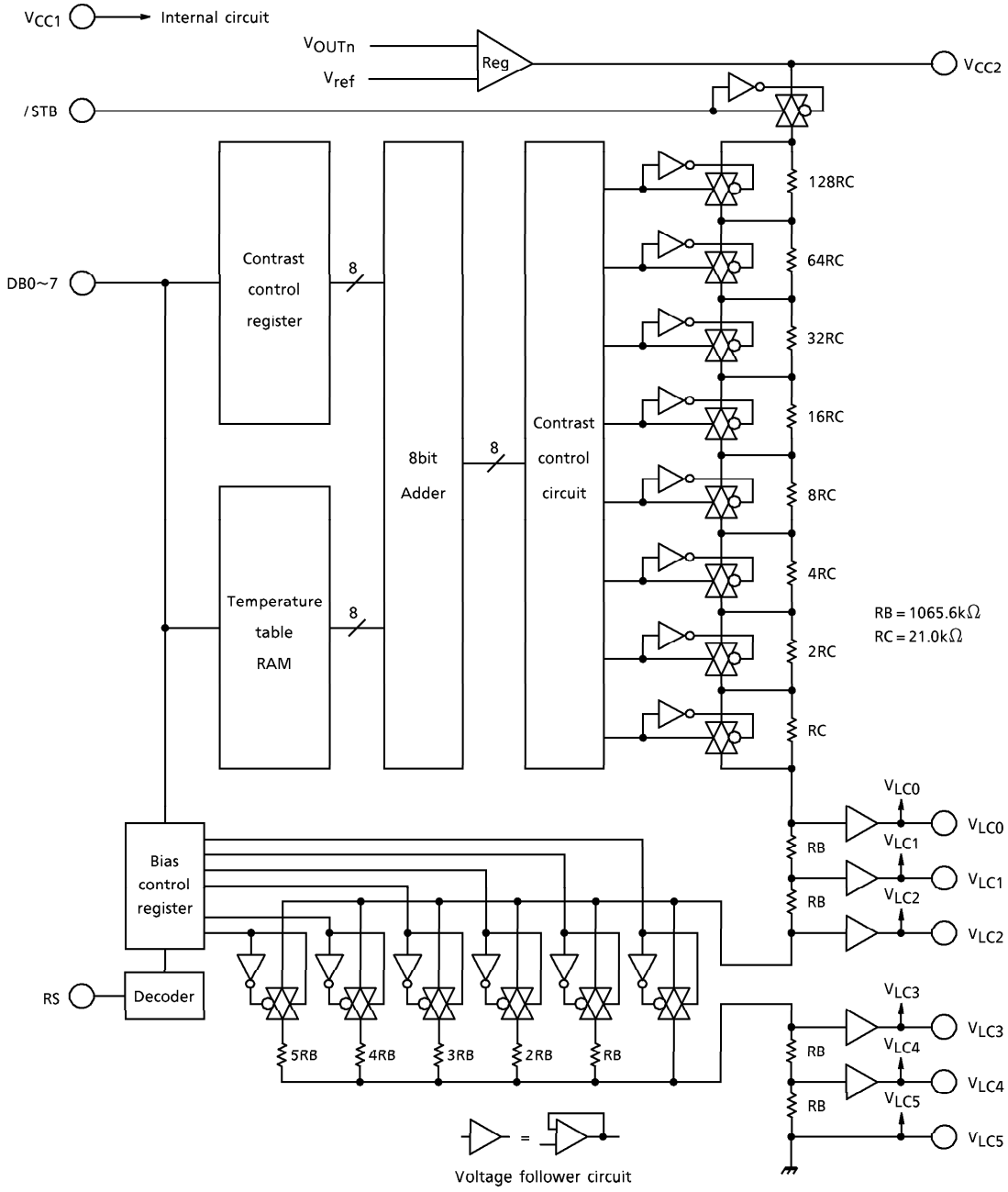


When using external power supply, input the voltage to V_{CC1}, and unconnect to capacitance.

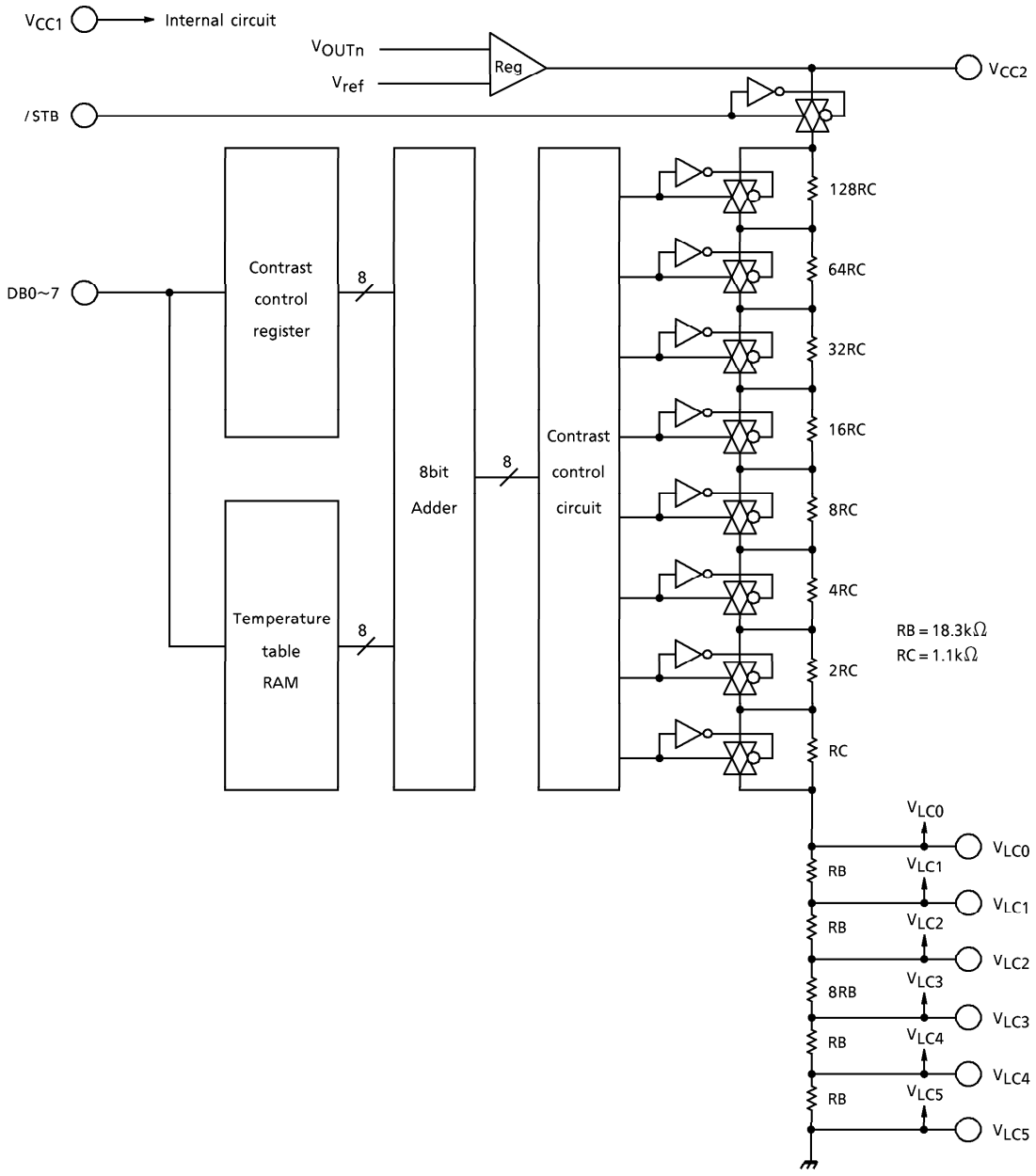
- Voltage driver resistor, contrast control circuit (Normal mode)

  The T6K03A / B / C has on-chip resistors to divide bias voltage with OP-Amp., and a contrast control circuit.

  The voltage bias is changed by instruction command. And one of four bias is selected.

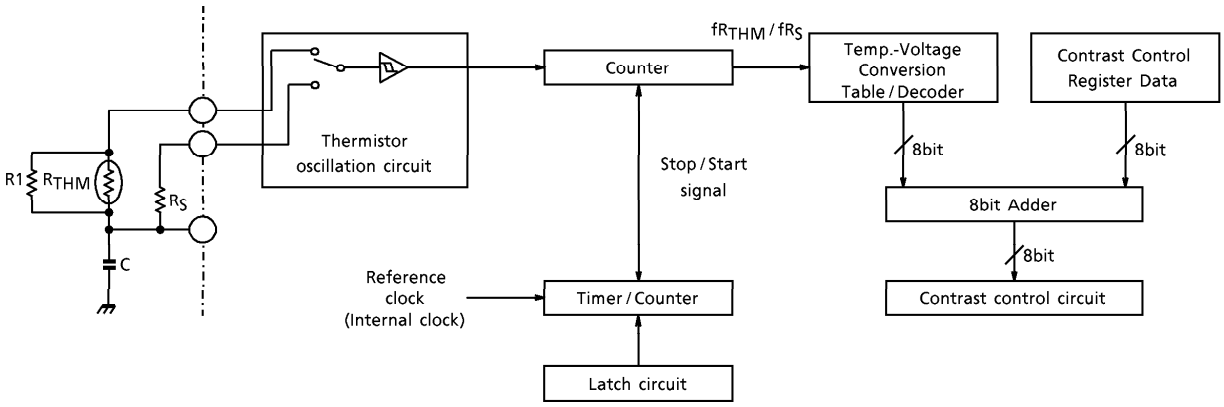


- Voltage driver resistor, contrast control circuit (Power Save Mode)



- Temperature compensation circuit

  The T6K03A / B / C has the temperature compensation circuit.



R1 : 91kΩ
R_S : 47kΩ
R_{THM} : 100kΩ Thermistor
Semitec Type 104HT-1P
C : 1000pF

COMMAND DEFINITION

COMMAND	Reg. No.	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Register set (REG)	—	0	0	0	1	*	Register (0~127)						
Status read (STRD)	—	0	0	1	0	MD	(*)	LYW	F/N	G/B	DP	Y/X	U/D
Data mode (DMD)	R0	0	1	0	1	*	*	*	*	*	D/TM	Y/X	U/D
Display mode (DPE)	R1	0	1	0	1	*	CDR	SDR	G/B	LY1	LY0	N/F	DP
Power (PWE)	R2	0	1	0	1	*	*	*	*	*	VR	OP	DC
Bias/Duty (DTE)	R3	0	1	0	1	Bias Select (5~9)				Duty Select (0~15)			
Oscillation (OSE)	R4	0	1	0	1	*	*	*	*	*	*	*	OSC
Gray scale 1 (GR1)	R5~R8	0	1	0	1	*	*	*	Grayscale Data 1 (0~31)				
Gray scale 2 (GR2)	R9~R12	0	1	0	1	*	*	*	Grayscale Data 2 (0~31)				
X, Y address (SXYE)	R13	0	1	0	1	1	F/N	X-Address (0~63)					
		0	1	0	1	0	*	*	LYW	Y-Address (0~31)			
Z address (SZE)	R14	0	1	0	1	*	*	Z-Address (0~63)					
Contrast (SCE)	R15	0	1	0	1	Contrast Control (0~255)							
TMP mode (TMPM)	R16	0	1	0	1	*	*	*	*	TMOF	*	1/0	1/0
TMP address (TMPA)	R17	0	1	0	1	*	TMP Address (0~127)						
FRS control (FRSC)	R18	0	1	0	1	*	*	FR control					
TEST mode (CHE1~3)	R20~22	0	1	0	1	Please don't using this register							
Gray scale 3 (GRC)	R64~R127	0	1	0	1	Grayscale Data							
Data write (DAWR)	—	1	1	0	1	Write Data							
Data read (DARD)	—	1	1	1	0	Read Data							

* : INVALID

comment : When using the status read check, DB6 data is "L" level. T6K03B
When using the status read check, DB6 data is "H" level. T6K03A/C

- Register set

  Identify register number
  R0 (00H)~R127 (7FH)
  Note : T6K03A / B / C isn't using register between R24 to R63 and R19.

- R0 : Data mode

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	*	*	*	*	*	D/TM	Y/X	U/D

  D / TM : Select display RAM address counter / TMP RAM address counter
  D / TM = 1 : Display RAM counter D / TM = 0 : TMP RAM counter

  X / Y : Select X / Y-counter
  Y / X = 1 : Y-counter selected Y / X = 0 : X-counter selected

  U / D : Select counter Up / Down mode
  U / D = 1 : Up mode U / D = 0 : Down mode

- R1 : Display mode

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	*	CDR	SDR	G/B	LY1	LY0	N/F	DP

  CDR : Select common data how
  CDR = 1 : COM1→COM64 CDR = 0 : COM64→COM1

  SDR : Select segment data direction
  See page 25

  G / B : Select gray scale or Black / White mode
  G / B = 1 : Gray scale mode G / B = 0 : Black / White mode

  LY1 : Select display layer 1 (When G / B = 1, This bit is ignored.)
  LY1 = 1 : Select layer 1 LY1 = 0 : Not select layer 1

  LY0 : Select display layer 2 (When G / B = 1, This bit is ignored.)
  LY0 = 1 : Select layer 0 LY0 = 0 : Not select layer 0

  (When LY1 and LY0 is "H" level, display data has 0R-data of LY1 and LY0.)

  N / F : Select display
  N / F = 1 : Normal display N / F = 0 : Flag display only (Power save mode)

  DP : Display ON / OFF
  DP = 1 : Display ON DP = 0 : Display OFF

- R2 : Power management

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	*	*	*	*	*	VR	OP	DC

VR : Voltage regulator
VR = 1 : Voltage regulator ON VR = 0 : Voltage regulator OFF

OP : Op-amp
OP = 1 : Op-amp ON OP = 0 : Op-amp OFF

DC : DC-DC converter
DC = 1 : DC-DC converter ON DC = 0 : DC-DC converter OFF

- R3 : Duty / Bias select

Code

D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	1	0	1	*	*	*	*	1	1	1	1	1/65 duty
0	1	0	1	*	*	*	*	1	1	1	0	1/63 duty
0	1	0	1	*	*	*	*	1	1	0	1	1/61 duty
0	1	0	1	*	*	*	*	1	1	0	0	1/59 duty
0	1	0	1	*	*	*	*	1	0	1	1	1/57 duty
0	1	0	1	*	*	*	*	1	0	1	0	1/55 duty
0	1	0	1	*	*	*	*	1	0	0	1	1/53 duty
0	1	0	1	*	*	*	*	1	0	0	0	1/51 duty
0	1	0	1	*	*	*	*	0	1	1	1	1/49 duty
0	1	0	1	*	*	*	*	0	1	1	0	1/47 duty
0	1	0	1	*	*	*	*	0	1	0	1	1/45 duty
0	1	0	1	*	*	*	*	0	1	0	0	1/43 duty
0	1	0	1	*	*	*	*	0	0	1	1	1/41 duty
0	1	0	1	*	*	*	*	0	0	1	0	1/39 duty
0	1	0	1	*	*	*	*	0	0	0	1	1/37 duty
0	1	0	1	*	*	*	*	0	0	0	0	1/35 duty
0	1	0	1	1	0	0	1	*	*	*	*	1/9 bias
0	1	0	1	1	0	0	0	*	*	*	*	1/8 bias
0	1	0	1	0	1	1	1	*	*	*	*	1/7 bias
0	1	0	1	0	1	1	0	*	*	*	*	1/6 bias
0	1	0	1	0	1	0	1	*	*	*	*	1/5 bias
0	1	0	1	0	1	0	0	*	*	*	*	Don't connect

- R4 : Oscillation control

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	*	*	*	*	*	*	*	OSC

OSC : Oscillator ON / OFF
OSC = 1 : Oscillator ON OSC = 0 : Oscillator OFF

- R5~R8 : Gray scale register (Normal scale)

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R5	0	1	0	1	*	*	*	GS0 (0~31)				
R6	0	1	0	1	*	*	*	GS1 (0~31)				
R7	0	1	0	1	*	*	*	GS2 (0~31)				
R8	0	1	0	1	*	*	*	GS3 (0~31)				

→

Corresponding Display RAM Data	
0	0
0	1
1	0
1	1

The contents of this register define four levels of gray scale from GS0 to GS3.

- R9~R12 : Gray scale register (Power save scale)

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R9	0	1	0	1	*	*	*	GS0 (0~31)				
R10	0	1	0	1	*	*	*	GS1 (0~31)				
R11	0	1	0	1	*	*	*	GS2 (0~31)				
R12	0	1	0	1	*	*	*	GS3 (0~31)				

→

Corresponding Display RAM Data	
0	0
0	1
1	0
1	1

The contents of this register define four levels of gray scale from GS0 to GS3.

- R13 : X-address, Y-address set

(1) X-address set

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	1	F/N	X-Address (0~63)					

F/N = 0 : Set display RAM address from 0 to 63
F/N = 1 : Set flag RAM (The data from DB0 to DB5 is ignored)

(2) Y-address set

When G/B = 1 (Gray scale mode)

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	*	*	Y-Address (0~31)				

When G/B = 0 (Black/White mode)

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	*	*	LYW	Y-Address (0~15)			

LYW = 1 : Write data to Layer 1 LYW = 0 : Write data to Layer 0

- R14 : Z-address set

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	*	*	Z-Address (0~63)					

The command set the starting line of display RAM.

- R15 : Contrast control

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Contrast Control (0~255)							

This command set contrast.
Contrast data 255 correspond to maximum contrast.
Contrast data 0 correspond to minimum contrast.

- R16 : TMP mode

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	*	*	*	*	TMOF	*	1/0	1/0

TMOP : Temperature compensation ON/OFF
TMOF = 1 : ON TMOF = 0 : OFF (Note 1)

DB1	DB0	
1	1	4sec cycle
1	0	2sec cycle
0	1	1sec cycle
0	0	No measurement

(Note 1) Data on the output bus of the temperature table RAM are fixed on "L" data.
Therefore, data on the contrast control register are inputted to contrast control circuit.

- R17 : TMP address

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	*	TMP address (0~127)						

This command set temperature compensation address.
In case of using this command, counter up mode only.

- R18 : FRS control

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	*	*	FR control (0~63)					

This command sets the number of the row lines for polarity change.
The setting of FRS corresponds to the row line number, see following table.

FRS	FRAME
0	In case 1/x duty is selected by R3, FR signal inverts on every x line. (Note)
n	FR signal inverts on every (n + 1) line.

(Note) In case FRS = 0 ;
FR signal inverts synchronously with the edge of COM1.
In case FRS ≠ 0 (1~63) ;
FR signal inverts synchronously with the edge of COMm. (m = 1 to 64, or ICON)
"m" shows a COM line right after the instruction practice.

- R20~R22

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Test mode							

Please don't access this register.

- R64~R127

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Gray scale-3 data							

The 32-Gray scale level can be made by inputting data to this register. 1-Gray scale level have two register. This register have the PWM (Pulse Width Modulation) and FRC (Frame Rate Control) control data.

a) Data of PWM (Pulse Width Modulation)

	HEX	4BIT	PWN (ON WIDTH)	NOTE
0	00	0000	0 (0/9)	
1	01	0001	1/9	
2	02	0010	2/9	
3	03	0011	3/9	
4	04	0100	4/9	
5	05	0101	5/9	
6	06	0110	6/9	
7	07	0111	7/9	
8	08	1000	8/9	
9	09	1001	1 (9/9)	
10	0A	1010	0/9	(Note 1)
11	0B	1011	0/9	(Note 1)
12	0C	1100	0/9	(Note 1)
13	0D	1101	0/9	(Note 1)
14	0E	1110	0/9	(Note 1)
15	0F	1111	0/9	(Note 1)

(*) The phase of PWM turns over by the even/add of the output pin.
(Note 1) This area is selected to off level (0/9 level).

b) Grayscal table of FRC (Frame Rate Control)

REGISTER	GRAYSCAL LEVEL	MSB (4BIT)	LSB (4BIT)	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
R64	0	1st FR (FR1)	0th FR (FR0)									
R65		3rd FR (FR3)	2nd FR (FR2)									
R66	1	1st FR (FR1)	0th FR (FR0)									
R67		3rd FR (FR3)	2nd FR (FR2)									
R68	2	1st FR (FR1)	0th FR (FR0)									
R69		3rd FR (FR3)	2nd FR (FR2)									
R70	3	1st FR (FR1)	0th FR (FR0)									
R71		3rd FR (FR3)	2nd FR (FR2)									
R72	4	1st FR (FR1)	0th FR (FR0)									
R73		3rd FR (FR3)	2nd FR (FR2)									
R74	5	1st FR (FR1)	0th FR (FR0)									
R75		3rd FR (FR3)	2nd FR (FR2)									
R76	6	1st FR (FR1)	0th FR (FR0)									
R77		3rd FR (FR3)	2nd FR (FR2)									
R78	7	1st FR (FR1)	0th FR (FR0)									
R79		3rd FR (FR3)	2nd FR (FR2)									
R80	8	1st FR (FR1)	0th FR (FR0)									
R81		3rd FR (FR3)	2nd FR (FR2)									
R82	9	1st FR (FR1)	0th FR (FR0)									
R83		3rd FR (FR3)	2nd FR (FR2)									
R84	10	1st FR (FR1)	0th FR (FR0)									
R85		3rd FR (FR3)	2nd FR (FR2)									
R86	11	1st FR (FR1)	0th FR (FR0)									
R87		3rd FR (FR3)	2nd FR (FR2)									
R88	12	1st FR (FR1)	0th FR (FR0)									
R89		3rd FR (FR3)	2nd FR (FR2)									
R90	13	1st FR (FR1)	0th FR (FR0)									
R91		3rd FR (FR3)	2nd FR (FR2)									
R92	14	1st FR (FR1)	0th FR (FR0)									
R93		3rd FR (FR3)	2nd FR (FR2)									
R94	15	1st FR (FR1)	0th FR (FR0)									
R95		3rd FR (FR3)	2nd FR (FR2)									
R96	16	1st FR (FR1)	0th FR (FR0)									
R97		3rd FR (FR3)	2nd FR (FR2)									
R98	17	1st FR (FR1)	0th FR (FR0)									
R99		3rd FR (FR3)	2nd FR (FR2)									
R100	18	1st FR (FR1)	0th FR (FR0)									
R101		3rd FR (FR3)	2nd FR (FR2)									
R102	19	1st FR (FR1)	0th FR (FR0)									
R103		3rd FR (FR3)	2nd FR (FR2)									
R104	20	1st FR (FR1)	0th FR (FR0)									
R105		3rd FR (FR3)	2nd FR (FR2)									
R106	21	1st FR (FR1)	0th FR (FR0)									
R107		3rd FR (FR3)	2nd FR (FR2)									
R108	22	1st FR (FR1)	0th FR (FR0)									
R109		3rd FR (FR3)	2nd FR (FR2)									
R110	23	1st FR (FR1)	0th FR (FR0)									
R111		3rd FR (FR3)	2nd FR (FR2)									
R112	24	1st FR (FR1)	0th FR (FR0)									
R113		3rd FR (FR3)	2nd FR (FR2)									
R114	25	1st FR (FR1)	0th FR (FR0)									
R115		3rd FR (FR3)	2nd FR (FR2)									
R116	26	1st FR (FR1)	0th FR (FR0)									
R117		3rd FR (FR3)	2nd FR (FR2)									
R118	27	1st FR (FR1)	0th FR (FR0)									
R119		3rd FR (FR3)	2nd FR (FR2)									
R120	28	1st FR (FR1)	0th FR (FR0)									
R121		3rd FR (FR3)	2nd FR (FR2)									
R122	29	1st FR (FR1)	0th FR (FR0)									
R123		3rd FR (FR3)	2nd FR (FR2)									
R124	30	1st FR (FR1)	0th FR (FR0)									
R125		3rd FR (FR3)	2nd FR (FR2)									
R126	31	1st FR (FR1)	0th FR (FR0)									
R127		3rd FR (FR3)	2nd FR (FR2)									

- Status read

	D/I	RS	/WR	/RD	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	MD	*	LYW	F/N	G/B	DP	Y/X	V/D

MD : When input the V_{DD} level from MD terminal,
MD (DB7) = 1.
When input the V_{SS} level from MD terminal,
MD (DB7) = 0.

LYW : When LYW = 1, the Layer No is Layer 1.
When LYW = 0, the Layer No is Layer 0.
(*) Using the black / white mode.

F / N : When F / N = 1, Display mode is FLAG Display only mode.
When F / N = 0, Display mode is Normal Display mode.

G / B : When G / B = 1, Display mode is Gray scale mode.
When G / B = 0, Display mode is Black / White mode.

DP : When DP = 1, Display is ON.
When DP = 0, Display is OFF.

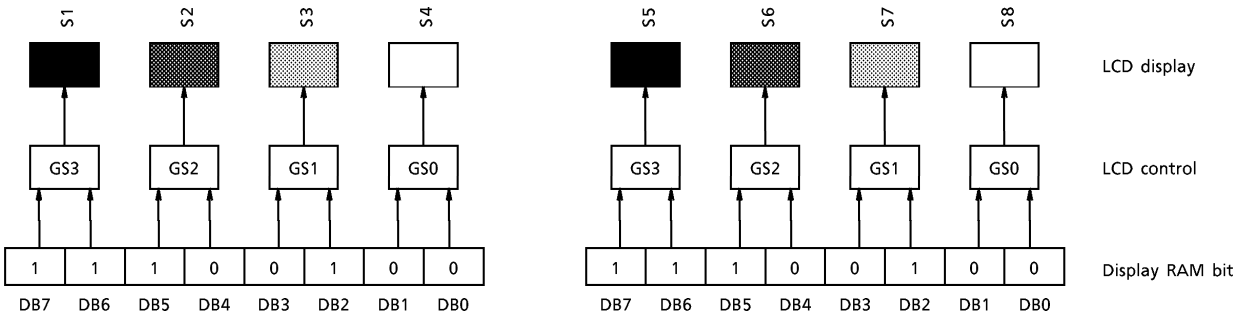
Y / X : When Y / X = 1, Y-counter is selected.
When Y / X = 0, X-counter is selected.

U / D : When U / D = 1, X and Y counters are in up mode.
When U / D = 0, X and Y counters are in down mode.

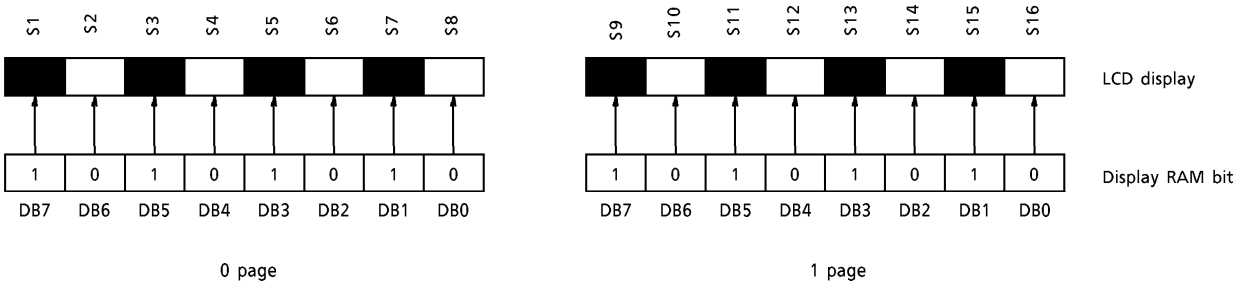
FUNCTION DESCRIPTION

- Display data bit

(1) In case of gray scale mode (Display RAM from 2bit)

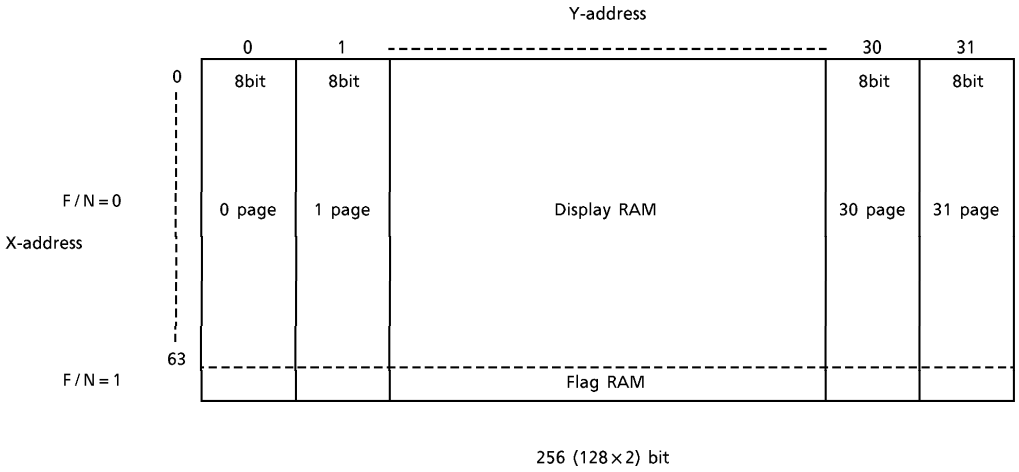


(2) In case of black / white mode (Display RAM from 1bit)



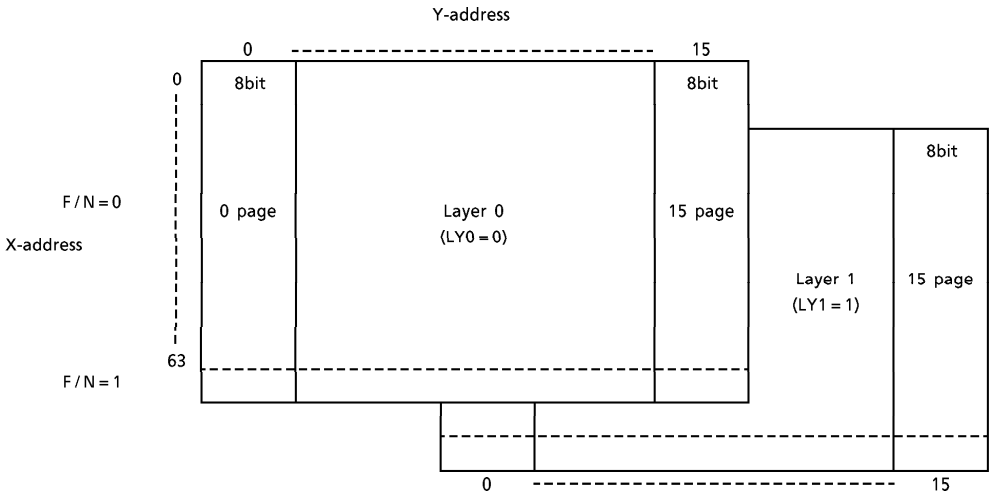
- Display mode

(1) Grayscale mode (G / B = 1)



256 (128 × 2) bit

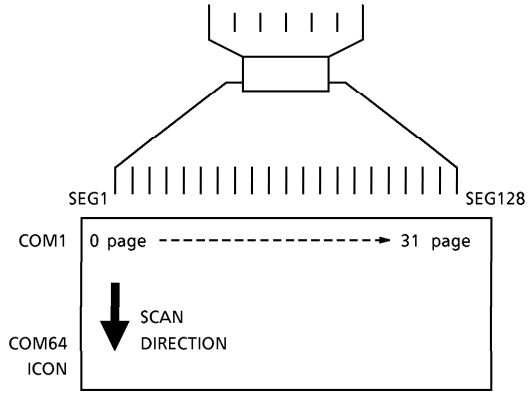
(2) Black / White mode (G / B = 0)



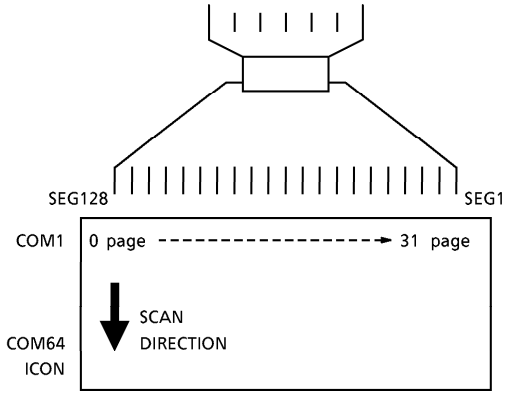
- RAM map and CDR, SDR relation

  Example : When G / B = 1

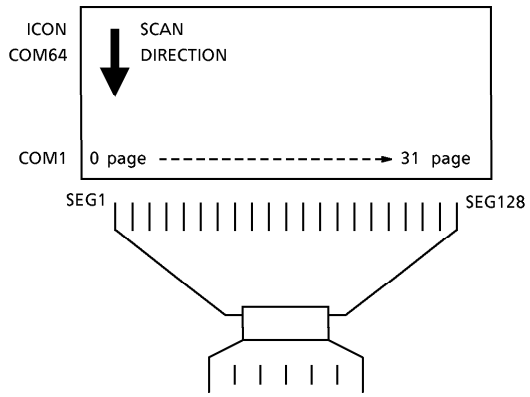
(1) CDR = 1, SDR = 1



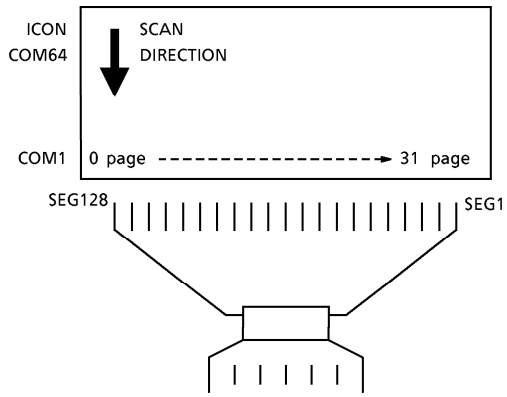
(2) CDR = 1, SDR = 0



(3) CDR = 0, SDR = 1



(4) CDR = 0, SDR = 0



- Reset function

When / RST = "L", reset function is executed and following instruction (resister) are executed.

COMMAND	REG No.	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Data mode	R0	*	*	*	*	*	1	1	1	Y-counter / Up-mode
Display mode	R1	*	1	1	1	0	0	1	0	(Note 1)
Power	R2	*	*	*	*	*	0	1	0	(Note 2)
Duty / Bias	R3	1	0	0	1	1	1	1	1	1 / 65 duty, 1 / 9 bias
Oscillation	R4	*	*	*	*	*	*	*	1	OSC ON
Gray scale 1	R5~R8	*	*	*	0	0	0	0	0	
Gray scale 2	R9~R12	*	*	*	0	0	0	0	0	
X-address	R13	—	0	0	0	0	0	0	0	X-Add = 0
Y-address		—	*	0	0	0	0	0	0	Y-Add = 0
Z-address	R14	*	*	0	0	0	0	0	0	Z-Add = 0
Contrast	R15	0	0	0	0	0	0	0	0	Contrast = Min
TMP mode	R16	*	*	*	*	0	*	0	0	TMP OFF
TMP address	R17	*	0	0	0	0	0	0	0	TMP-add (X-add) = 0
FRS control	R18	*	*	0	0	0	0	0	0	1 / 65 duty
Gray scale 3	R64~R127	0	0	0	0	0	0	0	0	

(Note 1) COM1→COM64, SEG1→SEG128, Gray scale mode, Normal display,
(Note 2) VR OFF, OP-AMP ON, DC-DC OFF

- Standby function

When / STB = "L", the T6K03A / B / C is in standby state. The internal oscillation is stopped, power consumption is reduced, and power supply for LCD (V_{LC0}~V_{LC5}) become V_{SS}.

● Expansion function

The T6K03A / B / C has expansion function. When using this function, the T6K03A / B / C (2chip) can drive 256 × 64 + icon dots LCD panel (maximum) or 128 × 128 + icon dots LCD panel (Maximum). Next table shows the selectable function by using M / S pins.

M / S	
H	L
● One chip mode Disable expansion mode ● Two chips mode (Master chip) Timing signal and power voltage supply to Slave chip.	● Two chips mode (Slave chip) Timing signal and power voltage are supplied from Master chip.

Fig.6 and Fig.7 illustrate the application example of disable expansion mode and enable expansion mode.

In enable expansion mode (Tow chip mode)

As shown in Fig.7-1, Fig.7-2 Master chip supplies LCD drive signals and power voltage to slave chip. (The oscillator, the timing circuits, Op-Amp, and Contrast control circuit are disable.)

(1) Disable expansion mode

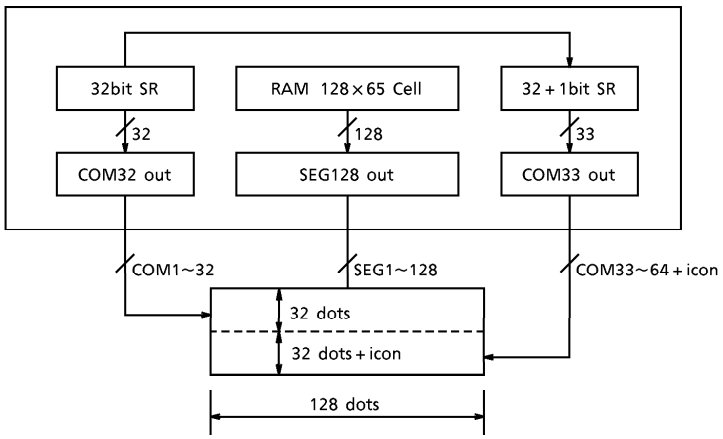


Fig.6

(2) Enable expansion mode

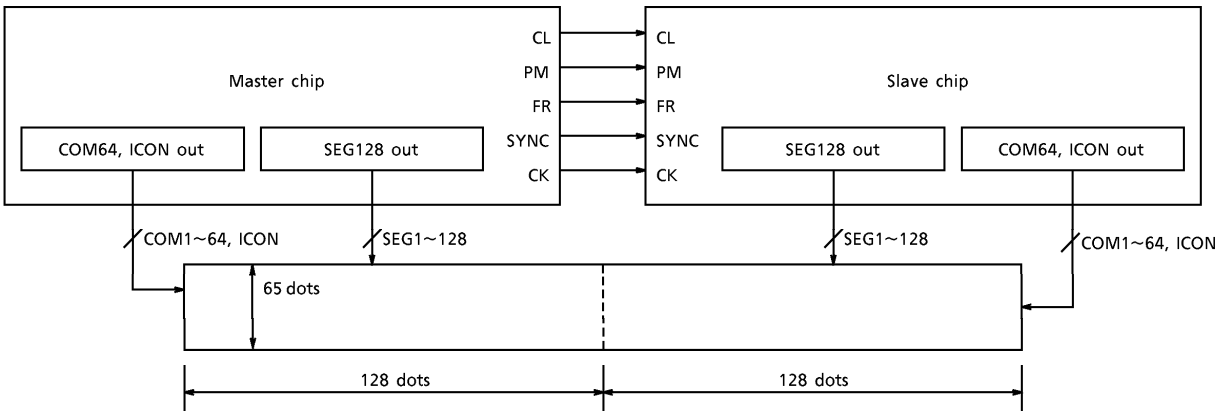


Fig.7-1

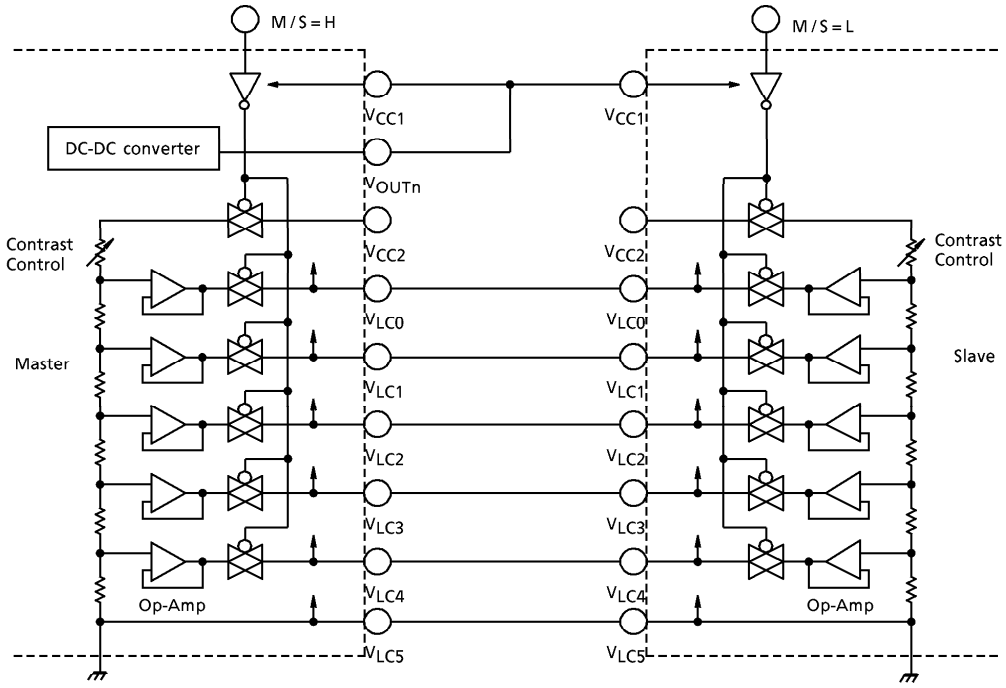


Fig.7-2

● X-address counter and Y (Page) -address counter

Fig.8-1 shows a sample of operating procedure for the X-address counter.
After reset is executed, X-address becomes X-address = 0, then select X-counter / Up mode. Next set the X-address to 62 by commanding SXYE (R13).
After data has been written to or read, the X-address is automatically incremented by one.
After X-counter / Down mode has been selected and data has been written to or read, the X-address is automatically decremented by one.
When the X-counter is selected, Y-counter does not count up or down.
And flag-counter does not count up or down too.

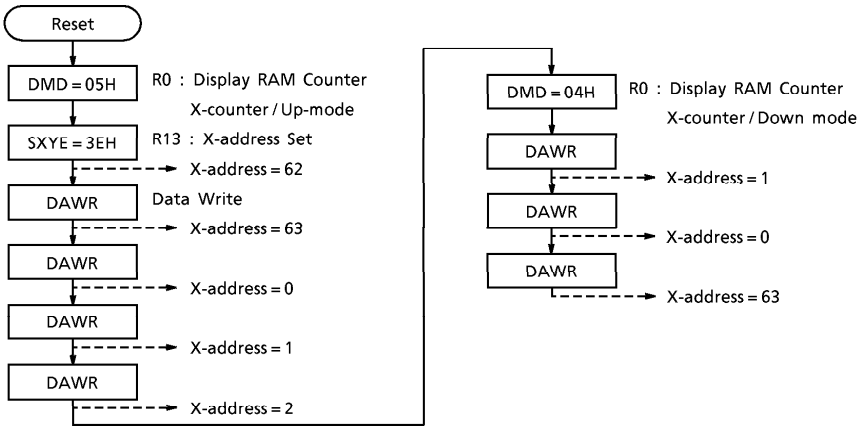


Fig.8-1

Fig.8-2 shows a sample operating procedure for the Y-address counter.
After reset is executed, Y (Page) -address becomes Y-address = 0, then select Y (Page) -counter / Up-mode. After data has been written to or read, the Y (Page) -address counter is automatically incremented by one.
After Y (Page) -counter / Down mode has been selected and data has been written to or read, the Y (Page) -address is automatically decremented by one.
When the Y (Page) -counter is selected, X-counter doesn't count up or down.

(Note) When using the Gray scale mode, Y (Page) -address is 00H~31H.
When using the Black / White mode, Y (Page) -address is 00H~15H.

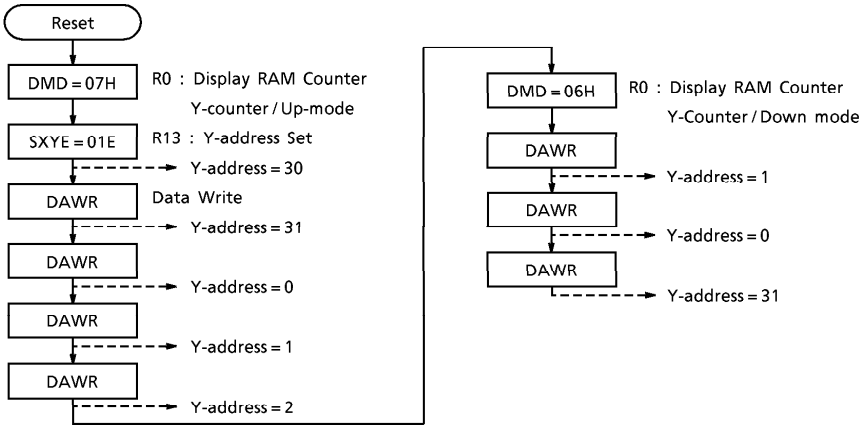
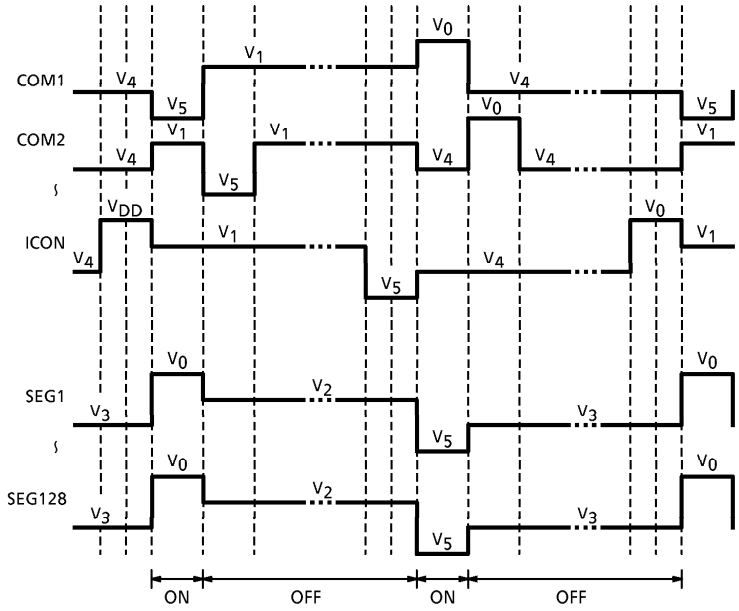


Fig.8-2 (Gray scale mode)

- **LCD DRIVER WAVEFORM** (Case of normal mode)



LCD driver timing chart (1/65 duty)

MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD} (Note 1)	−0.3~7.0	V
Supply Voltage (2)	$V_{LC1, 2, 3, 4, 5}$ V_{CC1}, V_{CC2}	V_{SS} + 18.0~V_{SS} − 0.3	V
Input Voltage	V_{IN} (Note 1, 2)	−0.3~V_{DD} + 0.3	V
Operating Temperature	T_{opr}	−30~85	°C
Storage Temperature	T_{stg}	−55~125	°C

(Note 1) Referred to V_{SS} = 0V
(Note 2) Applied data bus terminals and Input terminals expect V_{CC1}, V_{CC2}, V_{LC0}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}, V_{LC5}.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (1)

(Test condition : If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, V_{LC5} = 0V, Ta = 25°C)

ITEM		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Operating Supply (1)		V_{DD}	—	—	2.7	—	3.3	V	V_{DD}, V_{IN}
Operating Supply (2)		V_{LC0} $V_{CC1, 2}$	—	—	6.0 – V_{SS}	—	16.5 – V_{SS}	V	V_{LC0}, V_{CC1}, V_{CC2}
Input Level	"H" Level	V_{IH}	—	—	0.8V_{DD}	—	V_{DD}	V	DB0~DB7, D/I, /WR, /RD, /CS1, CS2, /RST, /STB, RS, SI, SCK, P/S, 68/80, CL, PM, FR, SYNC, CK
	"L" Level	V_{IL}	—	—	0	—	0.2V_{DD}	V	
Output Level	"H" Level	V_{OH}	—	I_{OH} = –400μA	V_{DD} – 0.2	—	V_{DD}	V	DB0~DB7, SO, CL, PM, FR, SYNC, CK
	"L" Level	V_{OL}	—	I_{OL} = 400μA	0	—	0.2	V	
Column Driver On Resistance	Normal Mode	Rcol1	—	(Note 1)	—	—	7.5	kΩ	SEG1~SEG128
	Power Save Mode	Rcol2	—	(Note 2)	—	—	15.0	kΩ	SEG1~SEG128
Row Driver On Resistance	Normal Mode	Rrow1	—	(Note 1)	—	—	1.5	kΩ	COM1~COM64, ICON
	Power Save Mode	Rrow2	—	(Note 2)	—	—	5.0	kΩ	COM1~COM64, ICON
Input Leakage		I_{IL}	—	V_{IN} = V_{DD} ~GND	– 1	—	1	μA	DB0~DB7, D/I, /WR, /RD, /CS1, CS2, /RST, /STB, RS, SI, SCK, P/S, 68/80, CL, PM, FR, SYNC, CK
Operating Freq		f_{OSC}	—	(Note 6)	—	82	—	kHz	OSC1
External Clock Freq		f_{ex}	—	(Note 6)	—	82	—	kHz	OSC1
External Clock Duty		f_{duty}	—	—	45	50	55	%	OSC1
External Clock Rise / Fall Time		t_r / t_f	—	—	—	—	50	ns	OSC1
Current Consumption (1)		I_{SS1}	—	(Note 3)	—	460	650	μA	V_{SS}
Current Consumption (2)		I_{SS2}	—	(Note 4)	—	970	1200	μA	V_{SS}
Current Consumption (3)		I_{SSSTB}	—	(Note 5)	– 1	—	1	μA	V_{SS}

(Note 1) V_{SS} + V_{LC0} = 11.0V, Load current = ± 100μA, 1/9 bias

(Note 2) V_{SS} + V_{LC0} = 3.0V, Load current = ± 100μA, 1/12 bias

(Note 3) V_{DD} = 3.0V, $V_{CC1, 2}$ = V_{OUT4} (X5 mode), No data access, Internal clock (f_{OSC} = 82kHz), LCD out pin No Load, 1/9 bias, 1/65 duty, OP-Amp. on, regulator on

(Note 4) V_{DD} = 3.0V, $V_{CC1, 2}$ = V_{OUT4} (X5 mode), Data access cycle $\overline{fCE}$ = 1MHz, Internal clock (OSC = 82kHz), LCD out pin No Load, 1/9 bias, 1/65 duty, OP-Amp. on, regurator on

(Note 5) V_{DD} = 3.3V, $V_{CC1, 2}$ – V_{SS} = 16.0V, /STB = L

(Note 6) In case of 1/65 duty and f_{FR} = 70Hz

DC CHARACTERISTICS (2)
Common DC characteristic for T6K03A / B / C
(Test condition : If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, V_{LC5} = 0V, Ta = 25°C)

ITEM	SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Output Voltage (X2 Mode)	VO1	(1)	(Note 1)	5.00	5.07	—	V	V_{OUT1}
Output Voltage (X3 Mode)	VO2	(2)	(Note 2)	7.25	7.41	—	V	V_{OUT2}
Output Voltage (X4 Mode)	VO3	(3)	(Note 3)	9.64	9.84	—	V	V_{OUT3}
Output Voltage (X5 Mode)	VO4	(4)	(Note 4)	11.83	12.11	—	V	V_{OUT4}

(Note 1) V_{IN} = 2.7V, ILoad = 200μA, $V_{CC1,\ 2}$ = 5.40V (external power supply)
CnA – CnB = 1.0μF, V_{OUT1} – V_{SS} = 1.0μF, OSC = 82kHz, Ta = 25°C

(Note 2) V_{IN} = 2.7V, ILoad = 200μA, $V_{CC1,\ 2}$ = 8.10V (external power supply)
CnA – CnB = 1.0μF, V_{OUT1} – V_{SS} = 1.0μF, OSC = 82kHz, Ta = 25°C

(Note 3) V_{IN} = 2.7V, I_{Load} = 200μA, $V_{CC1,\ 2}$ = 10.80V (external power supply)
CnA – CnB = 1.0μF, V_{OUT1} – V_{SS} = 1.0μF, OSC = 82kHz, Ta = 25°C

(Note 4) V_{IN} = 2.7V, I_{Load} = 200μA, $V_{CC1,\ 2}$ = 13.50V (external power supply)
CnA – CnB = 1.0μF, V_{OUT1} – V_{SS} = 1.0μF, OSC = 82kHz, Ta = 25°C

DC CHARACTERISTICS (3-1)
T6K03A
(Test condition : If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, V_{LC5} = 0V)

ITEM	SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Regulator Reference Voltage (1.2)	V_{ref12}	—	(Note 5)	1.09	—	1.35	V	VR12
Regulator Reference High Voltage (1)	VHR	—	(Note 6) Ta = 25°C	10.78	—	12.47	V	V_{CC2}
Regulator Reference High Voltage (2)	VHRC	—	(Note 6) Ta = – 20°C	0.986 × VHR	0.999 × VHR	1.012 × VHR	V	V_{CC2}
Regulator Reference High Voltage (3)	VHRH	—	(Note 6) Ta = 60°C	0.994 × VHR	1.006 × VHR	1.018 × VHR	V	V_{CC2}

(Note 5) V_{DD} = 2.7~3.3V, V_{SS} = 0V
(Note 6) $V_{CC1} \geqq$ 12.8V at Ta = – 20~60°C

DC CHARACTERISTICS (3-2)
T6K03B
(Test condition : If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, V_{LC5} = 0V)

ITEM	SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Regulator Reference Voltage (1.2)	V_{ref12}	—	(Note 5)	1.09	—	1.35	V	VR12
Regulator Reference High Voltage (1)	VHR	—	(Note 6) Ta = 25°C	10.43	—	12.47	V	V_{CC2}
Regulator Reference High Voltage (2)	VHRC	—	(Note 6) Ta = − 20°C	0.986 × VHR	0.999 × VHR	1.012 × VHR	V	V_{CC2}
Regulator Reference High Voltage (3)	VHRH	—	(Note 6) Ta = 60°C	0.994 × VHR	1.006 × VHR	1.018 × VHR	V	V_{CC2}

(Note 5) V_{DD} = 2.7~3.3V, V_{SS} = 0V
(Note 6) $V_{CC1} \geqq$ 12.8V at Ta = − 20~60°C

DC CHARACTERISTICS (3-3)
T6K03C
(Test condition : If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, V_{LC5} = 0V)

ITEM	SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Regulator Reference Voltage (1.2)	V_{ref12}	—	(Note 5)	1.09	—	1.35	V	VR12
Regulator Reference High Voltage (1)	VHR	—	(Note 6) Ta = 25°C	10.22	—	12.28	V	V_{CC2}
Regulator Reference High Voltage (2)	VHRC	—	(Note 6) Ta = − 20°C	0.986 × VHR	0.999 × VHR	1.012 × VHR	V	V_{CC2}
Regulator Reference High Voltage (3)	VHRH	—	(Note 6) Ta = 60°C	0.994 × VHR	1.006 × VHR	1.018 × VHR	V	V_{CC2}

(Note 5) V_{DD} = 2.7~3.3V, V_{SS} = 0V
(Note 6) $V_{CC1} \geqq$ 12.6V at Ta = − 20~60°C

DC CHARACTERISTICS (4)
Common DC characteristic for T6K03A / B / C
(Test condition : If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, V_{LC5} = 0V)

ITEM	SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	APPLICABLE TERMINAL
Op-Amp Output Voltage Offset (1)	V_{opoff}	—	(Note 1)	– 150	—	150	mV	V_{LC0}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}
Op-Amp Output Voltage Offset (2)	V_{opoffs}	—	(Note 2)	– 90	—	90	mV	V_{LC0}, V_{LC1}, V_{LC2}, V_{LC3}, V_{LC4}

(Note 1) V_{DD} = 2.7~3.3V, V_{SS} = 0V, 1 / 9 bias, 1 / 65 duty
V_{CC1} = 13.0V, V_{CC2} = 12.5V, Contrast control = max
Op-Amp ON, DC-DC OFF, regulator OFF, LCD outpin No Load

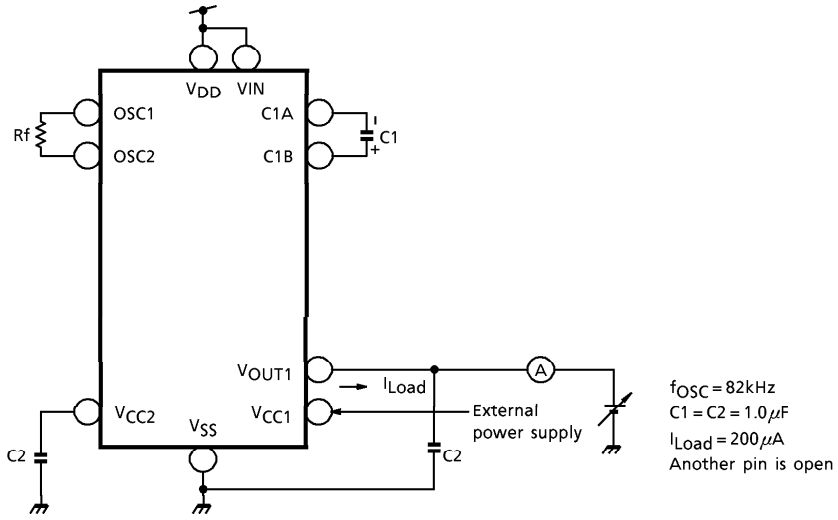
Case of V_{LC0} : $12.5 - V_{LC0} = V_{opoff}$
V_{LC1} : $(12.5 \div 8 / 9) - V_{LC1} = V_{opoff}$
V_{LC2} : $(12.5 \div 7 / 9) - V_{LC2} = V_{opoff}$
V_{LC3} : $(12.5 \div 2 / 9) - V_{LC3} = V_{opoff}$
V_{LC4} : $(12.5 \div 1 / 9) - V_{LC4} = V_{opoff}$

(Note 2) V_{DD} = 2.7~3.3V, V_{SS} = 0V, 1 / 9 bias, 1 / 65 duty
V_{CC1} = 13.0V, V_{CC2} = 12.5V, Contrast control = max
Op-Amp ON, DC-DC OFF, regulator OFF, LCD outpin No Load

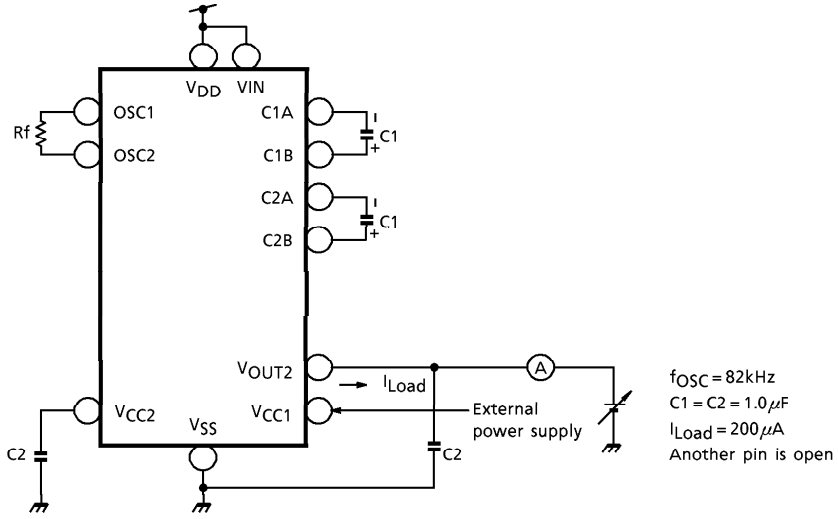
$$V_{opoffs} = ((V_{LC1} - V_{LC2}) - (V_{LC0} - V_{LC1})) + ((V_{LC3} - V_{LC4}) - (V_{LC4} - V_{LC5}))$$

TEST CIRCUIT

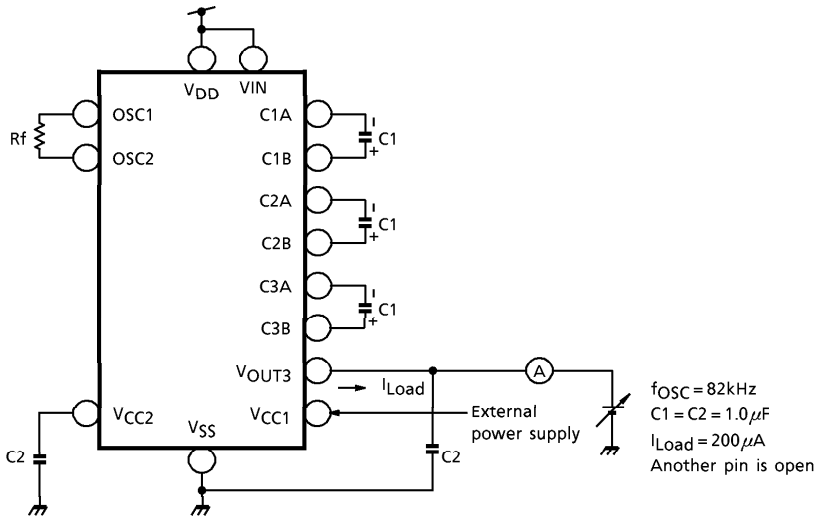
(1) DC-DC converter X2 mode



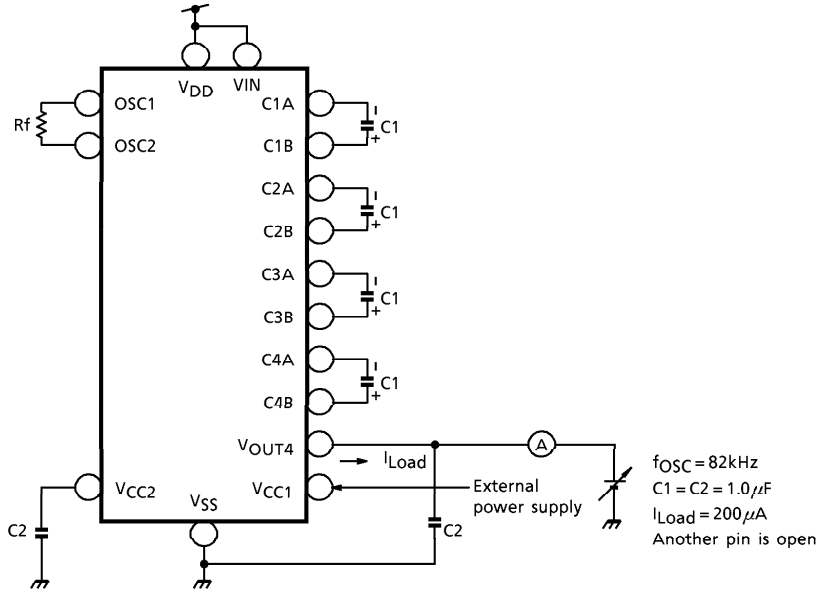
(2) DC-DC converter X3 mode



(3) DC-DC converter X4 mode

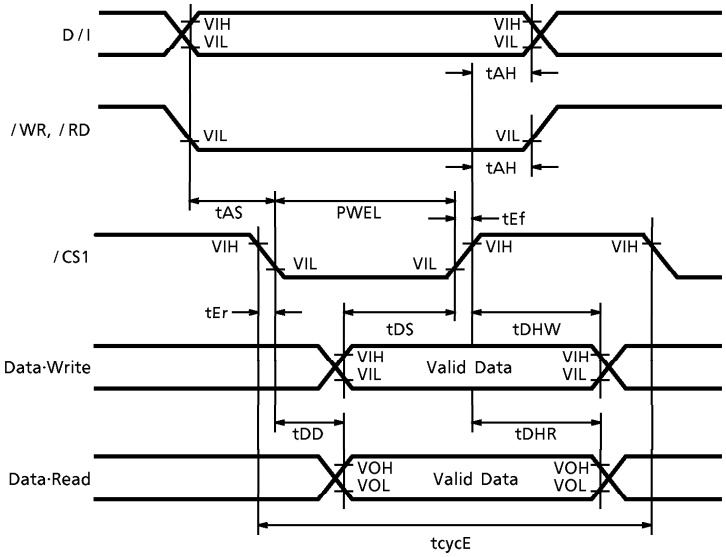


(4) DC-DC converter X5 mode



AC CHARACTERISTICS

- Switching characteristics (80 series MPU 8bit interface)

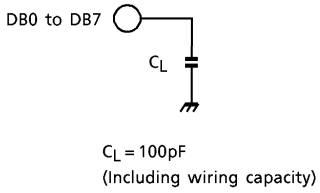


TEST CONDITION
(If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNIT
Enable Cycle Time	tcycE	500		ns
Enable Pulse Width	PWEL	410		ns
Enable Rise / Fall Time	tEr, tEf		25	ns
Address Set-up Time	tAS	20		ns
Address Hold Time	tAH	0		ns
Data Set-up Time	tDS	100		ns
Data Hold Time	tDHW	20		ns
Data Delay Time	tDD (Note)		400	ns
Data Hold Time	tDHR (Note)	20		ns

(Note) Connect to Load circuit.

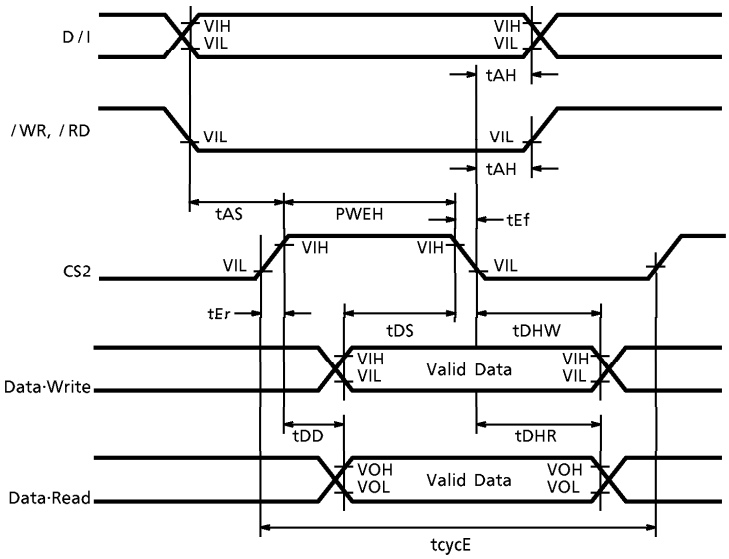
LOAD CIRCUIT



C_L = 100pF
(Including wiring capacity)

AC CHARACTERISTICS

- Switching characteristics (80 series MPU 8bit interface)

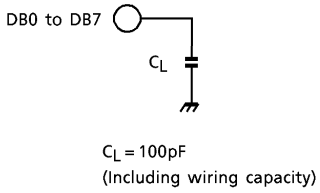


TEST CONDITION
(If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNITS
Enable Cycle Time	tcycE	500		ns
Enable Pulse Width	PWEL	410		ns
Enable Rise / Fall Time	tEr, tEf		25	ns
Address Set-up Time	tAS	20		ns
Address Hold Time	tAH	0		ns
Data Set-up Time	tDS	100		ns
Data Hold Time	tDHW	20		ns
Data Delay Time	tDD (Note)		400	ns
Data Hold Time	tDHR (Note)	20		ns

(Note) Connect to Load circuit.

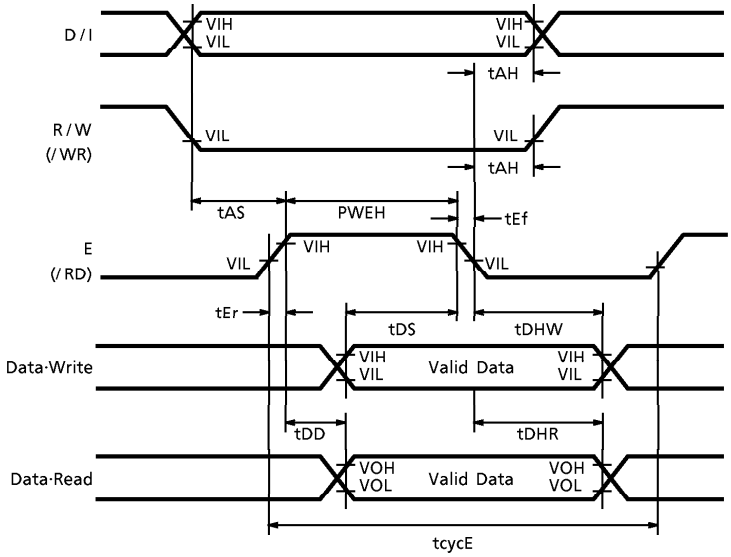
LOAD CIRCUIT



C_L = 100pF
(Including wiring capacity)

AC CHARACTERISTICS

- Switching characteristics (68 series MPU 8bit interface)

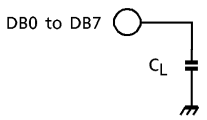


TEST CONDITION
(If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNITS
Enable Cycle Time	tcycE	500		ns
Enable Pulse Width	PWEH	410		ns
Enable Rise / Fall Time	tEr, tEf		25	ns
Address Set-up Time	tAS	20		ns
Address Hold Time	tAH	0		ns
Data Set-up Time	tDS	100		ns
Data Hold Time	tDHW	20		ns
Data Delay Time	tDD (Note)		400	ns
Data Hold Time	tDHR (Note)	20		ns

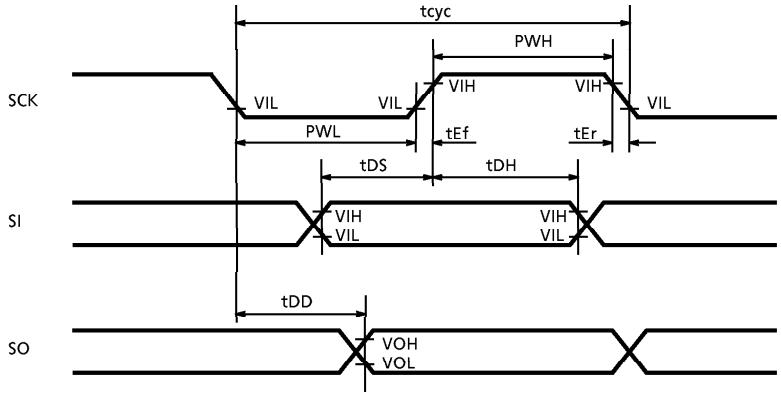
(Note) Connect to Load circuit.

LOAD CIRCUIT



C_L = 100pF
(Including wiring capacity)

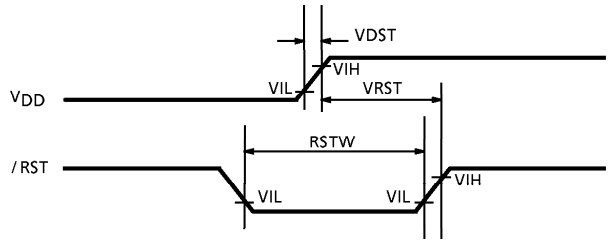
- Switching characteristics (serial interface)



TEST CONDITION
(If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNIT
Clock Cycle Time	tcycC	2000		ns
Clock Pulse Width	PWCL, PWCH	900		ns
Clock Rise / Fall Time	tCr, tCf		25	ns
Data Set-up Time	tDS	300		ns
Data Hold Time	tDH	100		ns
Data Delay Time	tDD		200	ns

- Switching characteristics (4)



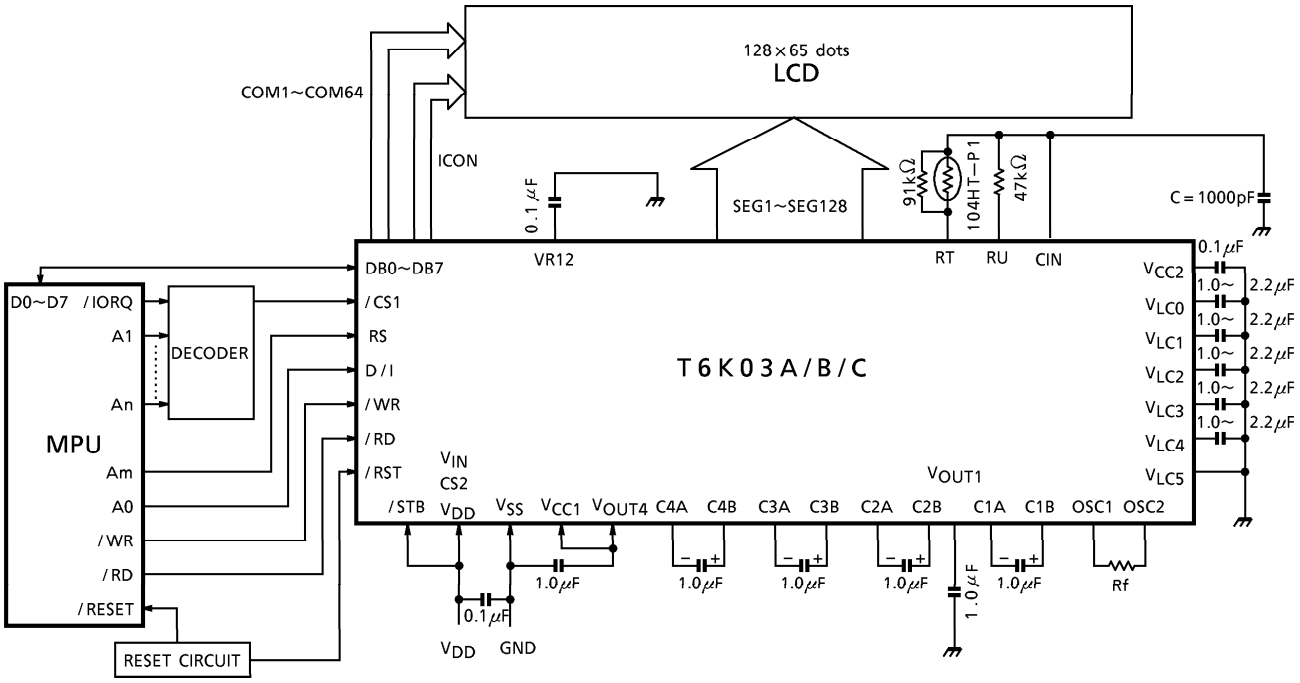
TEST CONDITION
(If not specified, V_{SS} = 0V, V_{DD} = 2.7~3.3V, Ta = 25°C)

ITEM	SYMBOL	MIN.	MAX.	UNIT
V_{DD} Rise Time	VDST		1	ms
Reset Hold Time	VRST	1		μs
Reset Pulse Width	RSTW	1		ms

APPLICATION CIRCUIT (1)

T6K03A / B / C One chip mode

- Using CR oscillation
- LCD drive bias 1 / 9
- Using DC-DC converter (X5 mode)
- Using 80 series MPU
- Using temperature compensation



APPLICATION CIRCUIT (2)

T6K03A / B / C Two chip mode

- Using CR oscillation
- LCD drive bias 1 / 9
- Using DC-DC converter (X5 mode)
- Using 80 series MPU