TOSHIBA CMOS DIGITAL INTEGRATED CIRCUITS SILICON MONOLITHIC

T6L34C

SOURCE DRIVER FOR TFT LCD PANELS

The T6L34C is a 256-gray-level, 384-channel-output source driver for TFT LCD panels. The device accepts 8 bit × 6 dot digital data inputs, for which the direction of data transfer can be selected by the U/D pin. The 12 (6 × 2) reference voltage input pins combined with the internal D/A converter materializes multicolor display in up to 16,700,000 colors.

Since the T6L34C supports a dot line inversion system, it eliminates the need for inversion of the LCD panel's counter electrode, allowing for high picture quality. Moreover, its output dynamic range is a large 12.6 V_{p-p} (max).

Based on high-speed CMOS, the T6L34C offers both low power consumption and high-speed operation. To configure an SXGA or XGA-compatible TFT LCD module, it allows a maximum operating frequency of 37.5 MHz.

Unit : mm

T6L34C	USER PITCH AREA	
	IN	OUT

Please contact Toshiba or an authorized Toshiba dealer TCP specification and product lineup.

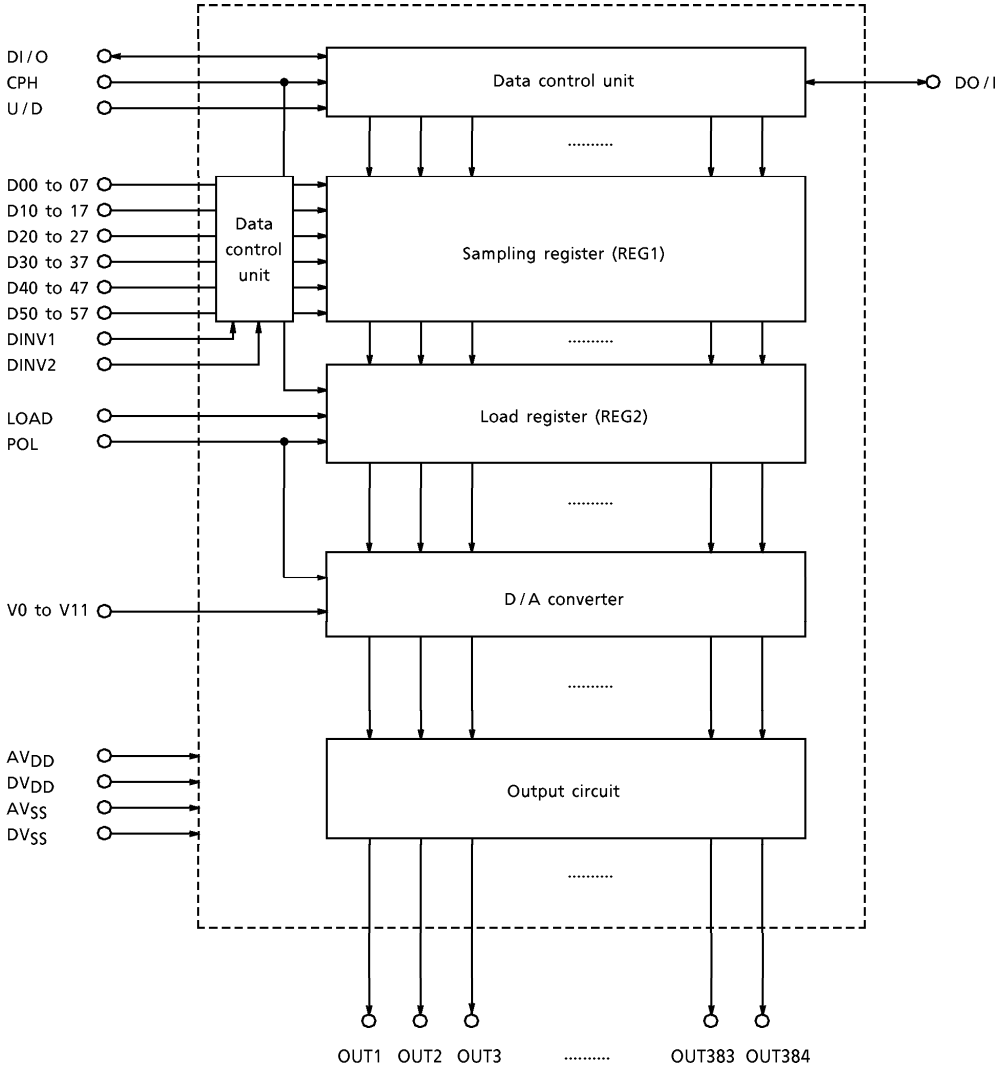
TCP (Tape Carrier Package)

FEATURES

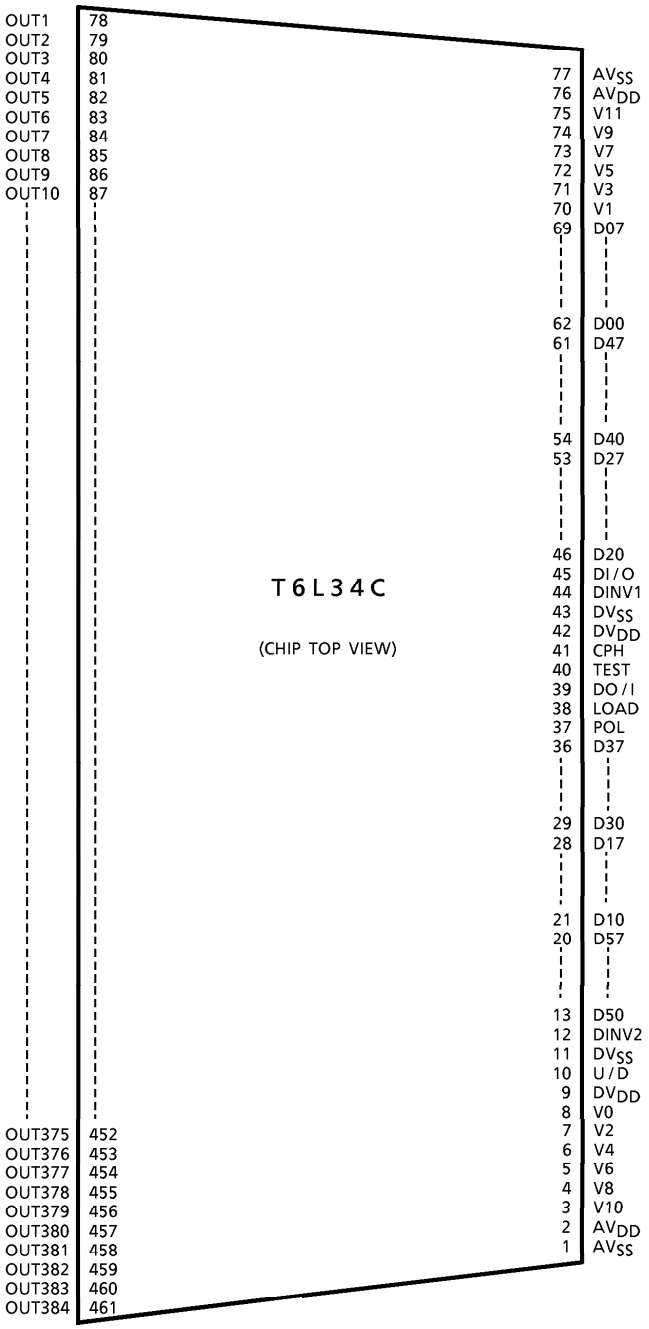
- Grayscale data : Digital CMOS-level 48-bit (8 bits × 6 outputs) parallel transfer method, selectable transfer direction
- Panel drive outputs : 384 outputs, 256 gray levels, R-DAC system, 12 (6 × 2) reference analog voltage inputs, dot/line inversion drive
- Fast operation : Max 37.5 MHz
- Power supply voltage : Digital power supply voltage ..... 3.0 to 3.6 V
  Analog power supply voltage ..... 7.5 to 13.0 V
- Operating temperature : −20 to 75°C
- Cascading of multiple devices
- Package : Tape carrier package (TCP)

980910EBE2

BLOCK DIAGRAM



PIN ASSIGNMENT



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

PIN FUNCTION

<table>
<tr><th>PIN NAME</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Data transfer enable pins
These two pins, which become active at the high signal, initiate the transfer of data into the sampling register of the device. One pin is configured as an determined by U/D as shown below :
<table><tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr><tr><td>H</td><td>Input</td><td>Output</td></tr><tr><td>L</td><td>Output</td><td>Input</td></tr></table>When set for input
A high on DI/O or DO/I is latched into the internal logic synchronously with the rising edge of CPH. When the internal circuit is in standby state, the device is ready to transfer data. The grayscale data are latched in sequentially, starting at the next rise of CPH.
When set for output
The pin is used to transfer the enable signal to the T6L34C at the next stage of the LCD driver.
The pin enters standby state after outputting a high.</td></tr>
<tr><td>U/D</td><td>I</td><td>Transfer direction select pin
This pin controls the direction in which the data are transferred into the sampling register. Data are transferred synchronously with each rising edge of CPH in one of the following sequences :
When U/D is high, data is transferred in the order OUT1 to OUT6, OUT7 to OUT12, and so on.
When U/D is low, the direction is reversed to the order OUT379 to OUT384, OUT373 to OUT378, and so on.
The voltage applied to this pin must be a DC-level voltage that is either high or low.</td></tr>
<tr><td>CPH</td><td>I</td><td>Data transfer clock input
This clock input is used to transfer the grayscale data.
The grayscale data is latched into the REG1 sequentially at each rising edge of CPH.
Always make sure that a constant-period clock is input to this pin.</td></tr>
<tr><td>D00 to 07
D10 to 17
D20 to 27
D30 to 37
D40 to 47
D50 to 57</td><td>I</td><td>Grayscale data bus
The data inputs consist of 8-bit words for each of the six channels, that are transferred in parallel at the rising edge of CPH. The relationship between the grayscale data and the the output pins is as follows :
Grayscale data = 128 × Dn7 + 64 × Dn6 + 32 × Dn5
+ 16 × Dn4 + 8 × Dn3 + 4 × Dn2 + 2 × Dn1 + Dn0
*where n = 0, 1, ···, 4, 5</td></tr>
</table>

PIN NAME	I/O	FUNCTION
DINV1 DINV2	I	Data polarity inverting pin These pins select whether or not the polarity of input data be inverted. The signals on these pins are latched into the REG1 synchronously with the rising edge of CPH in the same way as for the grayscale data bus. Logic operation : Data bus (Dxx) XOR DINV1, 2 when DINV1, 2 = high: data is inverted. when DINV1, 2 = low : data is not inverted. DINV1 chooses whether or not to invert grayscale data (D00 to D07, D10 to D17, D20 to D27). DINV2 chooses whether or not to invert grayscale data (D30 to D37, D40 to D47, D50 to D57).
LOAD	I	Data load input pin When a high voltage is supplied to the load input, the data are transferred from the sampling register to the load register synchronously at the rising edge of CPH. The selected analog voltage corresponding to the data is sent the LCD.
POL	I	Polarity inverting pin The signal of this pin is latched into the internal logic when a high voltage is supplied to the load input. When POL = high, the reference voltages for odd number outputs are V6 to V11 and those for even-number outputs are V0 to V5. When POL = low, the reference voltages for odd-number outputs are V0 to V5 and those for even-number outputs are V6 to V11.
V0 to V11	I	Reference analog input pins These pins are used to input the voltages used for the DAC. Conditions : $AV_{SS} < V11 \leqq V10 \leqq V9 \leqq V8 \leqq V7 \leqq V6 \leqq V5 \leqq V4 \leqq V3 \leqq V2 \leqq V1 \leqq V0 < AV_{DD}$
OUT1 to OUT384	O	LCD panel drive pins
AV_{DD}		Analog power supply pin
AV_{SS}		Analog GND pin This pin must be at the same potential level as the digital GND pin.
DV_{DD}		Digital power supply pin.
DV_{SS}		Digital GND pin This pin must be at the same potential level as the analog GND pin.
TEST	I	Test pin Leave this pin open.

DEVICE OPERATION

(1) Starting data transfer

A high input to the data transfer enable pin (DI / O or DO / I) is latched into the internal logic synchronously with the rising edge of CPH, setting the device ready to transfer data.
Data transfer starts at the next rise of CPH.
This enable pin must not be held for more than one CPH period.

(2) Data transfer method

The data in the grayscale data bus is latched to the sampling register (REG1) synchronously with each rising edge of CPH.
Grayscale data for six outputs are latched into the device simultaneously in one transfer. Therefore, 64 transfers are performed to latch the data. When the data loading is completed, the device enters a standby state. The data written into REG1 is the result of logical operation between the grayscale data bus and DINV.

(Note) : Make sure that a clock of the same period as applied during data transfer is input even while in standby state.
The LOAD input must not be driven high during data transfer.

(3) Terminating data transfer

The data transfer enable pin (DO / I or DI / O) output goes high synchronously with the rising edge of CPH, one clock period before the last data item is latched in. It is held high until the next rise of CPH.

(4) Panel drive output

After the data transfer enable pin (DO / I, DI / O) outputs, when a high voltage is supplied to the load input, the data in the sampling register (REG1) are transferred to the load register (REG2), and the device starts updating output to the LCD panel drive pins.

(Note) : Make sure the LOAD input is held high for more than 2 clock periods.

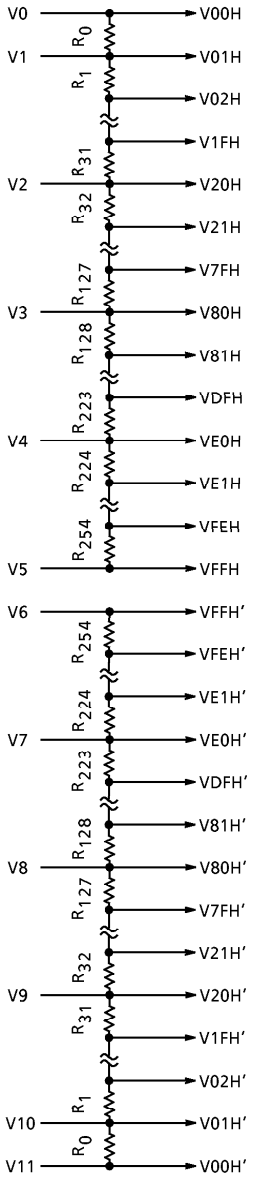
(5) Output offset correction function

The T6L34C incorporates a function which corrects offset to reduce output offset (see page 19).

(Note) : When tpdDX1 > tpdDX2 depending on the frequency of the CPH used, consult Toshiba.

(6) Reference power supply circuit

The D / A converter is comprised of ladder resistors and switches.



UNIT (Ω)

RESISTOR NAME	RESISTANCE VALUE	RESISTOR NAME	RESISTANCE VALUE	RESISTOR NAME	RESISTANCE VALUE	RESISTOR NAME	RESISTANCE VALUE
R_0	200	R_{32}	100	R_{64}	50	R_{96}	25
R_1	200	R_{33}	100	R_{65}	50	R_{97}	25
R_2	200	R_{34}	100	R_{66}	50	R_{98}	25
R_3	200	R_{35}	100	R_{67}	50	R_{99}	25
R_4	200	R_{36}	75	R_{68}	50	R_{100}	25
R_5	200	R_{37}	75	R_{69}	50	R_{101}	25
R_6	200	R_{38}	75	R_{70}	50	R_{102}	25
R_7	200	R_{39}	75	R_{71}	50	R_{103}	25
R_8	200	R_{40}	75	R_{72}	25	R_{104}	25
R_9	200	R_{41}	75	R_{73}	25	R_{105}	25
R_{10}	200	R_{42}	75	R_{74}	25	R_{106}	25
R_{11}	200	R_{43}	75	R_{75}	25	R_{107}	25
R_{12}	175	R_{44}	75	R_{76}	25	R_{108}	25
R_{13}	175	R_{45}	75	R_{77}	25	R_{109}	25
R_{14}	175	R_{46}	75	R_{78}	25	R_{110}	25
R_{15}	175	R_{47}	75	R_{79}	25	R_{111}	25
R_{16}	175	R_{48}	75	R_{80}	25	R_{112}	25
R_{17}	175	R_{49}	75	R_{81}	25	R_{113}	25
R_{18}	175	R_{50}	75	R_{82}	25	R_{114}	25
R_{19}	175	R_{51}	75	R_{83}	25	R_{115}	25
R_{20}	150	R_{52}	50	R_{84}	25	R_{116}	25
R_{21}	150	R_{53}	50	R_{85}	25	R_{117}	25
R_{22}	150	R_{54}	50	R_{86}	25	R_{118}	25
R_{23}	150	R_{55}	50	R_{87}	25	R_{119}	25
R_{24}	150	R_{56}	50	R_{88}	25	R_{120}	25
R_{25}	150	R_{57}	50	R_{89}	25	R_{121}	25
R_{26}	150	R_{58}	50	R_{90}	25	R_{122}	25
R_{27}	150	R_{59}	50	R_{91}	25	R_{123}	25
R_{28}	100	R_{60}	50	R_{92}	25	R_{124}	25
R_{29}	100	R_{61}	50	R_{93}	25	R_{125}	25
R_{30}	100	R_{62}	50	R_{94}	25	R_{126}	25
R_{31}	100	R_{63}	50	R_{95}	25	R_{127}	25

UNIT (Ω)

RESISTOR NAME	RESISTANCE VALUE	RESISTOR NAME	RESISTANCE VALUE	RESISTOR NAME	RESISTANCE VALUE	RESISTOR NAME	RESISTANCE VALUE
R_{128}	25	R_{160}	25	R_{192}	25	R_{224}	50
R_{129}	25	R_{161}	25	R_{193}	25	R_{225}	50
R_{130}	25	R_{162}	25	R_{194}	25	R_{226}	50
R_{131}	25	R_{163}	25	R_{195}	25	R_{227}	50
R_{132}	25	R_{164}	25	R_{196}	25	R_{228}	50
R_{133}	25	R_{165}	25	R_{197}	25	R_{229}	50
R_{134}	25	R_{166}	25	R_{198}	25	R_{230}	50
R_{135}	25	R_{167}	25	R_{199}	25	R_{231}	50
R_{136}	25	R_{168}	25	R_{200}	25	R_{232}	75
R_{137}	25	R_{169}	25	R_{201}	25	R_{233}	75
R_{138}	25	R_{170}	25	R_{202}	25	R_{234}	75
R_{139}	25	R_{171}	25	R_{203}	25	R_{235}	75
R_{140}	25	R_{172}	25	R_{204}	25	R_{236}	75
R_{141}	25	R_{173}	25	R_{205}	25	R_{237}	75
R_{142}	25	R_{174}	25	R_{206}	25	R_{238}	75
R_{143}	25	R_{175}	25	R_{207}	25	R_{239}	75
R_{144}	25	R_{176}	25	R_{208}	25	R_{240}	75
R_{145}	25	R_{177}	25	R_{209}	25	R_{241}	75
R_{146}	25	R_{178}	25	R_{210}	25	R_{242}	75
R_{147}	25	R_{179}	25	R_{211}	25	R_{243}	75
R_{148}	25	R_{180}	25	R_{212}	50	R_{244}	100
R_{149}	25	R_{181}	25	R_{213}	50	R_{245}	100
R_{150}	25	R_{182}	25	R_{214}	50	R_{246}	100
R_{151}	25	R_{183}	25	R_{215}	50	R_{247}	100
R_{152}	25	R_{184}	25	R_{216}	50	R_{248}	100
R_{153}	25	R_{185}	25	R_{217}	50	R_{249}	100
R_{154}	25	R_{186}	25	R_{218}	50	R_{250}	100
R_{155}	25	R_{187}	25	R_{219}	50	R_{251}	100
R_{156}	25	R_{188}	25	R_{220}	50	R_{252}	200
R_{157}	25	R_{189}	25	R_{221}	50	R_{253}	200
R_{158}	25	R_{190}	25	R_{222}	50	R_{254}	200
R_{159}	25	R_{191}	25	R_{223}	50	—	—

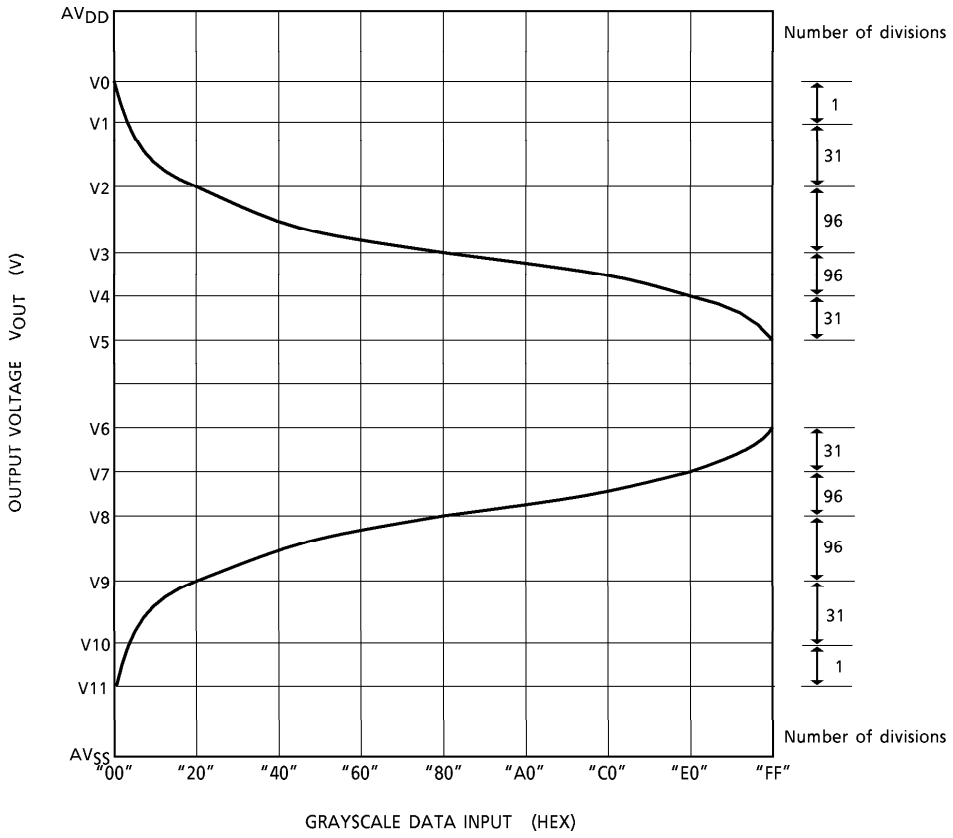
ΣR_0 = 0.2 kΩ
$\Sigma R_1 \sim R_{31}$ = 5.2 kΩ
$\Sigma R_{32} \sim R_{127}$ = 4.0 kΩ
$\Sigma R_{128} \sim R_{223}$ = 2.7 kΩ
$\Sigma R_{224} \sim R_{254}$ = 2.7 kΩ

Total = 14.8 kΩ

(6) Grayscale data and output voltages

The device's LCD drive output voltages are determined by the grayscale data values and the 12 (6 × 2) reference analog inputs corresponding to the the range of possible line voltages (V0 to V11). Note that since the T6L34C is corresponding to the dot inversion drive system, it can generate different grayscale voltages for even-numbered and odd-numbered outputs.

- Schematic representation of reference analog voltage inputs



- Grayscale Data and Output Voltages (Positive polarity output : V0 > V1 > V2 > V3 > V4 > V5)

GRAYSCALE DATA	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	OUTPUT VOLTAGE (ANTICIPATED VALUE)	
00H	0	0	0	0	0	0	0	0	V00H	V0
01H	0	0	0	0	0	0	0	1	V01H	V1
02H	0	0	0	0	0	0	1	0	V02H	V1 + (V2 − V1) × (200 × 1) / 5200
↓				↓					↓	↓
0CH	0	0	0	0	1	1	0	0	V0CH	V1 + (V2 − V1) × (200 × 11) / 5200
0DH	0	0	0	0	1	1	0	1	V0DH	V1 + (V2 − V1) × (2200 + 175 × 1) / 5200
↓				↓					↓	↓
14H	0	0	0	1	0	1	0	0	V14H	V1 + (V2 − V1) × (2200 + 175 × 8) / 5200
15H	0	0	0	1	0	1	0	1	V15H	V1 + (V2 − V1) × (3600 + 150 × 1) / 5200
↓				↓					↓	↓
18H	0	0	0	1	1	0	0	0	V18H	V1 + (V2 − V1) × (3600 + 150 × 4) / 5200
19H	0	0	0	1	1	0	0	1	V19H	V1 + (V2 − V1) × (4200 + 150 × 1) / 5200
↓				↓					↓	↓
1CH	0	0	0	1	1	1	0	0	V1CH	V1 + (V2 − V1) × (4200 + 150 × 4) / 5200
1DH	0	0	0	1	1	1	0	1	V1DH	V1 + (V2 − V1) × (4800 + 100 × 1) / 5200
1EH	0	0	0	1	1	1	1	0	V1EH	V1 + (V2 − V1) × (4800 + 100 × 2) / 5200
1FH	0	0	0	1	1	1	1	1	V1FH	V1 + (V2 − V1) × (4800 + 100 × 3) / 5200
20H	0	0	1	0	0	0	0	0	V20H	V2
21H	0	0	1	0	0	0	0	1	V21H	V2 + (V3 − V2) × (100 × 1) / 4000
↓				↓					↓	↓
24H	0	0	1	0	0	1	0	0	V24H	V2 + (V3 − V2) × (100 × 4) / 4000
25H	0	0	1	0	0	1	0	1	V25H	V2 + (V3 − V2) × (400 + 75 × 1) / 4000
↓				↓					↓	↓
34H	0	0	1	1	0	1	0	0	V34H	V2 + (V3 − V2) × (400 + 75 × 16) / 4000
35H	0	0	1	1	0	1	0	1	V35H	V2 + (V3 − V2) × (1600 + 50 × 1) / 4000
↓				↓					↓	↓
3FH	0	0	1	1	1	1	1	1	V3FH	V2 + (V3 − V2) × (1600 + 50 × 11) / 4000
40H	0	1	0	0	0	0	0	0	V40H	V2 + (V3 − V2) × (1600 + 50 × 12) / 4000
↓				↓					↓	↓
48H	0	1	0	0	1	0	0	0	V48H	V2 + (V3 − V2) × (1600 + 50 × 20) / 4000
49H	0	1	0	0	1	0	0	1	V49H	V2 + (V3 − V2) × (2600 + 25 × 1) / 4000
↓				↓					↓	↓
5FH	0	1	0	1	1	1	1	1	V5FH	V2 + (V3 − V2) × (2600 + 25 × 23) / 4000
60H	0	1	1	0	0	0	0	0	V60H	V2 + (V3 − V2) × (2600 + 25 × 24) / 4000
↓				↓					↓	↓
7FH	0	1	1	1	1	1	1	1	V7FH	V2 + (V3 − V2) × (2600 + 25 × 55) / 4000

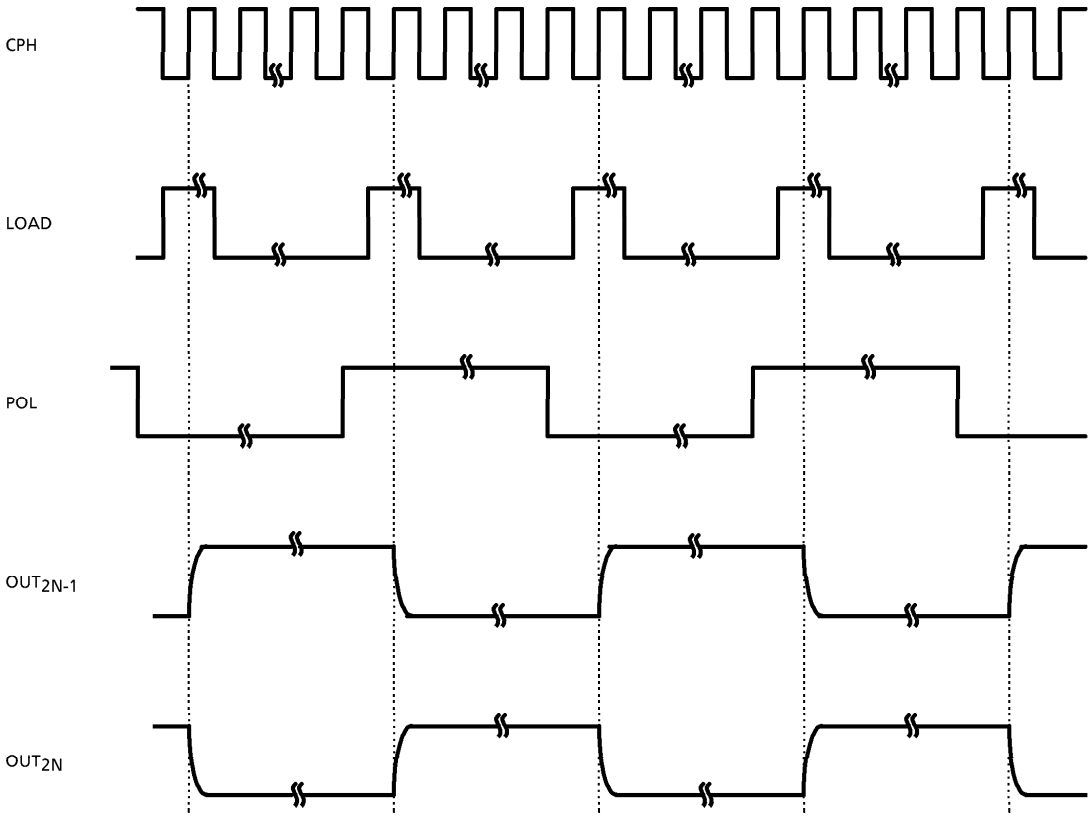
GRAYSCALE DATA	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	OUTPUT VOLTAGE (ANTICIPATED VALUE)	
80H	1	0	0	0	0	0	0	0	V80H	V3
81H	1	0	0	0	0	0	0	1	V81H	V3 + (V4 − V3) × (25 × 1) / 2700
↓					↓				↓	↓
9FH	1	0	0	1	1	1	1	1	V9FH	V3 + (V4 − V3) × (25 × 31) / 2700
A0H	1	0	1	0	0	0	0	0	VA0H	V3 + (V4 − V3) × (25 × 32) / 2700
↓					↓				↓	↓
BFH	1	0	1	1	1	1	1	1	VBFH	V3 + (V4 − V3) × (25 × 63) / 2700
C0H	1	1	0	0	0	0	0	0	VC0H	V3 + (V4 − V3) × (25 × 64) / 2700
↓					↓				↓	↓
D4H	1	1	0	1	0	1	0	0	VD4H	V3 + (V4 − V3) × (25 × 84) / 2700
D5H	1	1	0	1	0	1	0	1	VD5H	V3 + (V4 − V3) × (2100 + 50 × 1) / 2700
↓					↓				↓	↓
DFH	1	1	0	1	1	1	1	1	VDFH	V3 + (V4 − V3) × (2100 + 50 × 11) / 2700
E0H	1	1	1	0	0	0	0	0	VE0H	V4
E1H	1	1	1	0	0	0	0	1	VE1H	V4 + (V5 − V4) × (50 × 1) / 2700
↓					↓				↓	↓
E8H	1	1	1	0	1	0	0	0	VE8H	V4 + (V5 − V4) × (50 × 8) / 2700
E9H	1	1	1	0	1	0	0	1	VE9H	V4 + (V5 − V4) × (400 + 75 × 1) / 2700
↓					↓				↓	↓
F4H	1	1	1	1	0	1	0	0	VF4H	V4 + (V5 − V4) × (400 + 75 × 12) / 2700
F5H	1	1	1	1	0	1	0	1	VF5H	V4 + (V5 − V4) × (1300 + 100 × 1) / 2700
↓					↓				↓	↓
FCH	1	1	1	1	1	1	0	0	VFCH	V4 + (V5 − V4) × (1300 + 100 × 8) / 2700
FDH	1	1	1	1	1	1	0	1	VFDH	V4 + (V5 − V4) × (2100 + 200 × 1) / 2700
FEH	1	1	1	1	1	1	1	0	VFEH	V4 + (V5 − V4) × (2100 + 200 × 2) / 2700
FFH	1	1	1	1	1	1	1	1	VFFH	V5

- Grayscale Data and Output Voltages (Negative polarity output : V11 < V10 < V9 < V8 < V7 < V6)

GRAYSCALE DATA	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	OUTPUT VOLTAGE (ANTICIPATED VALUE)	
00H	0	0	0	0	0	0	0	0	V00H'	V11
01H	0	0	0	0	0	0	0	1	V01H'	V10
02H	0	0	0	0	0	0	1	0	V02H'	V10 + (V9 − V10) × (200 × 1) / 5200
↓					↓				↓	↓
0CH	0	0	0	0	1	1	0	0	V0CH'	V10 + (V9 − V10) × (200 × 11) / 5200
0DH	0	0	0	0	1	1	0	1	V0DH'	V10 + (V9 − V10) × (2200 + 175 × 1) / 5200
↓					↓				↓	↓
14H	0	0	0	1	0	1	0	0	V14H'	V10 + (V9 − V10) × (2200 + 175 × 8) / 5200
15H	0	0	0	1	0	1	0	1	V15H'	V10 + (V9 − V10) × (3600 + 150 × 1) / 5200
↓					↓				↓	↓
18H	0	0	0	1	1	0	0	0	V18H'	V10 + (V9 − V10) × (3600 + 150 × 4) / 5200
19H	0	0	0	1	1	0	0	1	V19H'	V10 + (V9 − V10) × (4200 + 150 × 1) / 5200
↓					↓				↓	↓
1CH	0	0	0	1	1	1	0	0	V1CH'	V10 + (V9 − V10) × (4200 + 150 × 4) / 5200
1DH	0	0	0	1	1	1	0	1	V1DH'	V10 + (V9 − V10) × (4800 + 100 × 1) / 5200
1EH	0	0	0	1	1	1	1	0	V1EH'	V10 + (V9 − V10) × (4800 + 100 × 2) / 5200
1FH	0	0	0	1	1	1	1	1	V1FH'	V10 + (V9 − V10) × (4800 + 100 × 3) / 5200
20H	0	0	1	0	0	0	0	0	V20H'	V9
21H	0	0	1	0	0	0	0	1	V21H'	V9 + (V8 − V9) × (100 × 1) / 4000
↓					↓				↓	↓
24H	0	0	1	0	0	1	0	0	V24H'	V9 + (V8 − V9) × (100 × 4) / 4000
25H	0	0	1	0	0	1	0	1	V25H'	V9 + (V8 − V9) × (400 + 75 × 1) / 4000
↓					↓				↓	↓
34H	0	0	1	1	0	1	0	0	V34H'	V9 + (V8 − V9) × (400 + 75 × 16) / 4000
35H	0	0	1	1	0	1	0	1	V35H'	V9 + (V8 − V9) × (1600 + 50 × 1) / 4000
↓					↓				↓	↓
3FH	0	0	1	1	1	1	1	1	V3FH'	V9 + (V8 − V9) × (1600 + 50 × 11) / 4000
40H	0	1	0	0	0	0	0	0	V40H'	V9 + (V8 − V9) × (1600 + 50 × 12) / 4000
↓					↓				↓	↓
48H	0	1	0	0	1	0	0	0	V48H'	V9 + (V8 − V9) × (1600 + 50 × 20) / 4000
49H	0	1	0	0	1	0	0	1	V49H'	V9 + (V8 − V9) × (2600 + 25 × 1) / 4000
↓					↓				↓	↓
5FH	0	1	0	1	1	1	1	1	V5FH'	V9 + (V8 − V9) × (2600 + 25 × 23) / 4000
60H	0	1	1	0	0	0	0	0	V60H'	V9 + (V8 − V9) × (2600 + 25 × 24) / 4000
↓					↓				↓	↓
7FH	0	1	1	1	1	1	1	1	V7FH'	V9 + (V8 − V9) × (2600 + 25 × 55) / 4000

GRAYSCALE DATA	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	OUTPUT VOLTAGE (ANTICIPATED VALUE)	
80H	1	0	0	0	0	0	0	0	V80H'	V8
81H	1	0	0	0	0	0	0	1	V81H'	V8 + (V7 − V8) × (25 × 1) / 2700
↓					↓				↓	↓
9FH	1	0	0	1	1	1	1	1	V9FH'	V8 + (V7 − V8) × (25 × 31) / 2700
A0H	1	0	1	0	0	0	0	0	VA0H'	V8 + (V7 − V8) × (25 × 32) / 2700
↓					↓				↓	↓
BFH	1	0	1	1	1	1	1	1	VBFH'	V8 + (V7 − V8) × (25 × 63) / 2700
C0H	1	1	0	0	0	0	0	0	VC0H'	V8 + (V7 − V8) × (25 × 64) / 2700
↓					↓				↓	↓
D4H	1	1	0	1	0	1	0	0	VD4H'	V8 + (V7 − V8) × (25 × 84) / 2700
D5H	1	1	0	1	0	1	0	1	VD5H'	V8 + (V7 − V8) × (2100 + 50 × 1) / 2700
↓					↓				↓	↓
DFH	1	1	0	1	1	1	1	1	VDFH'	V8 + (V7 − V8) × (2100 + 50 × 11) / 2700
E0H	1	1	1	0	0	0	0	0	VE0H'	V7
E1H	1	1	1	0	0	0	0	1	VE1H'	V7 + (V6 − V7) × (50 × 1) / 2700
↓					↓				↓	↓
E8H	1	1	1	0	1	0	0	0	VE8H'	V7 + (V6 − V7) × (50 × 8) / 2700
E9H	1	1	1	0	1	0	0	1	VE9H'	V7 + (V6 − V7) × (400 + 75 × 1) / 2700
↓					↓				↓	↓
F4H	1	1	1	1	0	1	0	0	VF4H'	V7 + (V6 − V7) × (400 + 75 × 12) / 2700
F5H	1	1	1	1	0	1	0	1	VF5H'	V7 + (V6 − V7) × (1300 + 100 × 1) / 2700
↓					↓				↓	↓
FCH	1	1	1	1	1	1	0	0	VFCH'	V7 + (V6 − V7) × (1300 + 100 × 8) / 2700
FDH	1	1	1	1	1	1	0	1	VFDH'	V7 + (V6 − V7) × (2100 + 200 × 1) / 2700
FEH	1	1	1	1	1	1	1	0	VFEH'	V7 + (V6 − V7) × (2100 + 200 × 2) / 2700
FFH	1	1	1	1	1	1	1	1	VFFH'	V6

- LOAD, POL, and output waveforms

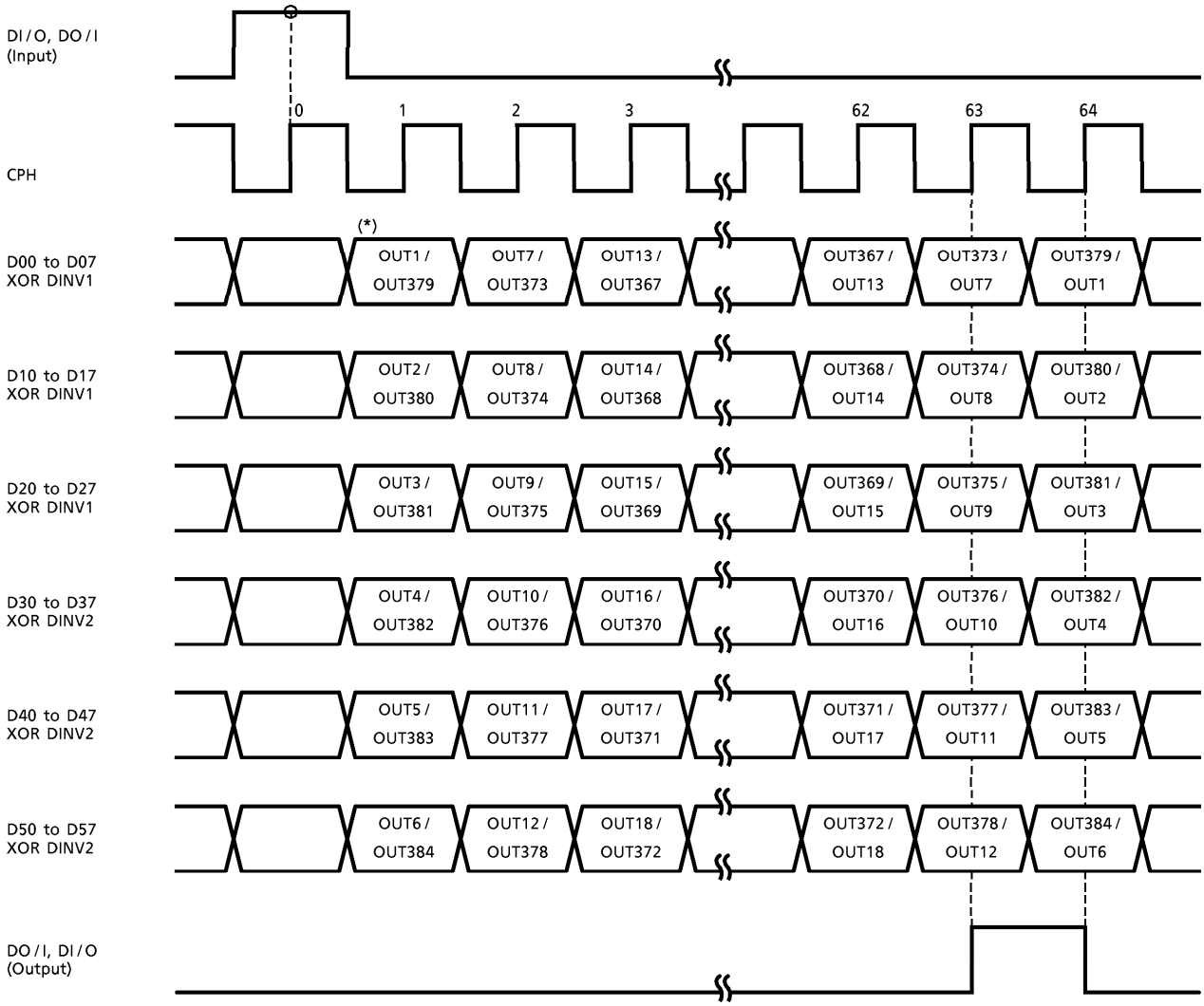


POL	OUT_{2N-1}	OUT_{2N}
L	V0 to V5	V6 to V11
H	V6 to V11	V0 to V5

* OUT_{2N-1} (odd-numbered outputs) ;
OUT_{2N} (even-numbered outputs)

TIMING DIAGRAMS 1

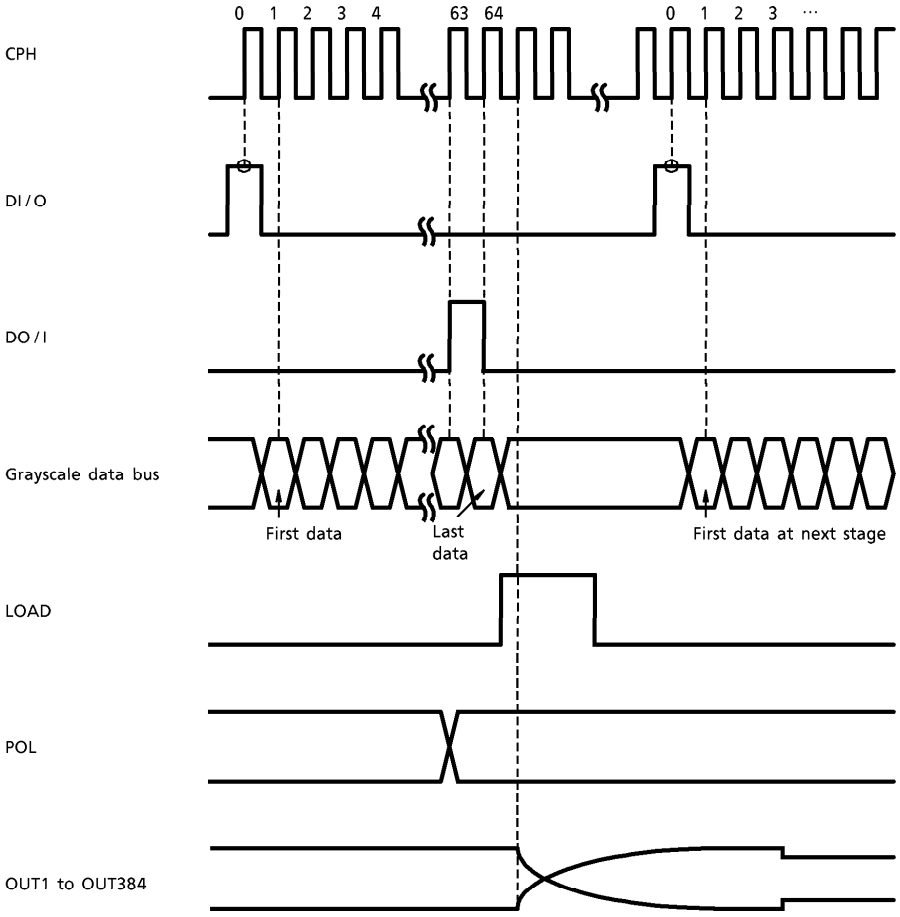
- Start pulse and data sequence



(*) Upper stage : OUT1 → U / D = high
Lower stage : OUT379 → U / D = low

TIMING DIAGRAMS 2

- Load and cascaded operations



ABSOLUTE MAXIMUM RATINGS (AV_{SS} = DV_{SS} = 0 V)

CHARACTERISTICS	SYMBOL	RATING	UNIT
Analog Supply Voltage	AV_{DD}	− 0.3 to 15.0	V
Digital Supply Voltage	DV_{DD}	− 0.3 to 6.0	V
Reference Analog Voltage	V0 to V9	− 0.3 to AV_{DD} + 0.3	V
Digital Input Voltage	V_{IN}	− 0.3 to DV_{DD} + 0.3	V
Storage Temperature	T_{stg}	− 55 to 125	°C

RECOMMENDED OPERATING CONDITIONS (AV_{SS} = DV_{SS} = 0 V)

CHARACTERISTICS	SYMBOL	TEST CONDITION	RATING	UNIT
Analog Supply Voltage	AV_{DD}	7.5 to 13.0	V	
Digital Supply Voltage	DV_{DD}	3.0 to 3.6	V	
Reference Analog Voltage	V0 to V5	0.5AV_{DD} to AV_{DD} − 0.2	V	
	V6 to V11	0.2 to 0.5AV_{DD}		
Operating Temperature	T_{OP}	− 20 to 75	°C	
Operating Frequency	f_{CPH}	22.0 to 37.5	MHz	CPH
Output Load Capacitance	C_L	200	pF / PIN	OUT1 to OUT384

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Referenced to AV_{DD} = 7.5 to 13.0 V, DV_{DD} = 3.0 to 3.6 V, AV_{SS} = DV_{SS} = 0 V, Ta = −20 to 75°C unless otherwise noted)

CHARACTERISTICS		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	RELEVANT PIN
Input Voltage	Low Level	V_{IL}	—		0		0.4 × DV_{DD}	V	Logic input
	High Level	V_{IH}			0.6 × DV_{DD}		DV_{DD}		
Output Voltage	Low Level	V_{OL}	—	I_{OL} = 1 mA	0		+0.5	V	Logic output
	High Level	V_{OH}		I_{OH} = −1 mA	DV_{DD} − 0.5		DV_{DD}		
Output Voltage Range		VDO	—		+0.2		AV_{DD} − 0.2	V	OUT1 to OUT384
Output Voltage Deviation		ΔVO	—	(Note 1)			T.B.D	mV	OUT1 to OUT384
Input Leakage Current		I_{IN}	—				1	μA	Logic input
Standby Current		ID_{STB}	—				1	μA	DV_{DD}
Current Consumption		AI_{DD}	—	(Note 2)			20	mA	AV_{DD}
		DI_{DD}		(Note 2)			5		DV_{DD}

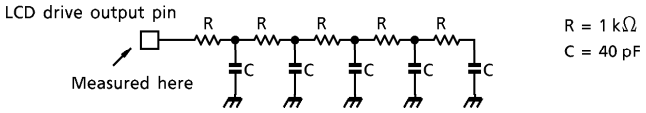
(Note 1) : Output voltage after offset correction (Typ. 210 CPH)
Please refer to Page 19 output offset timing chart.

(Note 2) : CPH = 33 MHz, 1H = 20 μs, non-load

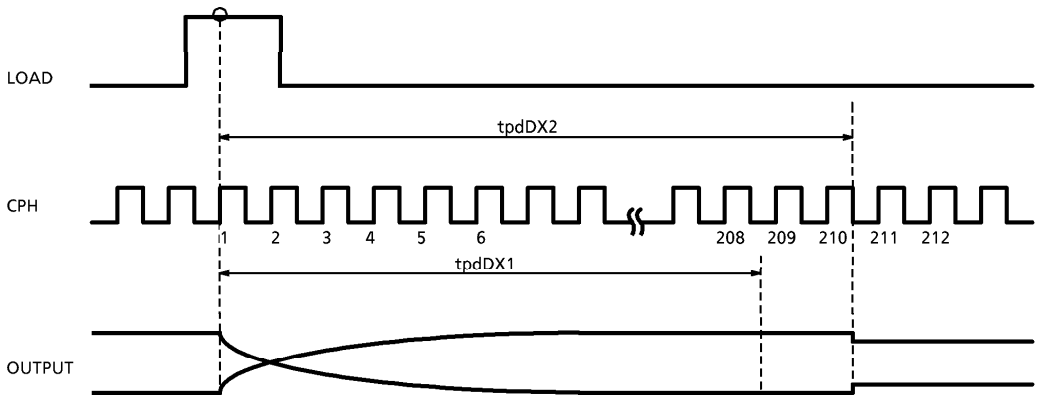
AC CHARACTERISTICS (Referenced to AV_{DD} = 7.5 to 13.0 V, DV_{DD} = 3.0 to 3.6 V, AV_{SS} = DV_{SS} = 0 V, Ta = −20 to 75°C unless otherwise noted)

CHARACTERISTICS	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
CPH Pulse Width H	tCWH	—		4			ns
CPH Pulse Width L	tCWL	—		4			ns
Enable Setup Time	tsDI	—		4			ns
Enable Hold Time	thDI	—		0			ns
Data Setup Time	tsDD	—		4			ns
Data Hold Time	thDD	—		0			ns
LOAD Setup Time	tsDL	—		4			ns
LOAD High Duration	twDL	—		2			CPH period
LOAD to Enable Input Duration	tsLD1	—		2			CPH period
LOAD to Enable Output Duration	tsLD2	—		1			CPH period
POL Setup Time	tsDP	—		4			ns
POL Hold Time	thDP	—		0			ns
Enable Output Delay Time	tpdDO	—	C_L = 25 pF			10.0	ns
Output Delay Time 1	tpdDE	—	Target output voltage × 0.9 (Note 3)			3.0	μs
Output Delay Time 2	tpdDX1	—	Target output voltage ± ΔVO (Note 3)			7.0	μs
Output Offset Correction Time	tpdDX2	—			210		CPH period

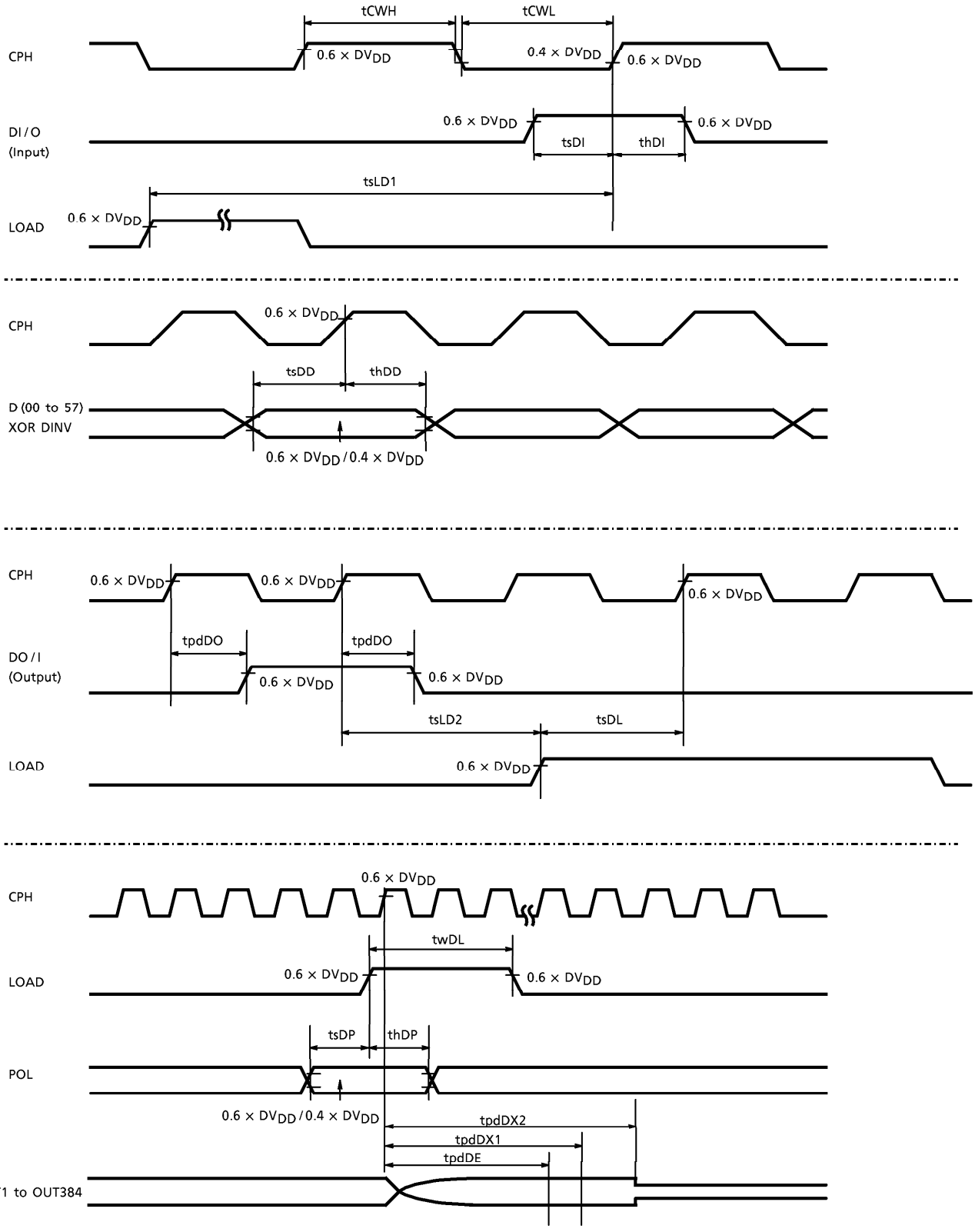
(Note 3) : Output load condition



- Output Offset Correction Timing Chart



(*) tpdDX1 : Output voltage before offset correction (Max 7 μs)
tpdDX2 : Output voltage after offset correction (Typ. 210 CPH)


tCWH
tCWL
CPH
0.6 × DVDD
0.4 × DVDD
0.6 × DVDD
DI / O
(Input)
0.6 × DVDD
0.6 × DVDD
tsDI
thDI
tsLD1
LOAD
0.6 × DVDD
CPH
0.6 × DVDD
tsDD
thDD
D (00 to 57)
XOR DINV
0.6 × DVDD / 0.4 × DVDD
CPH
0.6 × DVDD
0.6 × DVDD
0.6 × DVDD
tpdDO
tpdDO
DO / I
(Output)
0.6 × DVDD
0.6 × DVDD
tsLD2
tsDL
LOAD
0.6 × DVDD
CPH
0.6 × DVDD
twDL
LOAD
0.6 × DVDD
0.6 × DVDD
tsDP
thDP
POL
0.6 × DVDD / 0.4 × DVDD
tpdDX2
tpdDX1
tpdDE
OUT1 to OUT384