TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T C 7 M H 2 4 5 F K

Octal Bus Transceiver

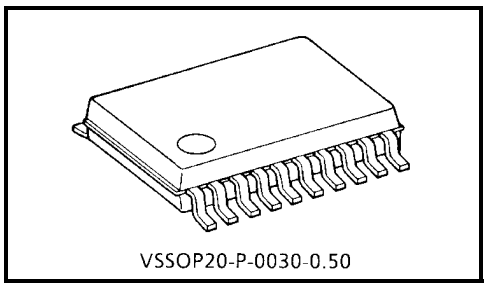
The TC7MH245FK is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.



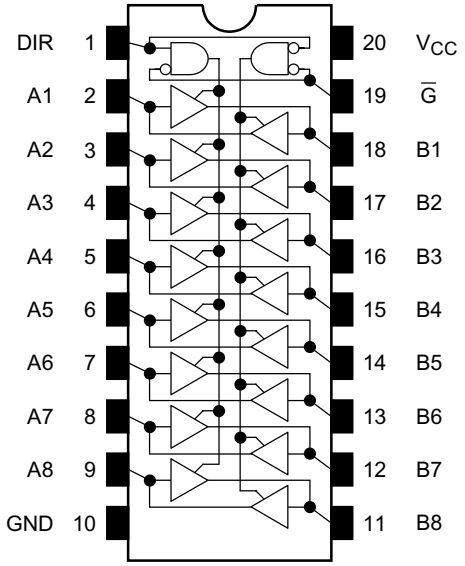
Weight: 0.03 g (typ.)

Features

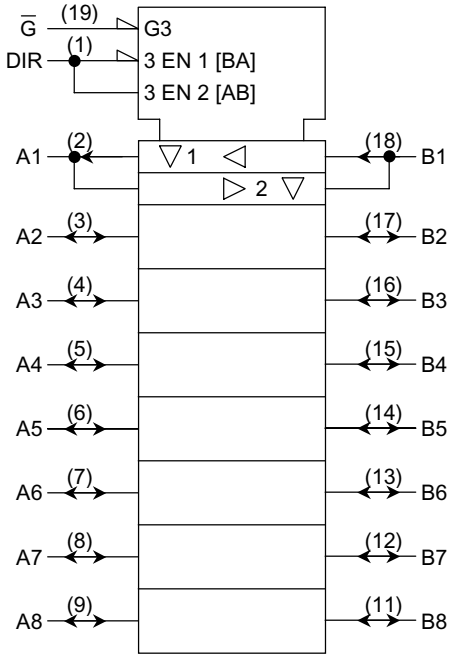
- High speed: t_{pd} = 4.0 ns (typ.) (V_{CC} = 5 V)
- Low power dissipation: I_{CC} = 4 μA (max) (Ta = 25°C)
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2~5.5 V
- Low noise: V_{OLP} = 1.0 V (max)
- Pin and function compatible with 74ALS245

Note: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.
A parasitic diode is formed between the bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5 V to 3 V systems directly.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs		Outputs	Function	
$\overline{G}$	DIR		A-Bus	B-Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	Z	

X: Don't care

Z: High impedance

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5~7.0	V
DC input voltage (DIR, $\overline{G}$)	V_{IN}	−0.5~7.0	V
DC bus I/O voltage	$V_{I/O}$	−0.5~V_{CC} + 0.5	V
Input diode current (DIR, $\overline{G}$)	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65~150	°C

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0~5.5	V
Input voltage (DIR, $\overline{G}$)	V_{IN}	0~5.5	V
Bus I/O voltage	$V_{I/O}$	0~V_{CC}	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~100 (V_{CC} = 3.3 ± 0.3 V) 0~20 (V_{CC} = 5 ± 0.5 V)	ns/V

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition		Ta = 25°C				Ta = −40~85°C		Unit
					V_{CC} (V)	Min	Typ.	Max	Min	Max	
Input voltage	High level	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
					3.0~5.5	V_{CC} × 0.7	—	—	V_{CC} × 0.7	—	
	Low level	V_{IL}	—		2.0	—	—	0.50	—	0.50	
					3.0~5.5	—	—	V_{CC} × 0.3	—	V_{CC} × 0.3	
Output voltage	High level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
					4.5	4.4	4.5	—	4.4	—	
				I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
				I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
	Low level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0	0.1	—	0.1	
					3.0	—	0	0.1	—	0.1	
					4.5	—	0	0.1	—	0.1	
				I_{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
				I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.25	−	±2.50	μA
Input leakage current		I_{IN}	V_{IN} = 5.5 V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA

AC Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	5.8	8.4	1.0	10.0	ns
				50	—	8.3	11.9	1.0	13.5	
			5.0 ± 0.5	15	—	4.0	5.5	1.0	6.5	
				50	—	5.5	7.5	1.0	8.5	
3-state output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	3.3 ± 0.3	15	—	8.5	13.2	1.0	15.5	ns
				50	—	11.0	16.7	1.0	19.0	
			5.0 ± 0.5	15	—	5.8	8.5	1.0	10.0	
				50	—	7.3	10.6	1.0	12.0	
3-state output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	3.3 ± 0.3	50	—	11.5	15.8	1.0	18.0	ns
			5.0 ± 0.5	50	—	7.0	9.7	1.0	11.0	
Output to output skew	t_{osLH} t_{osHL}	(Note1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input capacitance	C_{IN}	DIR, $\overline{G}$			—	4	10	—	10	pF
Bus input capacitance	$C_{I/O}$	A_n, B_n			—	8	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note2)			—	21	—	—	—	pF

Note1: This parameter is guaranteed by design.

$t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

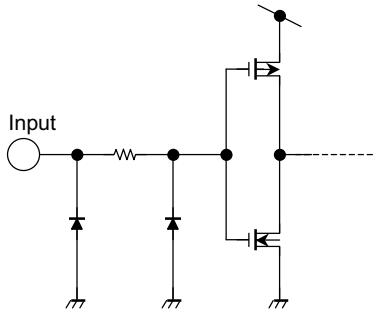
Average operating current can be obtained by the equation:

$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

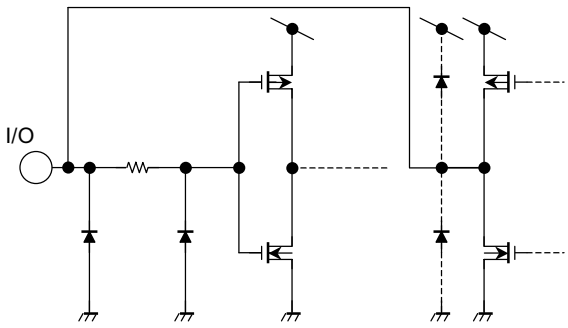
Noise Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.7	1.0	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	−0.7	−1.0	V
Minimum high level dynamic input voltage V_{IH}	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage V_{IL}	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

Input Equivalent Circuit

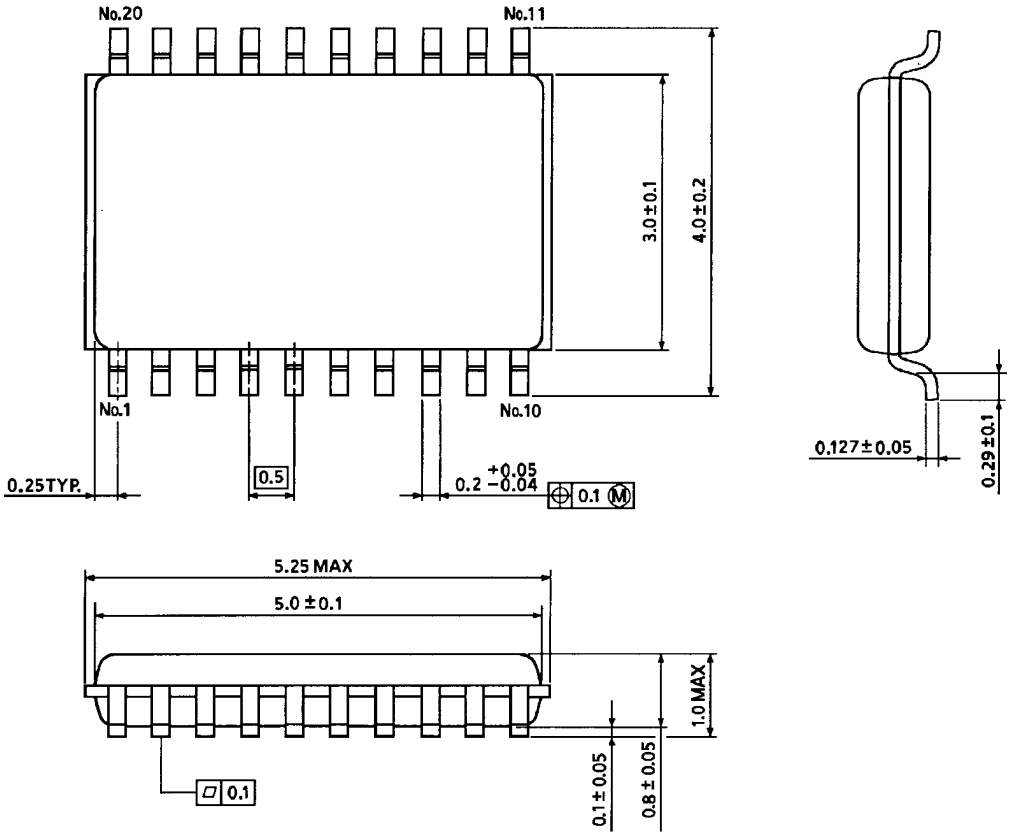


Bus Terminal Equivalent Circuit



Package Dimensions

VSSOP20-P-0030-0.50 Unit : mm



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