

TOSHIBA Transistor Silicon PNP Epitaxial S-MOS Planar Type (with built-in bias resistor)

HN7G02FU

Power Management Switch Application, Inverter Circuit Application, Driver Circuit Application and Interface Circuit Application.

- The transistor and S-MOS combined allows reduced part count, thus enabling use in small-size equipment and simple system configuration.

Q1 (transistor): RN2110 Equivalent

Q2 (MOS-FET): 2SK1830 Equivalent

Q1 Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Collector-base voltage	V_{CBO}	-50	V
Collector-emitter voltage	V_{CEO}	-50	V
Emitter-base voltage	V_{EBO}	-5	V
Collector current	I_C	-100	mA

Q2 Maximum Ratings (Ta = 25°C)

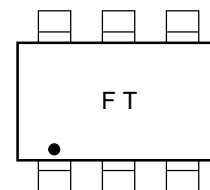
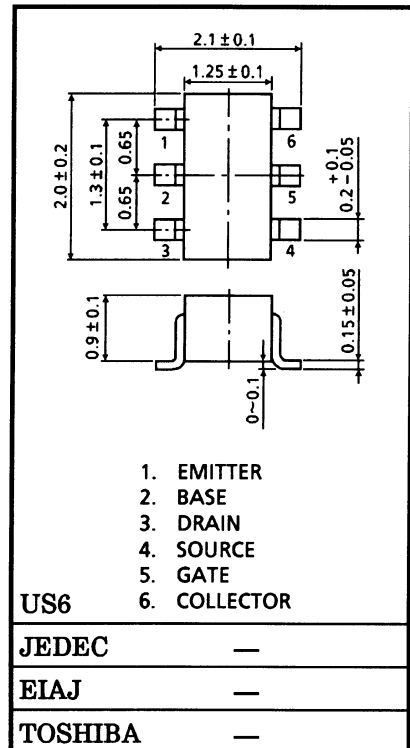
Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GSS}	10	V
DC drain current	I_D	50	mA

Q1, Q2 Common Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Collector power dissipation	P_C (Note)	200	mW
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	-55~150	°C

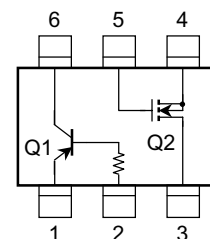
Note: Total rating

Unit in mm



Marking

Equivalent Circuit
(top view)



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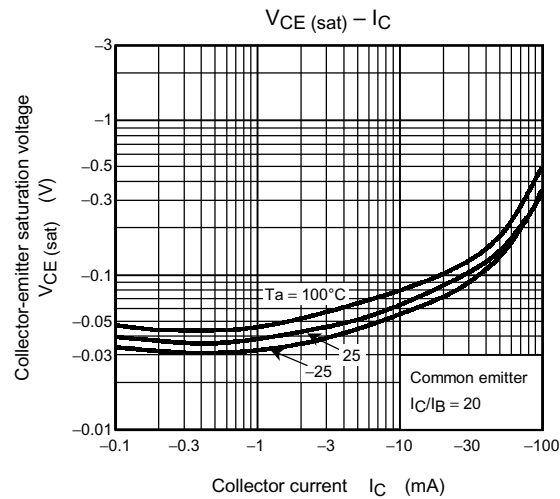
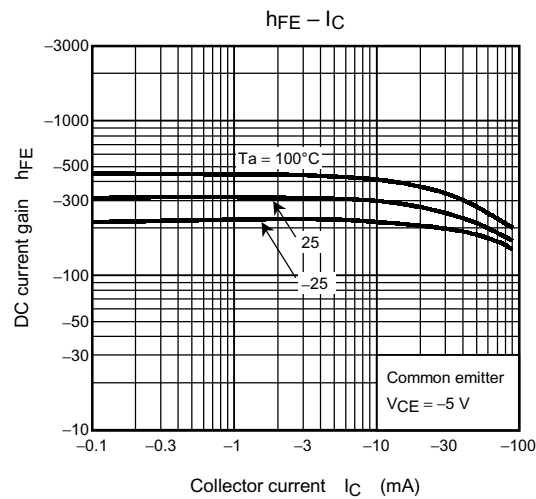
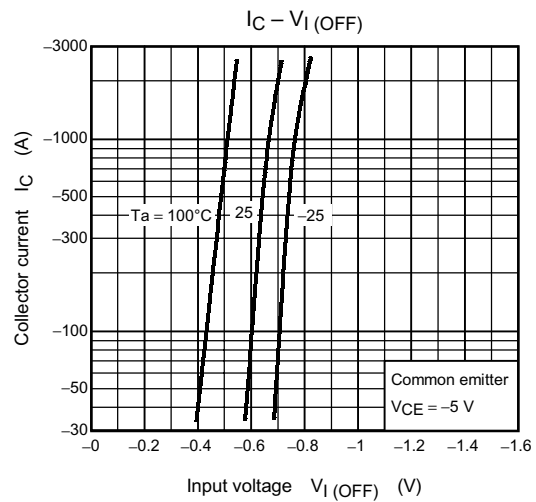
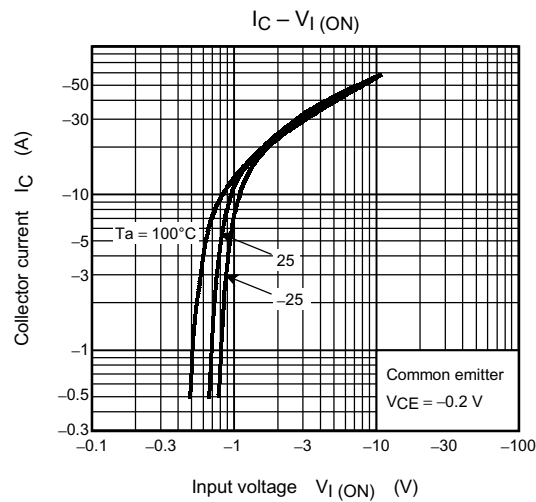
Q1 (transistor) Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current	I_{CBO}	$V_{CB} = -50\text{ V}$, $I_E = 0$	—	—	-100	nA
Emitter cut-off current	I_{EBO}	$V_{EB} = -5\text{ V}$, $I_C = 0$	—	—	-100	nA
DC current gain	h_{FE}	$V_{CE} = -5\text{ V}$, $I_C = -1\text{ mA}$	120	—	400	
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 5\text{ mA}$, $I_B = -0.25\text{ mA}$	—	-0.1	-0.3	V
Input resistor	R1	—	3.29	4.7	6.11	k Ω

Q2 (MOS-FET) Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = 10\text{ V}$, $V_{DS} = 0$	—	—	1	μA
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 100\text{ }\mu\text{A}$, $V_{GS} = 0$	20	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = 20\text{ V}$, $V_{GS} = 0$	—	—	1	μA
Gate threshold voltage	V_{th}	$V_{DS} = 3\text{ V}$, $I_D = 0.1\text{ mA}$	0.5	—	1.5	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}$, $I_D = 10\text{ mA}$	20	—	—	mS
Drain-source ON resistance	$R_{DS(ON)}$	$I_D = 10\text{ mA}$, $V_{GS} = 2.5\text{ V}$	—	20	40	Ω

Q1 (Transistor)



Q2 (MOS-FET)

(a) Switching time test circuit

