FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12535-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89850R Series

MB89855R/P857/W857

■ DESCRIPTION

The MB89850R series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to the F²MC-8L CPU core which can operate at low voltage but at high speed, the microcontrollers contain a variety of peripheral functions such as a timer unit, PWM timers, a UART, a serial interface, a 10-bit A/D converter, and an external interrupt.

The MB89850R series is applicable to a wide range of applications from consumer products to industrial equipment, including portable devices.

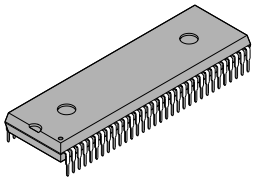
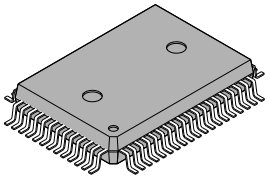
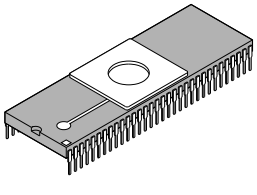
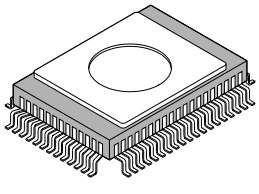
*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Various package options
  SDIP package (64 pins)/QFP package (64 pins)
- High-speed processing at low voltage
  Minimum execution time: 0.4 µs/3.5 V, 0.8 µs/2.7 V

(Continued)

■ PACKAGE

64-pin Plastic SH-DIP	64-pin Plastic QFP	64-pin Ceramic SH-DIP	64-pin Ceramic QFP
			
(DIP-64P-M01)	(FPT-64P-M06)	(DIP-64C-A06)	(FPT-64C-A02)

MB89850R Series

(Continued)

- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- 8-bit PWM timers: 2 channels
  Also usable as a reload timer
- UART
  Full-duplex double buffer
  Synchronous and asynchronous data transfer
- 8-bit serial I/O
  Switchable transfer direction allows communication with various equipment.
- 10-bit A/D converter
  Conversion time: 13.2 µs
  Activation by an external input or a timer unit capable
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
- Bus interface functions
  Including hold and ready functions
- Timer unit
  Outputs non-overlap three-phase waveforms to control an AC inverter motor.
  Also usable as a PWM timer (4 channels)

■ PRODUCT LINEUP

Parameter \ Part number	MB89855R	MB89P857 MB89W857
Classification	Mass production products (mask ROM products)	One-time PROM pruducts/EPROM products, also used for evaluation
ROM size	16 K × 8 bits (internal mask ROM)	32 K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)
RAM size	512 × 8 bits	1 K × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 µs/10 MHz Interrupt processing time: 3.6 µs/10 MHz	
Ports	Input ports: 5 (All also serve as peripherals) Output ports (N-ch open drain): 8 (All also serve as peripherals) Output ports (CMOS): 8 (All also serve as bus control pins) I/O ports (CMOS): 32 (All also serve as bus pins or peripherals) Total: 53	
Timer unit	10-bit up/down count timer × 1 Compare registers with buffer × 4 Compare timer unit clear register with buffer × 1 Zero detection pin control 4 output channels Non-overlap three-phase waveform output Independent three-phase dead-time timer	
8-bit PWM timer 1, 8-bit PWM timer 2	8-bit reload timer operation (toggled output capable, operating clock cycle: 0.4 µs to 25.6 µs) 8-bit resolution PWM operation (conversion cycle: 102 µs to 6.528 ms)	
UART	8 bits Clock synchronous/asynchronous data transfer capable	
8-bit serial I/O	8 bits LSB first/MSB first selectability One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 0.8 µs, 3.2 µs, 12.8 µs)	
10-bit A/D converter	10-bit resolution × 8 channels A/D conversion time: 13.2 µs Continous activation by a compare channel 0 in timer unit or an external activation capable	
External interrupt	4 independent channels (edge selection, interrupt vector, source flag) Rising edge/falling edge selectability. Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)	
Standby modes	Sleep mode, stop mode	
Process	CMOS	
Operating voltage*	2.7 V to 6.0 V	2.7 V to 5.5 V

* : Varies with conditions such as the operating frequency. (See section “■ Electrical Characteristics.”)

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89855R	MB89P857	MB89W857
DIP-64P-M01	○	○	×
DIP-64C-A06	×	×	○
FPT-64P-M06	○	○	×
FPT-64C-A02	×	×	○

○ : Available × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the OTPROM (one-time PROM) products (also used for evaluation), verify its differences from the product that will actually be used.

Take particular care on the following point:

- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

When operated at low speed, the product with an OTPROM or an EPROM will consume more current than the product with a mask ROM.

However, the current consumption in sleep/stop modes is the same.

3. Mask Options

In the MB89P857/W857, no option can be set.

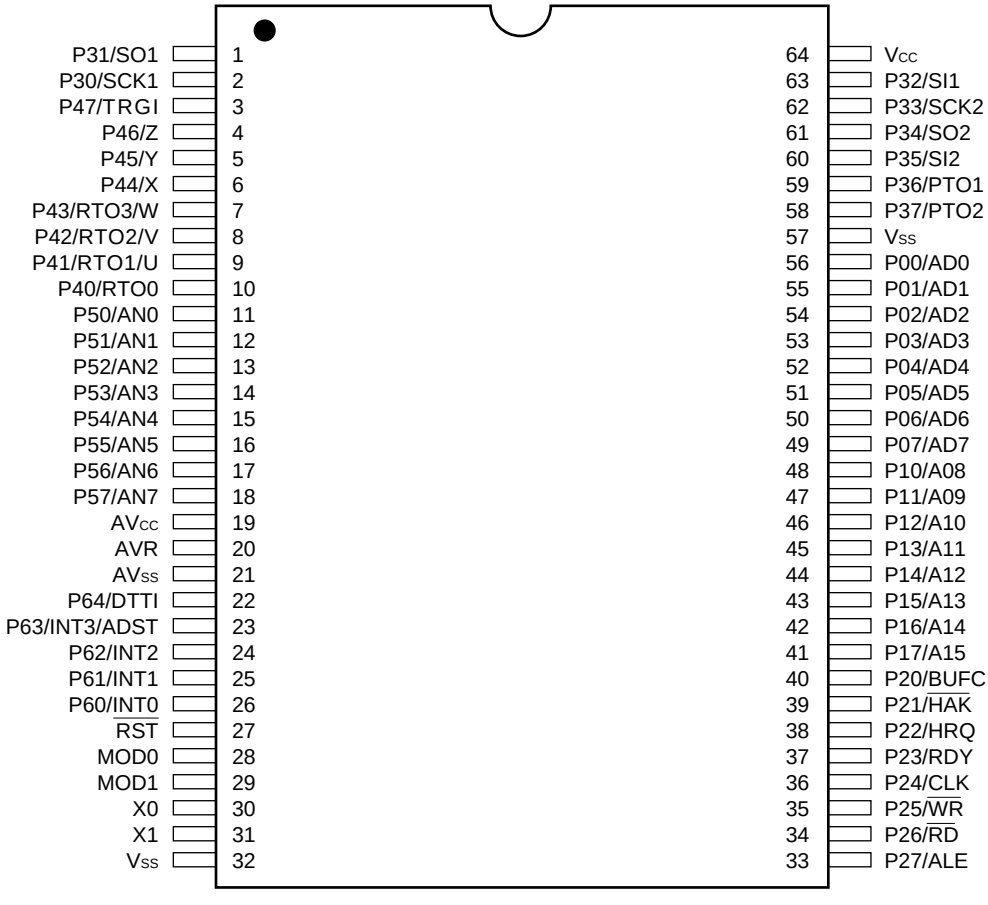
Before using options check section "■ Mask Options."

Take particular care on the following point:

- A pull-up resistor can be set for P00 to P07, P10 to P17 and P20 to P27 only at single-chip mode.

■ PIN ASSIGNMENT

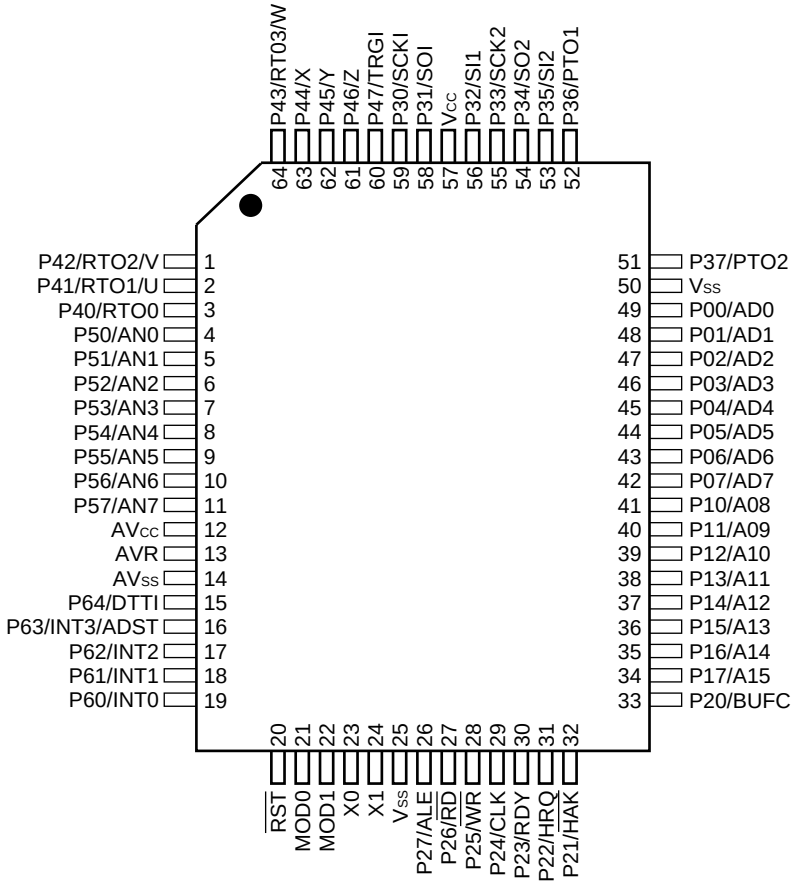
(Top view)



(DIP-64P-M01)

(DIP-64C-A06)

MB89850R Series



(FPT-64P-M06)
(FPT-64C-A02)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
SH-DIP*1	QFP*2			
30	23	X0	A	Crystal oscillator pins (10 MHz)
31	24	X1		
28	21	MOD0	B	Operating mode selection pins Connect directly to V_{CC} or V_{SS}.
29	22	MOD1		
27	20	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
56 to 49	49 to 42	P00/AD0 to P07/AD7	D	General-purpose I/O ports When an external bus is used, these ports function as multiplex pins of lower address output and data I/O.
48 to 41	41 to 34	P10/A08 to P17/A15	D	General-purpose I/O ports When an external bus is used, these ports function as upper address output.
40	33	P20/BUFC	F	General-purpose output port When an external bus is used, this port can also be used as a buffer control output.
39	32	P21/$\overline{HAK}$	F	General-purpose output port When an external bus is used, this port can also be used as a hold acknowledge output.
38	31	P22/HRQ	D	General-purpose output port When an external bus is used, this port can also be used as a hold request input.
37	30	P23/RDY	D	General-purpose output port When an external bus is used, this port functions as a ready input.
36	29	P24/CLK	F	General-purpose output port When an external bus is used, this port functions as a clock output.
35	28	P25/$\overline{WR}$	F	General-purpose output port When an external bus is used, this port functions as a write signal output.
34	27	P26/$\overline{RD}$	F	General-purpose output port When an external bus is used, this port functions as a read signal output.
33	26	P27/ALE	F	General-purpose output port When an external bus is used, this port functions as an address latch signal output.
2	59	P30/SCK1	E	General-purpose I/O port Also serves as the clock I/O for the UART. This port is a hysteresis input type.

(Continued)

*1: DIP-64P-M01, DIP-64C-A06

*2: FPT-64P-M06, FPT-64C-A02

(Continued)

Pin no.		Pin name	Circuit type	Function
SH-DIP*1	QFP*2			
1	58	P31/SO1	E	General-purpose I/O port Also serves as the data output for the UART. This port is a hysteresis input type.
63	56	P32/SI1	E	General-purpose I/O port Also serves as the data input for the UART. This port is a hysteresis input type.
62	55	P33/SCK2	E	General-purpose I/O port Also serves as the clock I/O for the 8-bit serial I/O. This port is a hysteresis input type.
61	54	P34/SO2	E	General-purpose I/O port Also serves as the data output for the 8-bit serial I/O. This port is a hysteresis input type.
60	53	P35/SI2	E	General-purpose I/O port Also serves as the data input for the 8-bit serial I/O. This port is a hysteresis input type.
59	52	P36/PTO1	E	General-purpose I/O port Also serves as the pulse output for the 8-bit PWM timer 1. This port is a hysteresis input type.
58	51	P37/PTO2	E	General-purpose I/O port Also serves as the pulse output for the 8-bit PWM timer 2. This port is a hysteresis input type.
10	3	P40/RTO0	E	General-purpose I/O port Also serves as the pulse output for the timer unit. This port is a hystereisis input type.
9, 8, 7	2, 1, 64	P41/RTO1/U, P42/RTO2/V, P43/RTO3/W	E	General-purpose I/O ports Also serve as the pulse output or non-overlap three-phase waveform output for the timer unit. These ports are a hysteresis input type.
6, 5, 4	63, 62, 61	P44/X, P45/Y, P46/Z	E	General-purpose I/O ports Also serve as a non-overlap three-phase waveform output. These ports are a hysteresis input type.
3	60	P47/TRGI	E	General-purpose I/O port Also serves as the trigger input for the timer unit. This port is a hysteresis input type.
11 to 18	4 to 11	P50/AN0 to P57/AN7	G	N-ch open-drain output ports Also serve as the analog input for the A/D converter.
26 to 24	19 to 17	P60/INT0 to P62/INT2	H	General-purpose input ports Also serve as an external interrupt input. These ports are a hysteresis input type.
23	16	P63/INT3/ ADST	H	General-purpose input port Also serves as an external interrupt input and as the activation trigger input for the A/D converter. This port is a hysteresis input type.

(Continued)

*1: DIP-64P-M01, DIP-64C-A06

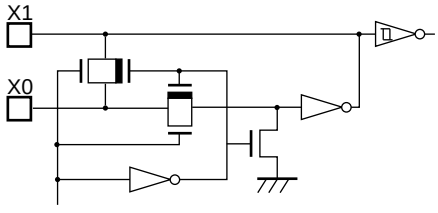
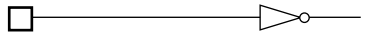
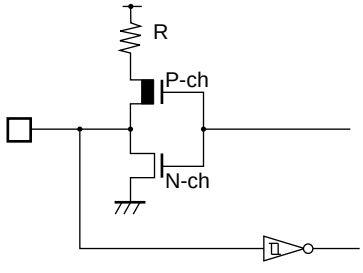
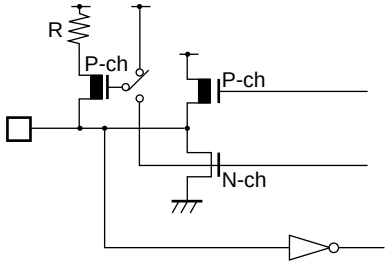
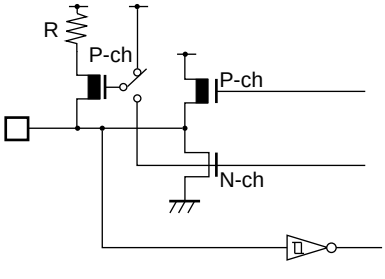
*2: FPT-64P-M06, FPT-64C-A02

(Continued)

Pin no.		Pin name	Circuit type	Function
SH-DIP*1	QFP*2			
22	15	P64/DTTI	H	General-purpose input port Also serves as a dead-time timer disable input. This port is a hysteresis input type. DTTI input is with a noise canceller.
64	57	V_{CC}	—	Power supply pin
32, 57	25, 50	V_{SS}	—	Power supply (GND) pins
19	12	AV_{CC}	—	A/D converter power supply pin
20	13	AVR	—	A/D converter reference voltage input pin
21	14	AV_{SS}	—	A/D converter power supply (GND) pin Use this pin at the same voltage as V_{SS}.

*1: DIP-64P-M01, DIP-64C-A06
*2: FPT-64P-M06, FPT-64C-A02

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		
C		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D		• CMOS output • CMOS input • Pull-up resistor optional (Mask ROM products) • At a pull-up resistor of approximately 50 kΩ/5.0 V
E		• CMOS output • Hysteresis input • Pull-up resistor optional (Mask ROM products) • At a pull-up resistor of approximately 50 kΩ/5.0 V

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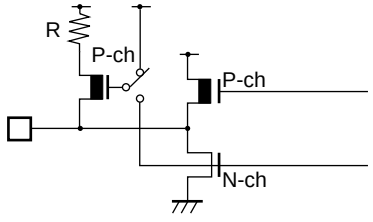
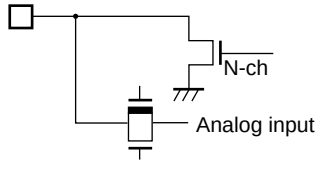
Type	Circuit	Remarks
F		• CMOS output • Pull-up resistor optional (Mask ROM products) • At a pull-up resistor of approximately 50 kΩ/5.0 V
G		• N-ch open-drain output • Analog input
H		• Hysteresis input • Pull-up resistor optional (Mask ROM products) • At a pull-up resistor of approximately 50 kΩ/5.0 V

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pin

Be sure to leave (internally connected) N.C. pin open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P857/W857

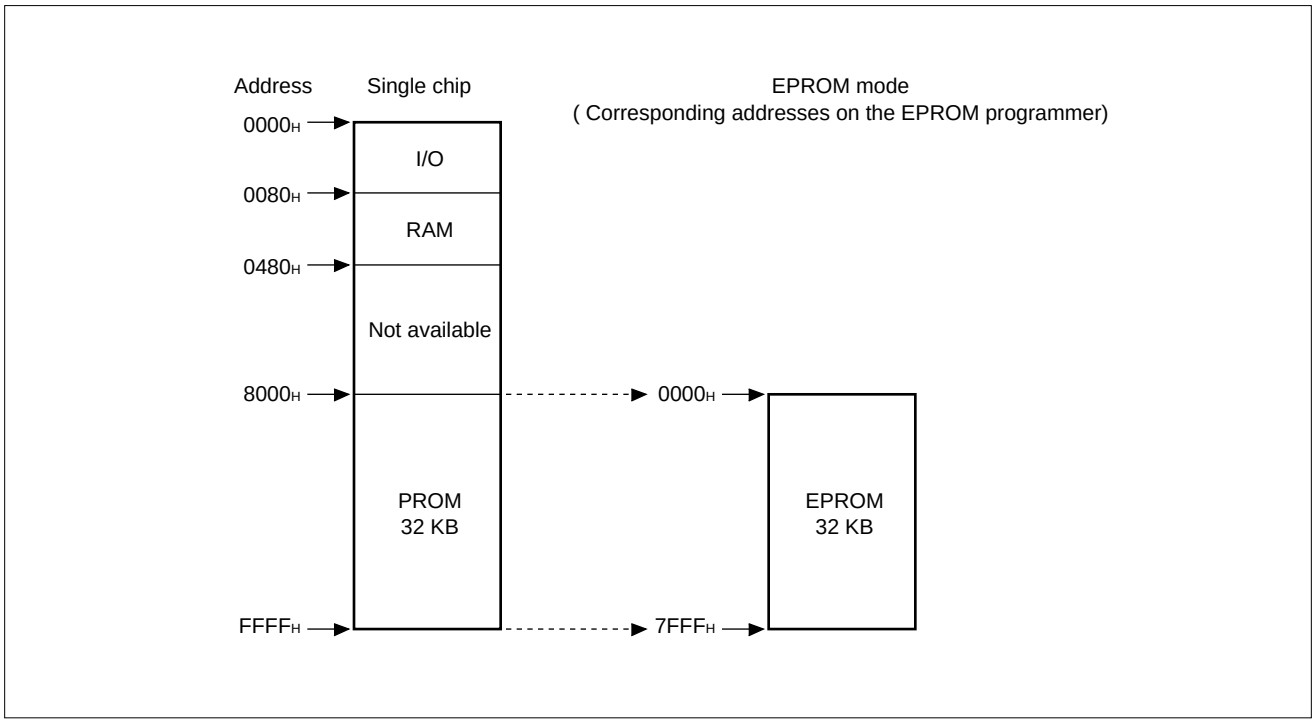
The MB89P857/W857 are an OTPROM version of the MB89850R series.

1. Features

- 32-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P857/W857 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

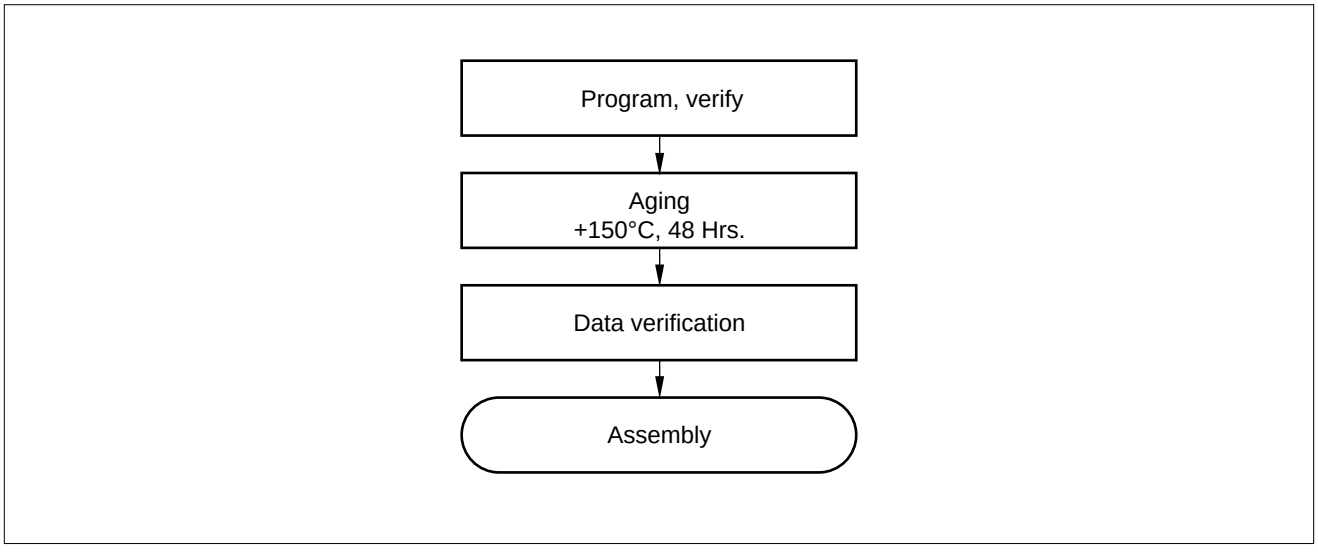
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$ (note that addresses 8000_H to $FFFF_H$ while operating as a single chip assign to addresses 0000_H to $7FFF_H$ in EPROM mode.)

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the internal EPROM to an ultraviolet light source. A dosage of 10 W-seconds/cm^2 is required to completely erase an internal EPROM. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000 µW/cm^2 for 15 to 21 minutes. The internal EPROM should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the internal EPROM and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure time will be much longer than with UV source at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the internal EPROM, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

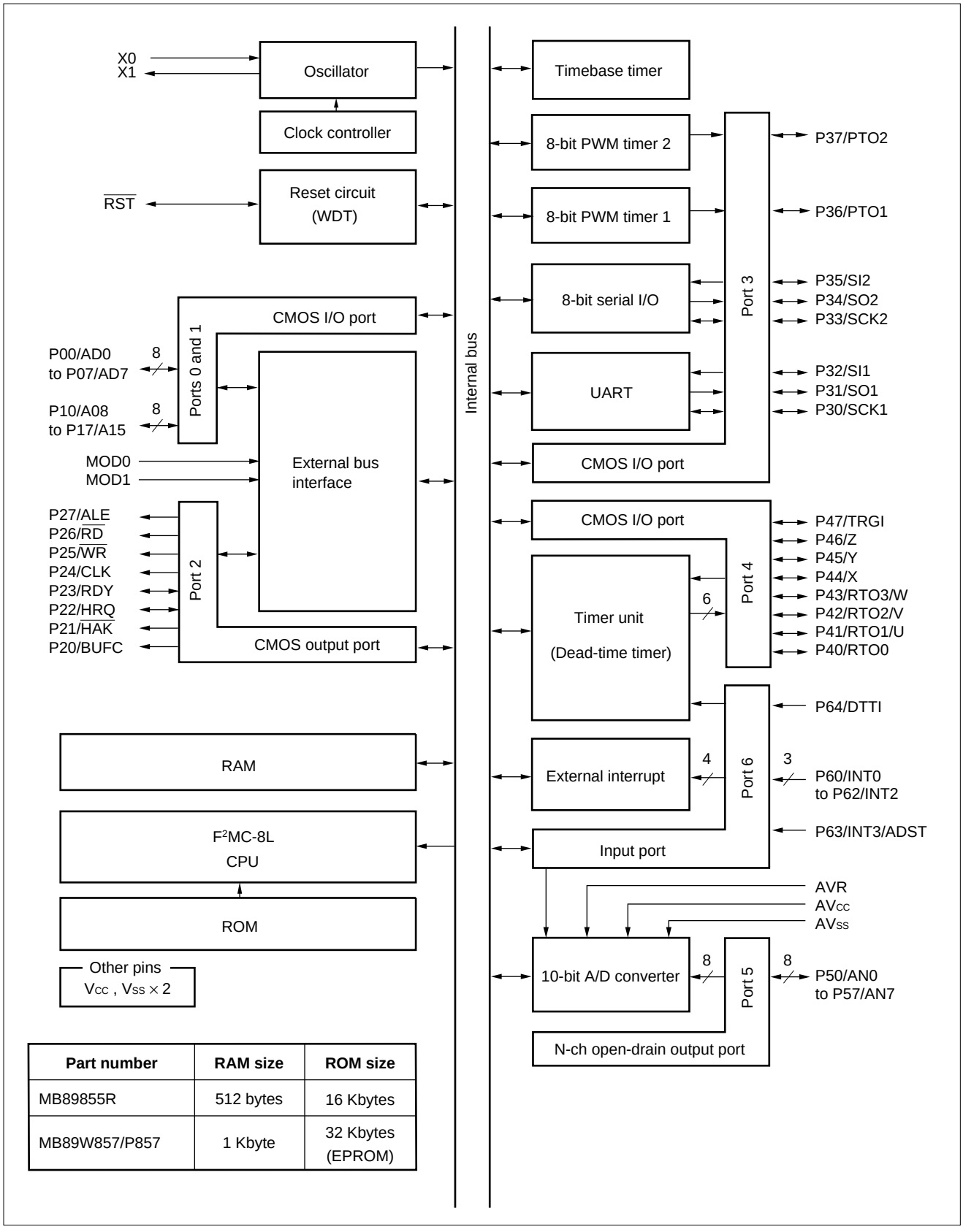
7. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
DIP-64P-M01	ROM-64SD-28DP-8L*
FPT-64P-M06	ROM-64QF-28DP-8L
FPT-64P-A02	ROM-64QF-28DP-8L5

* : Connect the adapter jumper pin to V_{SS} when using.

Inquiry: Sun Hayato Co., Ltd.: Fax 81-3-5396-9106

■ BLOCK DIAGRAM



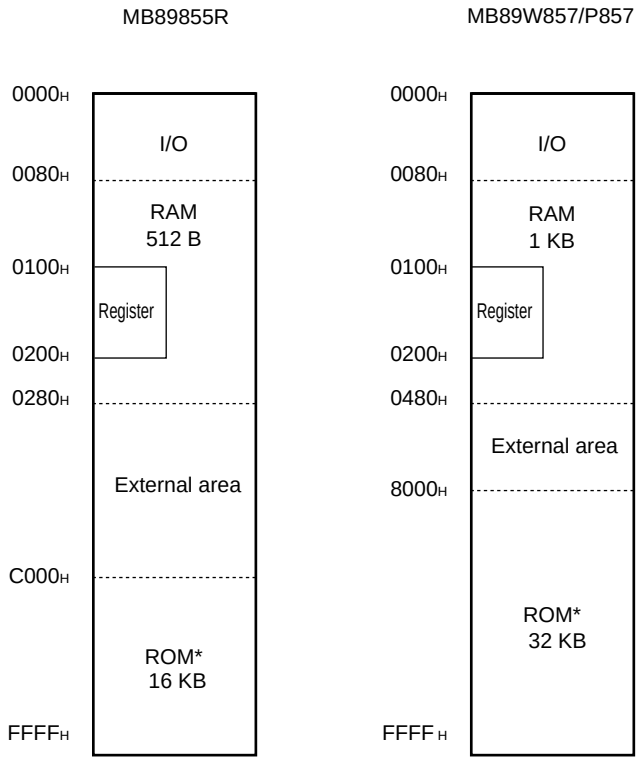
Part number	RAM size	ROM size
MB89855R	512 bytes	16 Kbytes
MB89W857/P857	1 Kbyte	32 Kbytes (EPROM)

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89850R series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89860/850 series is structured as illustrated below.

- **Memory Space**

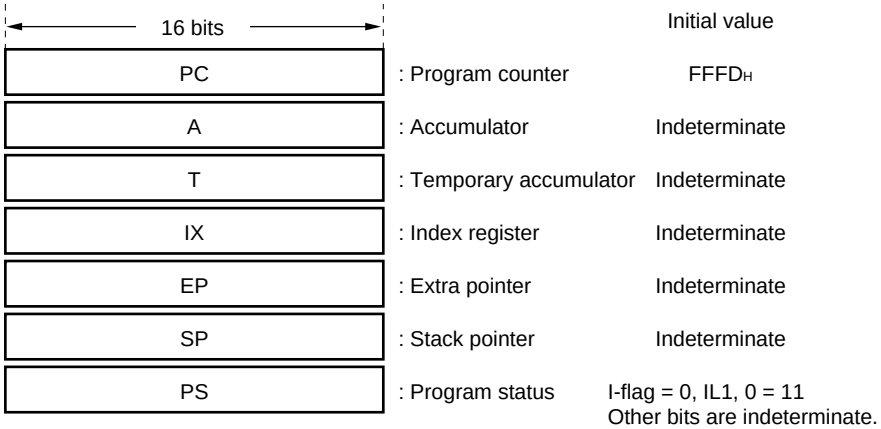


*: The ROM area is an external area depending on the mode.

2. Registers

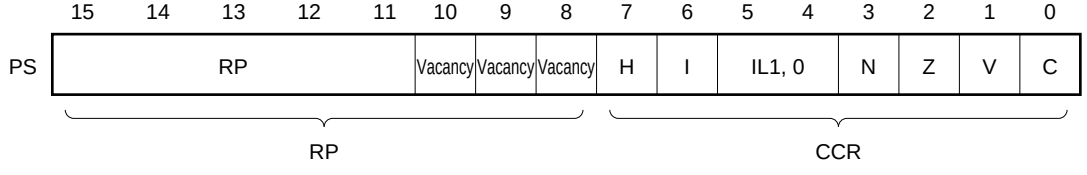
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



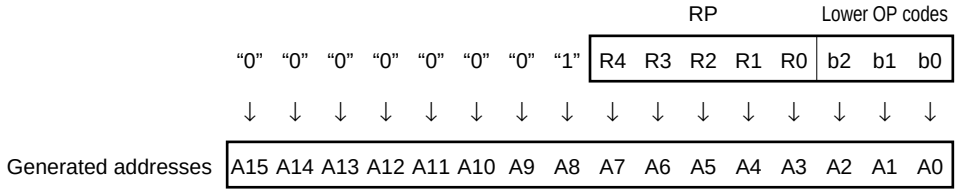
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

- **Structure of the Program Status Register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High ↕ Low = no interrupt
0	1		
1	0	2	
1	1	3	

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

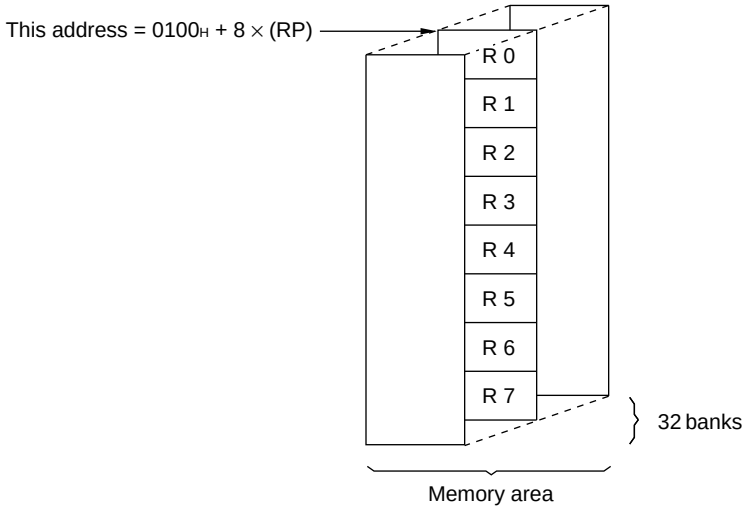
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89850R series. The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

- **Register Bank Configuration**



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(W)	BCTR	External bus pin control register
06H			Vacancy
07H			Vacancy
08H	(R/W)	STBC	Standby control register
09H	(W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBTC	Timebase timer control register
0BH			Vacancy
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(W)	DDR4	Port 4 data direction register
10H	(R/W)	PDR5	Port 5 data register
11H			Vacancy
12H	(R)	PDR6	Port 6 data register
13H			Vacancy
14H	(R/W)	PDR7	Port 7 data register
15H			Vacancy
16H	(R/W)	PDR8	Port 8 data register
17H to 1BH			Vacancy
1CH	(R/W)	CTR1	PWM control register 1
1DH	(W)	CMR1	PWM compare register 1
1EH	(R/W)	CTR2	PWM control register 2
1FH	(W)	CMR2	PWM compare register 2
20H	(R/W)	SMC	UART serial mode control register
21H	(R/W)	SRC	UART serial rate control register
22H	(R/W)	SSD	UART serial status/data register
23H	(R/W)	SIDR/SODR	UART serial data register
24H	(R/W)	SMR	Serial mode register
25H	(R/W)	SDR	Serial data register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
26H	(R/W)	EIC1	External interrupt control register 1
27H	(R/W)	EIC2	External interrupt control register 2
28H	(R/W)	ADC1	A/D converter control register 1
29H	(R/W)	ADC2	A/D converter control register 2
2AH	(R)	ADDH	A/D converter data register (H)
2BH	(R)	ADDL	A/D converter data register (L)
2CH			Vacancy
2DH	(W)	ZOCTR	Zero detection output control register
2EH	(W)	CLRBRH	Compare clear buffer register (H)
2FH	(W)	CLRBRL	Compare clear buffer register (L)
30H	(R/W)	TCSR	Timer control status register
31H	(R/W)	CICR	Compare interrupt control register
32H	(R/W)	TMCR	Timer mode control register
33H	(R/W)	COER	Compare/port selection register
34H	(R/W)	CMCR	Compare buffer mode control register
35H	(R/W)	DTCR	Dead-time timer control register
36H	(W)	DTSR	Dead-time setting register
37H	(R/W)	OCTBR	Output control buffer register
38H	(W)	OCPBR0H	Output compare buffer register 0 (H)
39H	(W)	OCPBR0L	Output compare buffer register 0 (L)
3AH	(W)	OCPBR1H	Output compare buffer register 1 (H)
3BH	(W)	OCPBR1L	Output compare buffer register 1 (L)
3CH	(W)	OCPBR2H	Output compare buffer register 2 (H)
3DH	(W)	OCPBR2L	Output compare buffer register 2 (L)
3EH	(W)	OCPBR3H	Output compare buffer register 3 (H)
3FH	(W)	OCPBR3L	Output compare buffer register 3 (L)
40H to 7BH			Vacancy
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH			Vacancy

Notes: • Do not use vacancies.
• When a read-modify-write instruction (such as bit set) is used to access a write-only register or a register containing a write-only bit, a bit designated by the instruction will have a predetermined value. However, a write-only bit included, if any, in bits not defined by the instruction will cause a malfunction. So no access to the register should be tried with any read-modefy-write instruction.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	*
A/D converter reference input voltage	AVR	V_{SS} – 0.3	V_{SS} + 7.0	V	AVR must not exceed AV_{CC} + 0.3 V.
Program voltage	V_{PP}	V_{SS} – 0.3	13.0	V	MOD1 pins of MB89P857/ W857
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 0.3	V	
“L” level maximum output current	I_{OL}	—	20	mA	
“L” level average output current	I_{OLAV1}	—	4	mA	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57
	I_{OLAV2}	—	15	mA	P40 to P47
“L” level total average output current	$\sum I_{OLAV1}$	—	30	mA	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57
	$\sum I_{OLAV2}$	—	50	mA	P40 to P47
“H” level maximum output current	I_{OH}	—	–20	mA	
“H” level average output current	I_{OHAV}	—	–4	mA	
“H” level total maximum output current	$\sum I_{OH}$	—	–20	mA	
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*: Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

WARNING: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

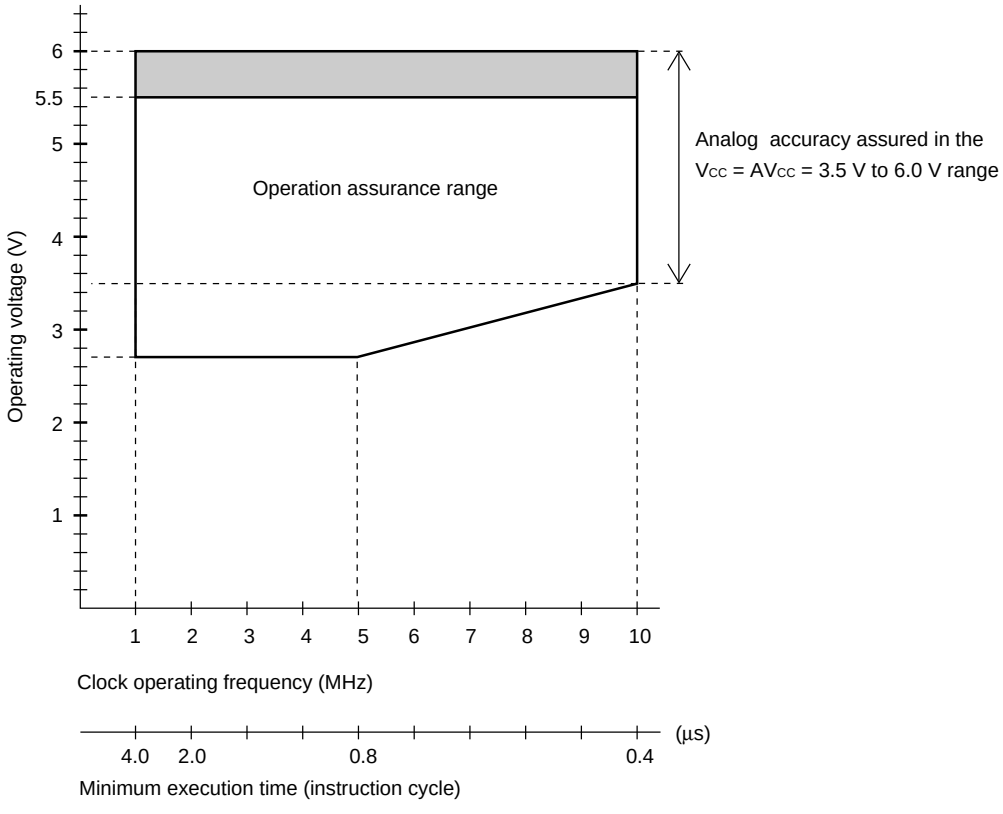
2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	2.7*	6.0*	V	Normal operation assurance range* MB89855R
		2.7*	5.5*	V	Normal operation assurance range* MB89P857/W855
		1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	0.0	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

*: These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and “5. A/D Converter Electrical Characteristics.”

Note: Connect the MOD0 and MOD1 pins to V_{CC} or V_{SS}.



Note: The shaded area is assured only for the MB89855R.

Figure 1 Operating Voltage vs. Clock Operating Frequency

3. DC Characteristics

(AV_{CC} = V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P22, P23	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, P30 to P37, P40 to P47, P60 to P64	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P22, P23	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, P30 to P37, P40 to P47, P60 to P64	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47	I_{OH} = –2.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P57	I_{OL} = +1.8 mA	—	—	0.4	V	
	V_{OL2}	P40 to P47	I_{OL} = +1.5 mA	—	—	1.5	V	
Input leackage current	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P64, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	
Pull-up resistance	R_{PULL}	$\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor
Power supply current	I_{CC}	V_{CC}	F_C = 10 MHz Normal operation mode (External clock)	—	15	18	mA	
	I_{CCS}		F_C = 10 MHz Sleep mode (External clock)	—	6	8	mA	
	I_{CCH}		Stop mode T_A = +25°C	—	—	10	µA	
	I_A	AV_{CC}	F_C = 10 MHz, when A/D conversion is activated	—	6	—	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

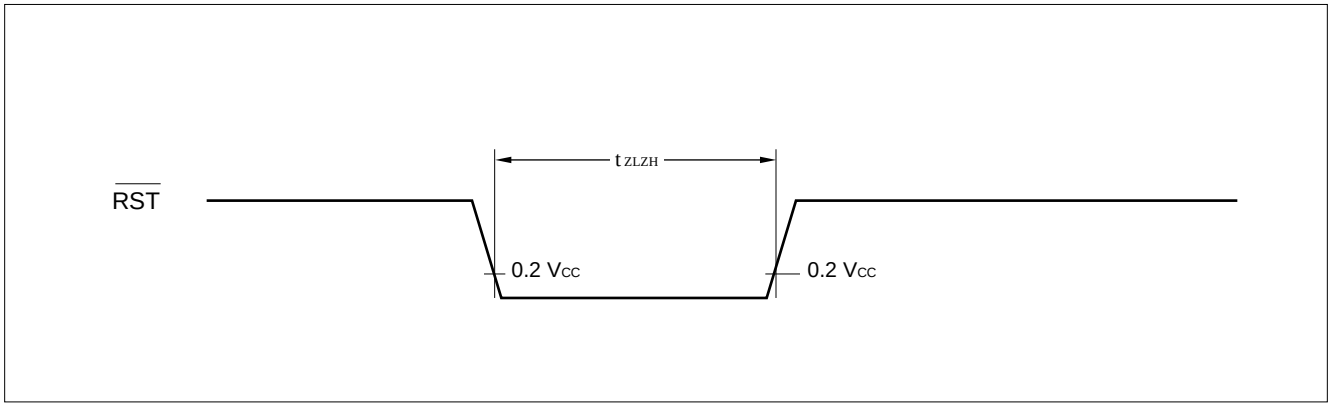
4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	16 t_{XCYL}*	—	ns	

* : t_{XCYL} is the oscillation cycle (1/F_C) to input to the X0 pin.

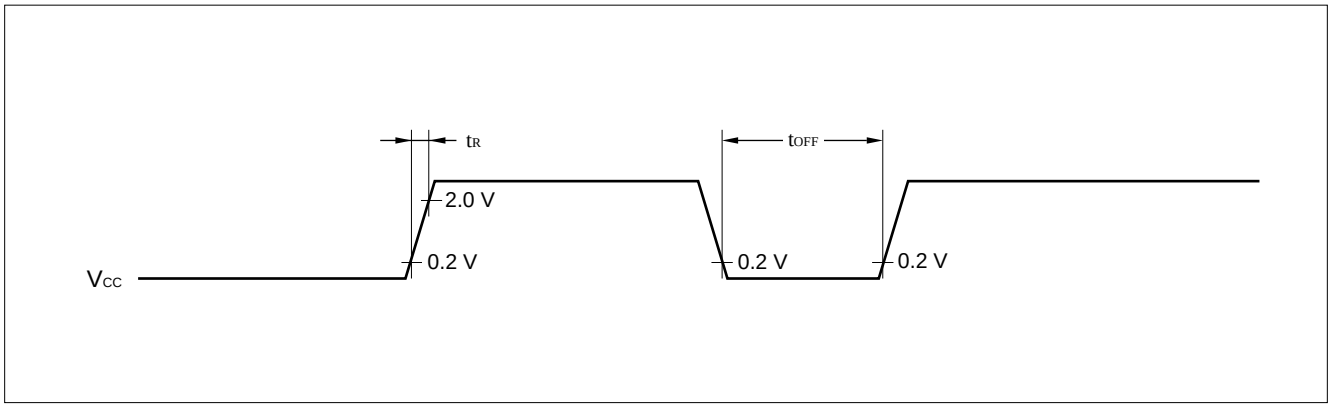


(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

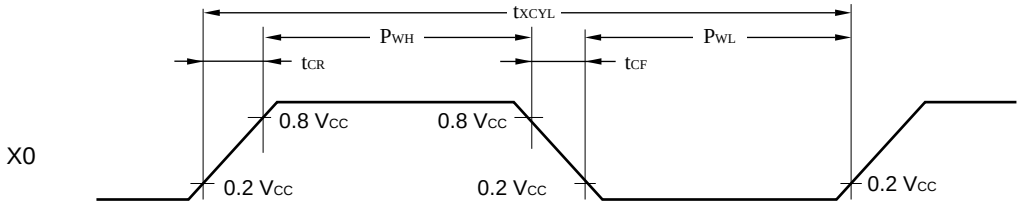


(3) Clock Timing

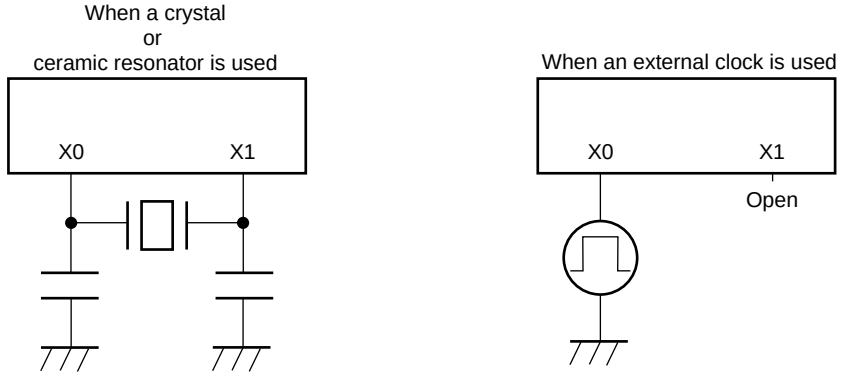
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	—	1	10	MHz	
Clock cycle time	t_{XCYL}			100	1000	ns	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}			—	10	ns	External clock

- **X0 and X1 Timing Conditions**



- **Clock Conditions**



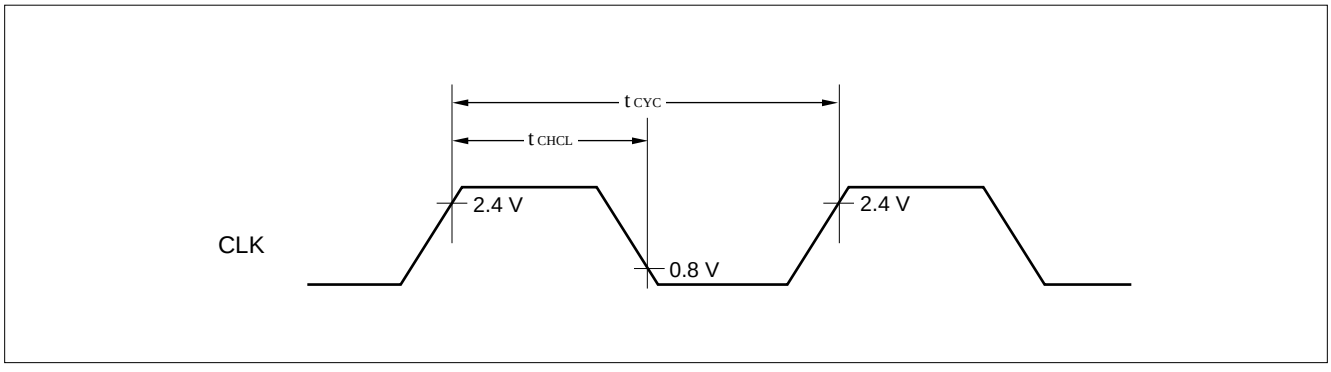
(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	4/F_C	µs	t_{inst} = 0.4 µs when operating at F_C = 10 MHz

(5) Clock Output Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	Load condition: 50 pF	200	—	ns	$t_{XCYL} \times 2$ at 10 MHz oscillation
CLK ↑ → CLK ↓	t_{CHCL}			30	100	ns	Approx. $t_{CYC}/2$ at 10 MHz oscillation

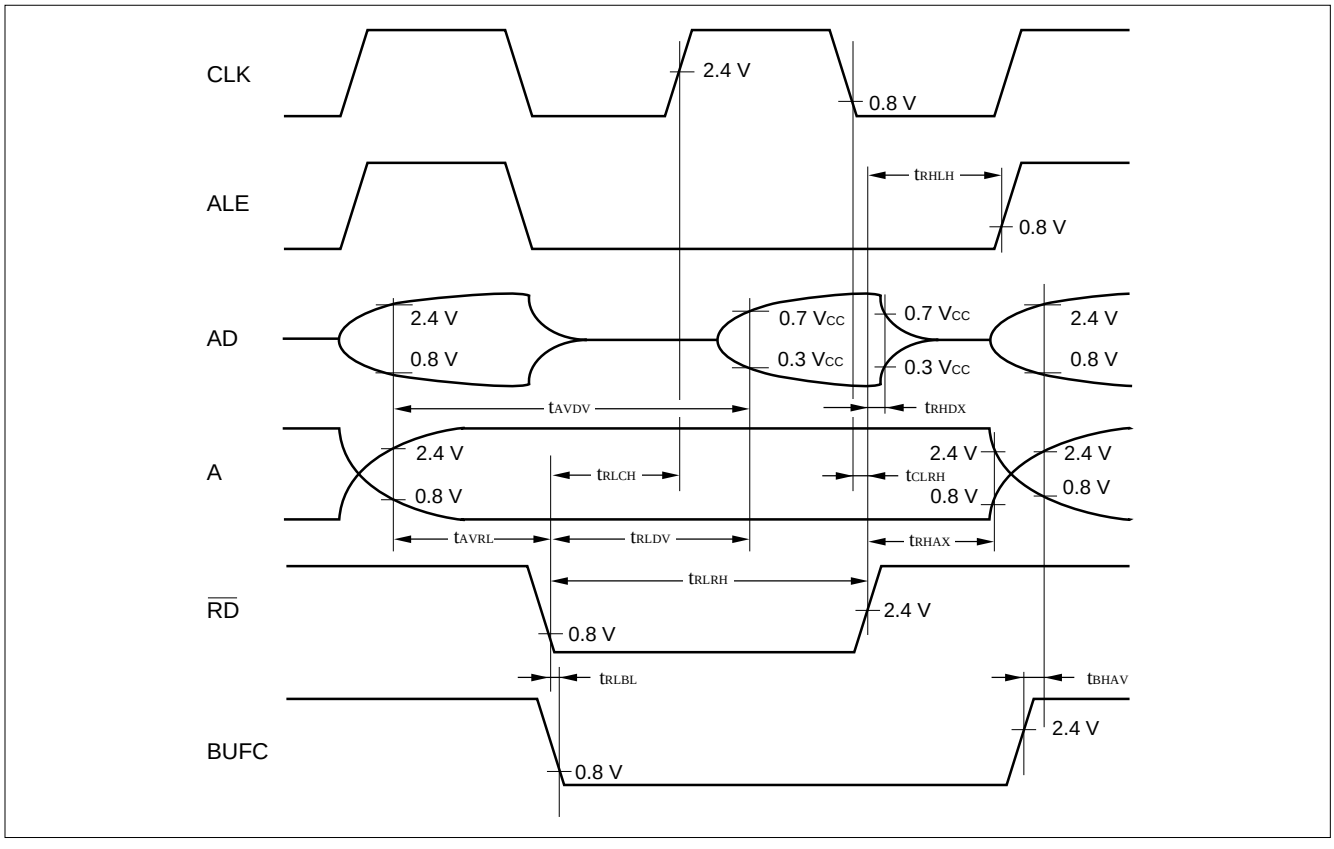


(6) Bus Read Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value (10 MHz)		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, A15 to A08, AD7 to AD0	Load condition: 50 pF	1/4 t_{inst}* – 64 ns	—	ns	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		1/2 t_{inst}* – 20 ns	—	ns	
Valid address → data read time	t_{AVDV}	AD7 to AD0, A15 to A08		—	1/2 t_{inst}*	ns	No wait
$\overline{RD}$ ↓ → data read time	t_{RLDV}	$\overline{RD}$, AD7 to AD0		—	1/2 t_{inst}* – 80 ns	ns	No wait
$\overline{RD}$ ↑ → data hold time	t_{RHDX}	AD7 to AD0, $\overline{RD}$		0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1/4 t_{inst}* – 40 ns	—	ns	
$\overline{RD}$ ↑ → address invalid time	t_{RHAX}	$\overline{RD}$, A15 to A08		1/4 t_{inst}* – 40 ns	—	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1/4 t_{inst}* – 60 ns	—	ns	
CLK ↓ → $\overline{RD}$ ↑ time	t_{CLRH}			0	—	ns	
$\overline{RD}$ ↓ → BUFC ↓ time	t_{RLBL}	$\overline{RD}$, BUFC		–5	—	ns	
BUFC ↑ → valid address time	t_{BHAV}	A15 to A08, AD7 to AD0, BUFC		5	—	ns	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



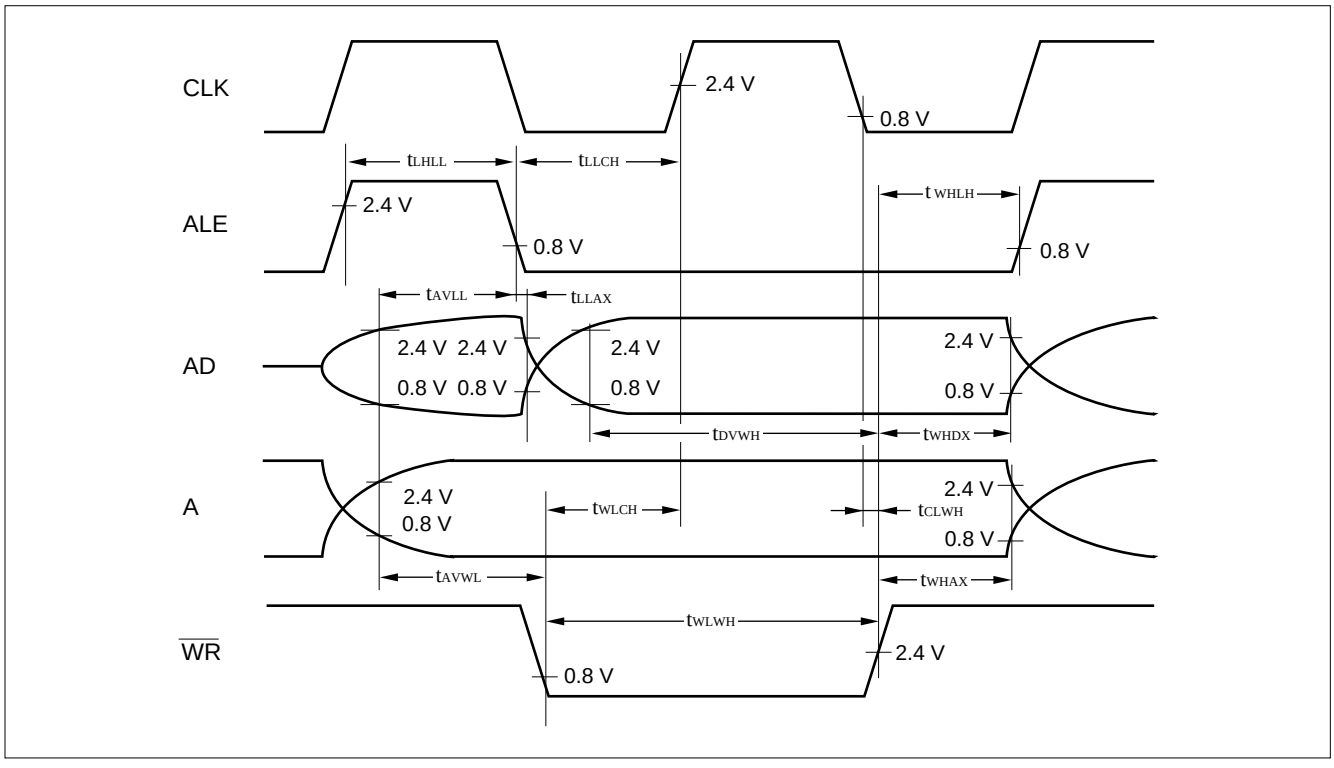
(7) Bus Write Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value (10 MHz)		Unit	Remarks
				Min.	Max.		
Valid address → ALE ↓ time	t_{AVLL}	AD7 to AD0, ALE, A15 to A08	Load condition: 50 pF	1/4 t_{inst}*1 – 64 ns	—	ns	
ALE ↓ time → address invalid time	t_{LLAX}			5	—	ns	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 60 ns	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		1/2 t_{inst}*1 – 20 ns	—	ns	
Write data → $\overline{WR}$ ↑ time	t_{DVWH}	AD7 to AD0, $\overline{WR}$		1/2 t_{inst}*1 – 60 ns	—	ns	
$\overline{WR}$ ↑ → address invalid time	t_{WHAX}	$\overline{WR}$, A15 to A08		1/4 t_{inst}*1 – 40 ns	—	ns	
$\overline{WR}$ ↑ → data hold time	t_{WHDX}	AD7 to AD0, $\overline{WR}$		1/4 t_{inst}*1 – 40 ns	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		1/4 t_{inst}*1 – 40 ns	—	ns	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		1/4 t_{inst}*1 – 60 ns	—	ns	
CLK ↓ → $\overline{WR}$ ↑ time	t_{CLWH}			0	—	ns	
ALE pulse width	t_{LHLL}	ALE		t_{XCYL} – 35 ns*2	—	ns	
ALE ↓ → CLK ↑ time	t_{LLCH}	ALE, CLK		t_{XCYL} – 35 ns*2	—	ns	

*1: For information on t_{inst}, see “(4) Instruction Cycle.”

*2: These characteristics are also applicable to the bus read timing.

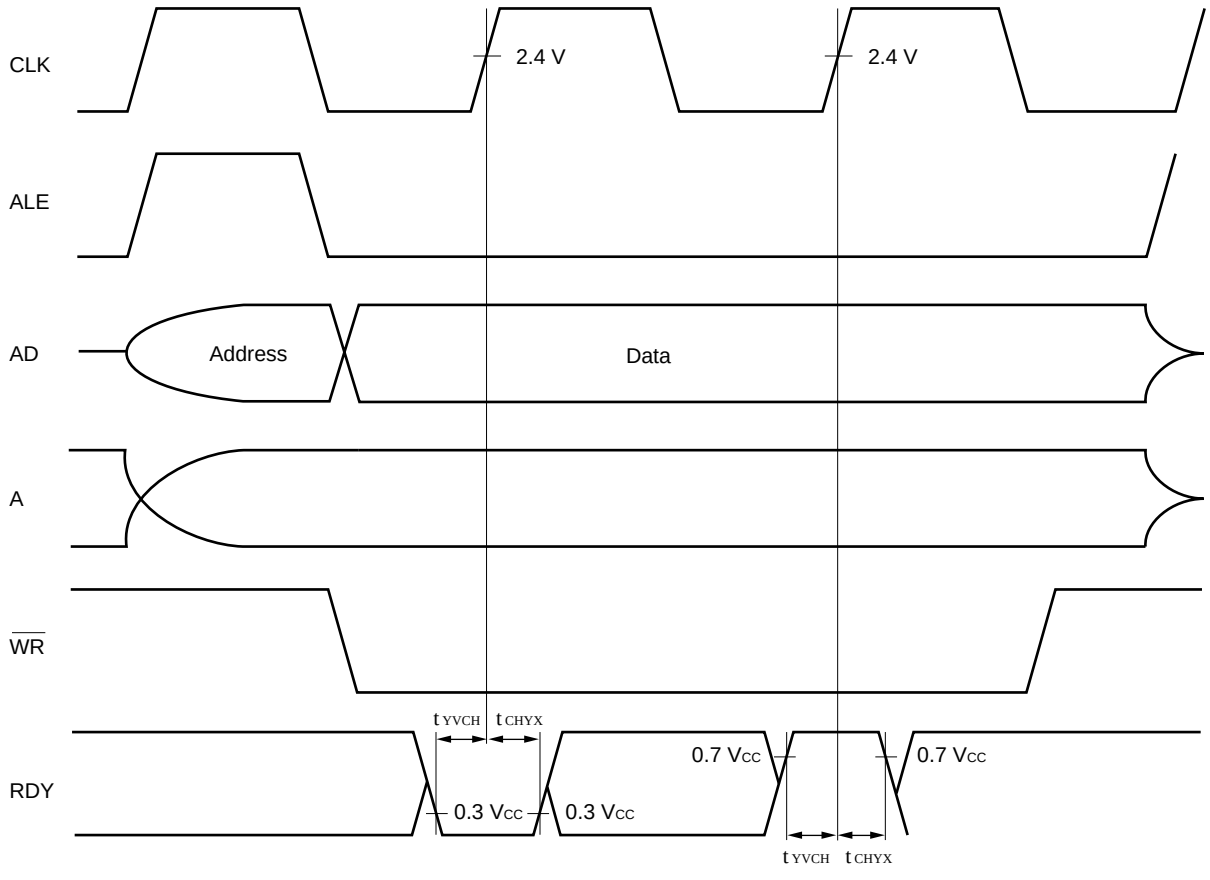


(8) Ready Input Timing

(V_{CC} = +5.0 V±10%, F_C = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY valid → CLK ↑ time	t_{YVCH}	RDY, CLK	Load condition: 50 pF	60	—	ns	*
CLK ↑ → RDY invalid time	t_{CHYX}			0	—	ns	*

* : These characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

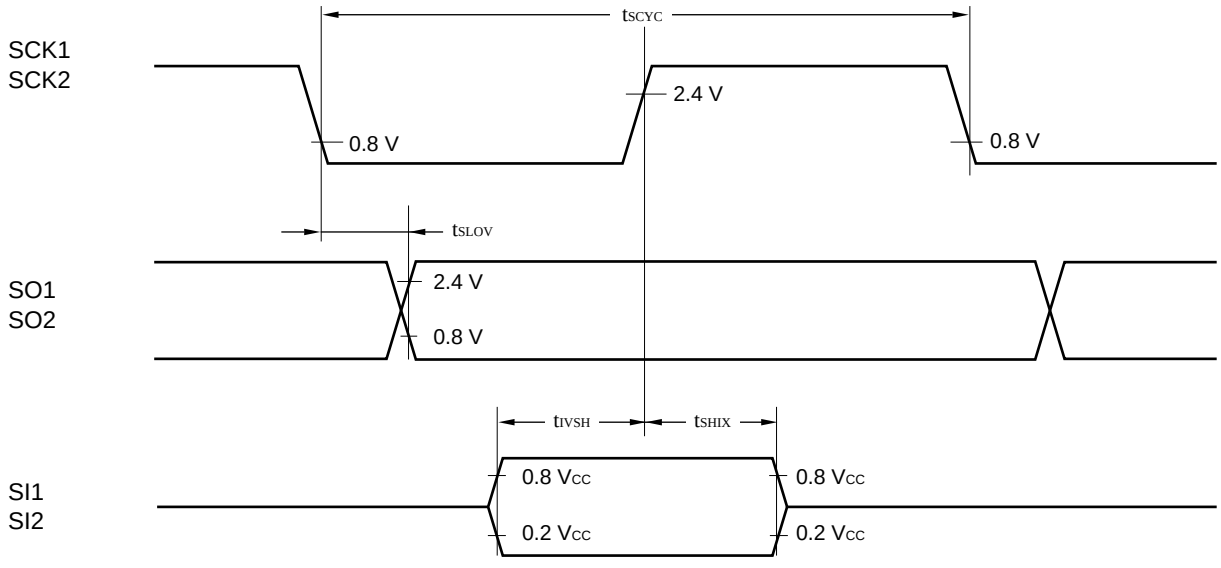
(9) UART and Serial I/O Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

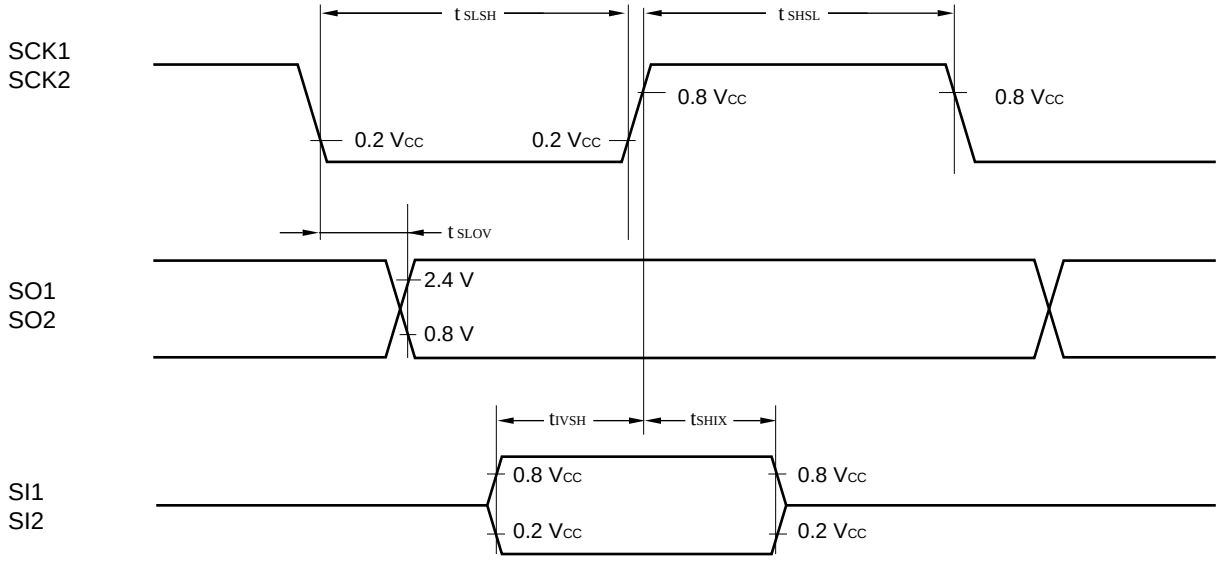
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK1,SCK2	Internal shift clock mode Load condition: 50 pF	2 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		–200	200	ns	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK1, SCK2	External shift clock mode Load condition: 50 pF	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}			1 t_{inst}*	—	µs	
SCK1 ↓ → SO1 time SCK2 ↓ → SO2 time	t_{SLOV}	SCK1, SO1 SCK2, SO2		0	200	ns	
Valid SI1 → SCK1 ↑ Valid SI2 → SCK2 ↑	t_{IVSH}	SI1, SCK1 SI2, SCK2		1/2 t_{inst}*	—	µs	
SCK1 ↑ → valid SI1 hold time SCK2 ↑ → valid SI2 hold time	t_{SHIX}	SCK1, SI1 SCK2, SI2		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**

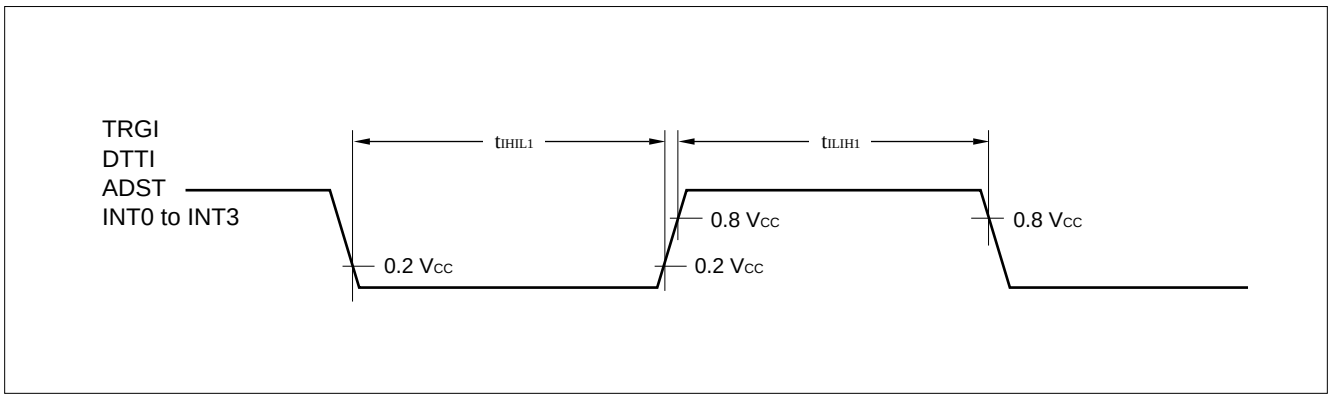


(10) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	TRGI, DTTI, ADST, INT0 to INT3	Load condition: 50 pF	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}			2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

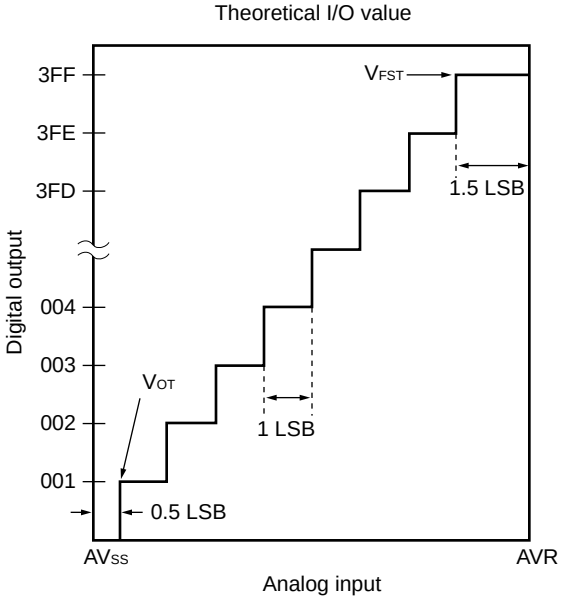
(AV_{CC} = V_{CC} = +3.5 V to +6.0 V, F_C = 10 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

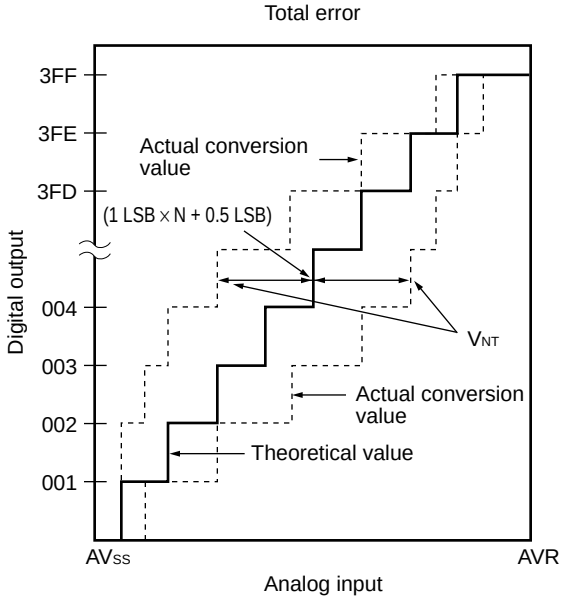
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—		AV_{CC} = V_{CC}	—	—	10	bit	
Linearity error				—	—	±2.0	LSB	
Differential linearity error				—	—	±1.5	LSB	
Total error				—	—	±3.0	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7		AV_{SS} – 1.5	AV_{SS} + 0.5	AV_{SS} + 2.5	LSB	
Full-scale transition voltage	V_{FST}			AVR – 3.5	AVR – 1.5	AVR + 0.5	LSB	
Interchannel disparity	—	—		—	—	4	LSB	
A/D mode conversion time			—	—	33 t_{inst}*	—	µs	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	—	10	µA	
Analog input voltage	—		—	0	—	AVR	V	
Reference voltage		AVR	—	0	—	AV_{CC}	V	
Reference voltage supply current	I_R		AVR = 5.0 V	—	200	—	µA	

* : For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔´“11 1111 1110”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error
  The total error indicates the difference between the actual value and theoretical value. This error is caused by the zero transition error, full-scale transition error, linearity error, quantization, and noise.





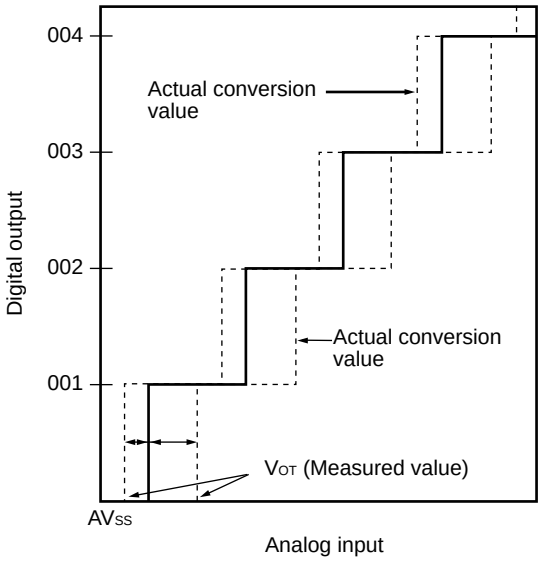
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{(V)}$$

$$\text{Total error of digital output “N”} = \frac{V_{NT} - (1\ \text{LSB} \times N + 0.5\ \text{LSB})}{1\ \text{LSB}}$$

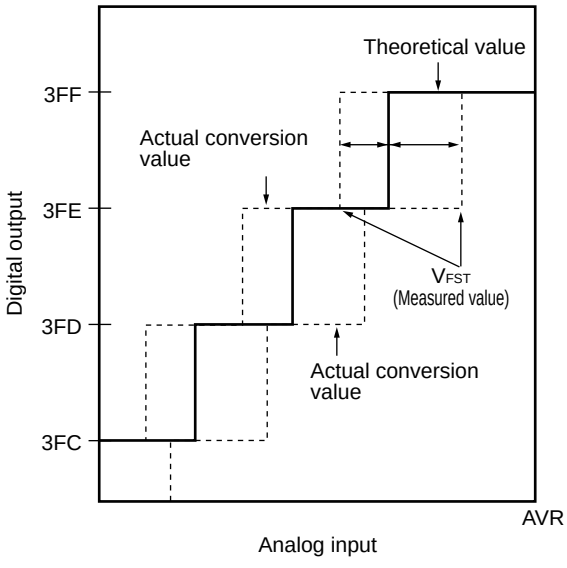
(Continued)

(Continued)

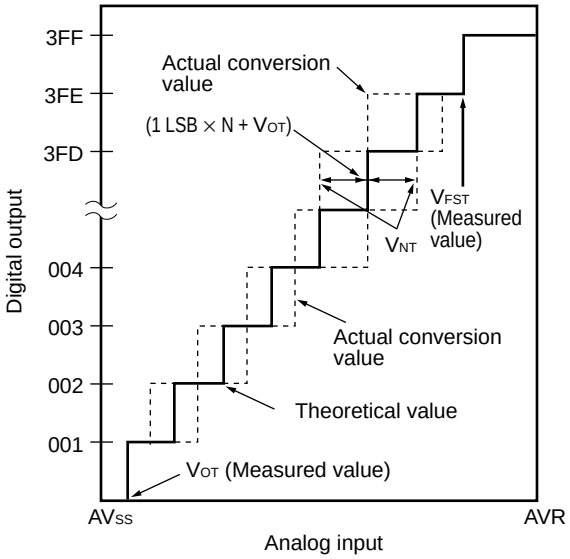
Zero transition error



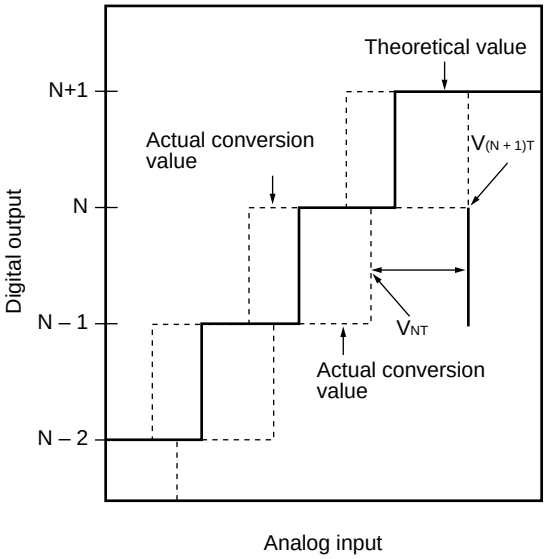
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output “N”} = \frac{V_{NT} - (1\ \text{LSB} \times N + V_{OT})}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output “N”} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

7. Notes on Using A/D Converter

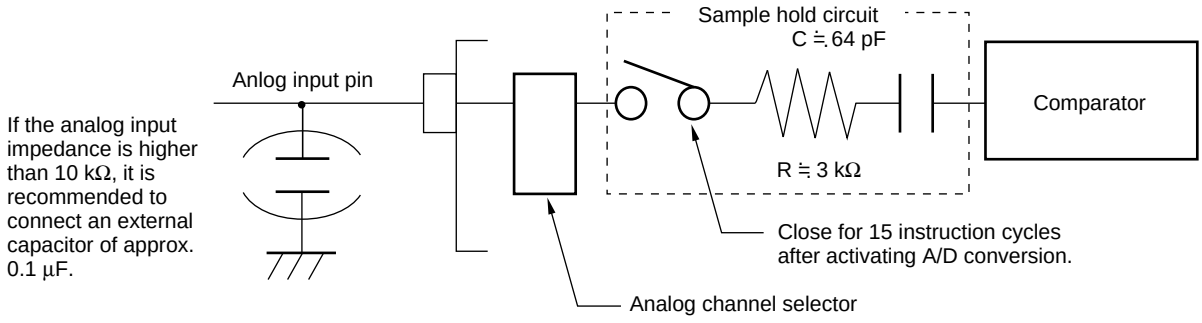
- **Input impedance of the analog input pins**

  The A/D converter used for the MB89860/850 series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for fifteen instruction cycles after activation A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

  Note that if the impedance connot be kept low, it is recommended to connect an external capacitor of about 0.1 µF for the analog input pin.

- **Analog Input Equivalent Circuit**

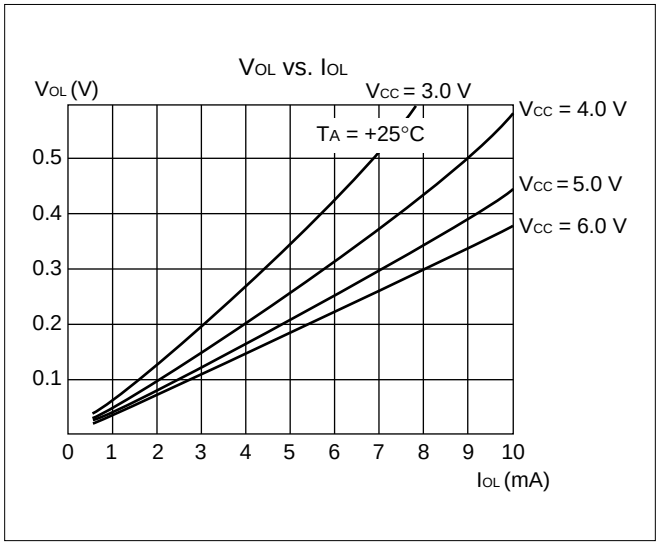


- **Error**

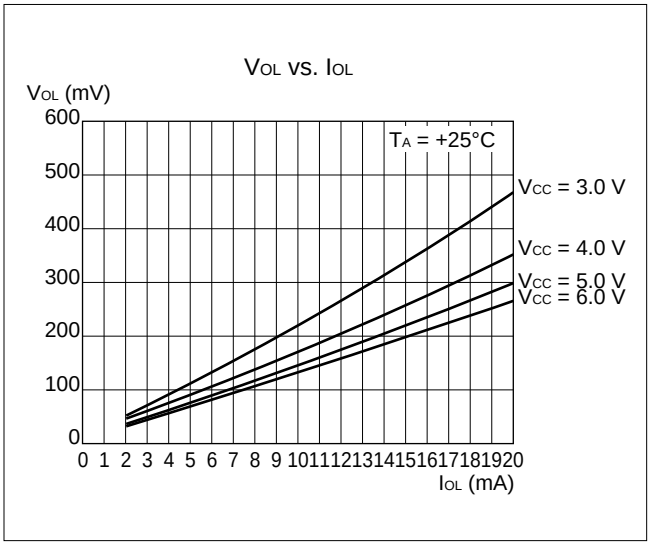
  The smaller the | AVR – AV_{SS} |, the greater the error would become relatively.

■ EXAMPLE CHARACTERISTICS

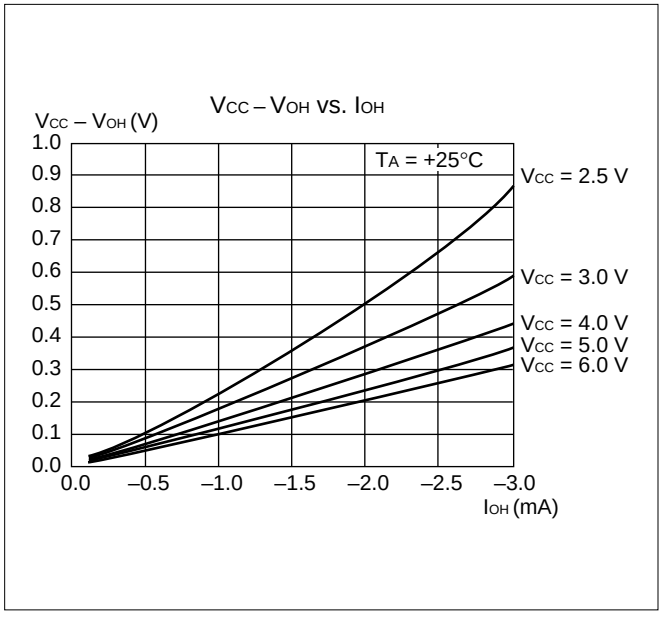
(1) "L" Level Output Voltage (P00 to P07, P10 to P17, P20 to P27, P30 to P37, and P50 to P57)



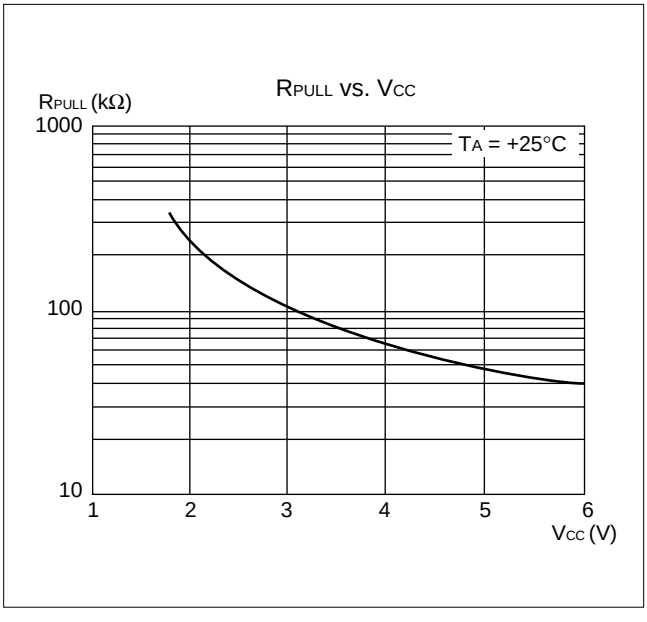
(2) "L" Level Output Voltage (P40 to P47)



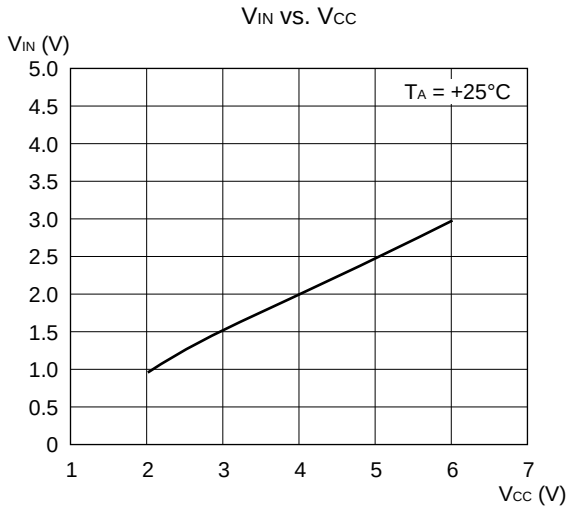
(3) "H" Level Output Voltage (P00 to P07, P10 to P17, P20 to P27, P30 to P37, and P40 to P47)



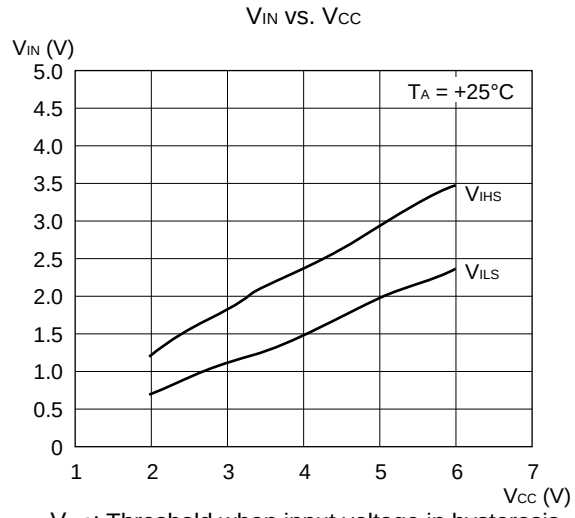
(4) Pull-up Resistance



(5) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



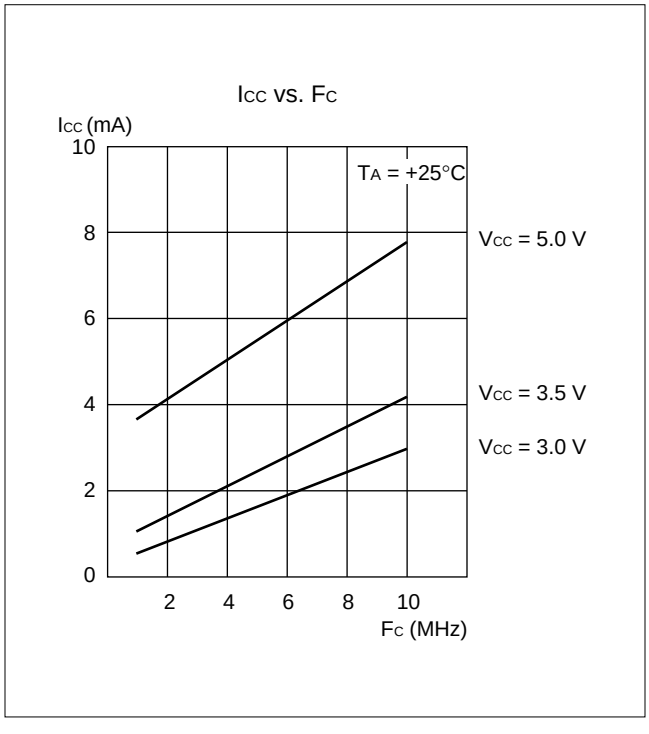
(6) "H" Level Input Voltage/"L" level Input Voltage (Hysteresis Input)



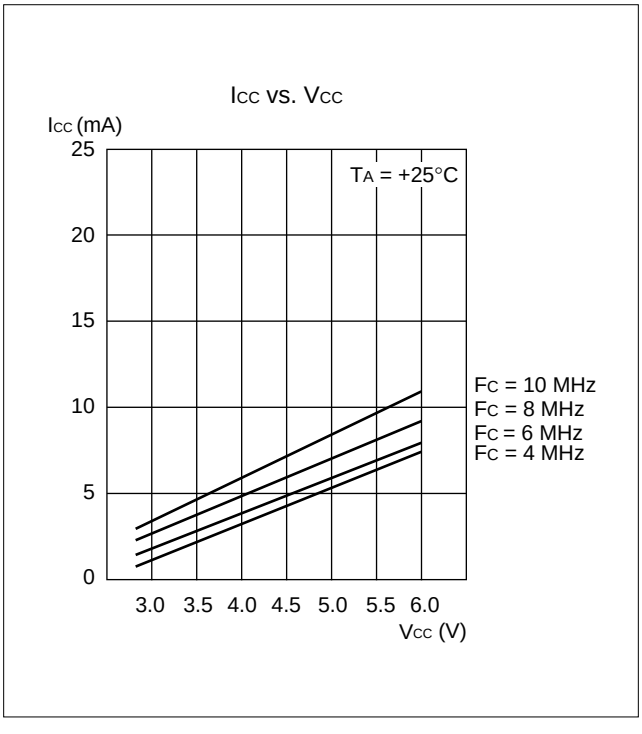
V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to "H" level

V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to "L" level

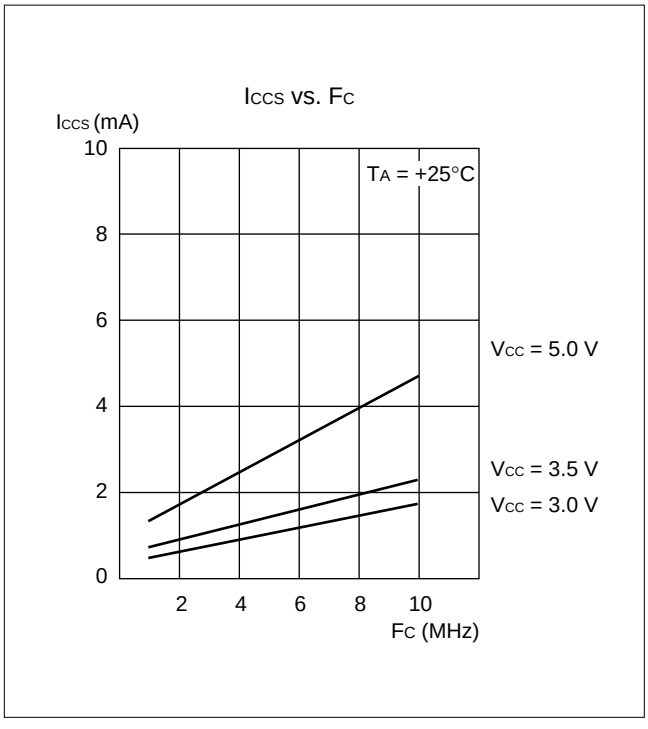
(7) Operating Supply Current vs. Frequency



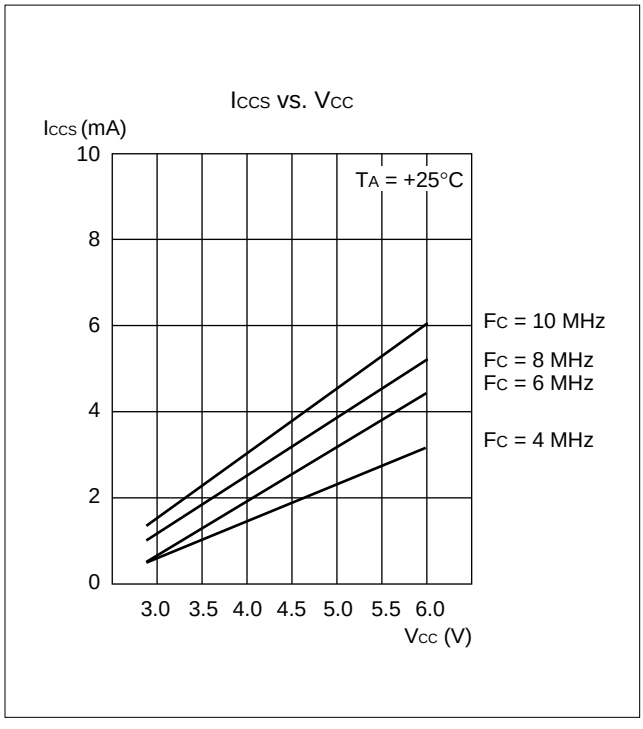
(8) Operating Supply Current vs. V_{CC}



(9) Sleep Power Supply Current vs. Frequency



(10) Sleep Power Supply Current vs. V_{CC}



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

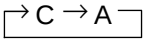
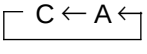
OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes:
- During byte transfer to A, T ← A is restricted to low bytes.
- Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 toDF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1		–	–	–	+ + – +	03
ROLC A	2	1		–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) +off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS (MB89855R)

Option type	Option selection	Remarks
Power-on reset	0: Without power-on reset 1: With power-on reset	—
Initial value of oscillation stabilization delay time	0: $2^{18}/F_C$ (s) (Crystal oscillator) 1: $2^{14}/F_C$ (s) (Ceramic oscillator)	Selects the initial value of the OSCS bit in the STBC register during power-on reset.
Reset pin output	0: Without reset output 1: With reset output	—
Pull-up resistor at port pin P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P60 to P64	1: Without pull-up resistor 0: With pull-up resistor	• Can be set per pin. • P00 to P07, P10 to P17, and P20 to P27 with a pull-up resistor can be set only for single-chip mode.

■ STANDARD OPTION LIST

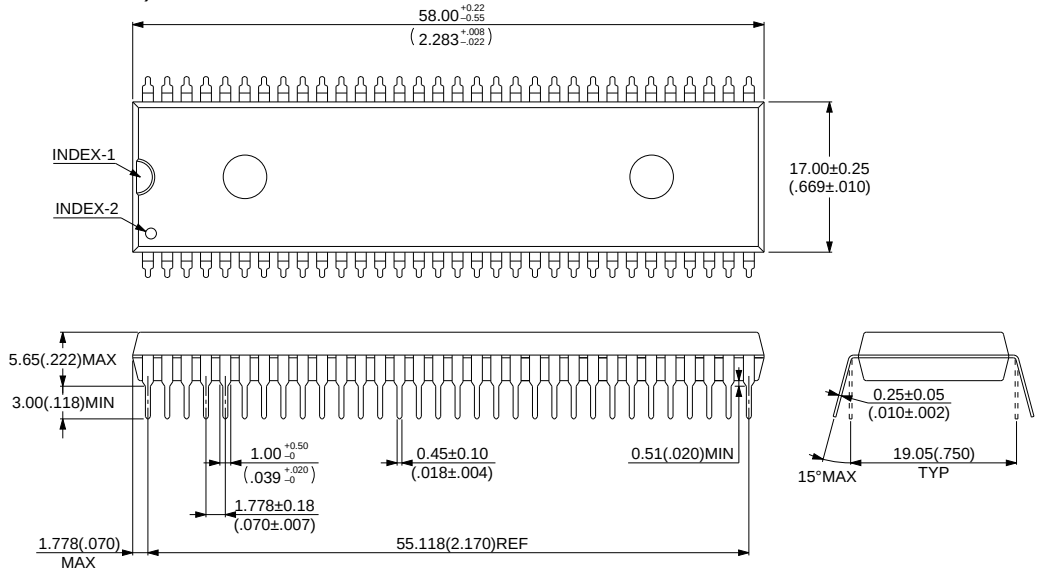
Parameter \ Part number	MB89P857/W857
Power-on reset	Available
Initial value of oscillation stabilization delay time	$2^{18}/F_C$ (s)
Output at reset pin	Available
Pull-up resistor at port pin	Not available

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89855RP-SH MB89P857P-SH	64-pin Plastic SH-DIP (DIP-64P-M01)	
MB89W857C-SH	64-pin Ceramic SH-DIP (DIP-64C-A06)	ES level only
MB89W857CF-ES-BND	64-pin Ceramic QFP (FPT-64C-A02)	ES level only

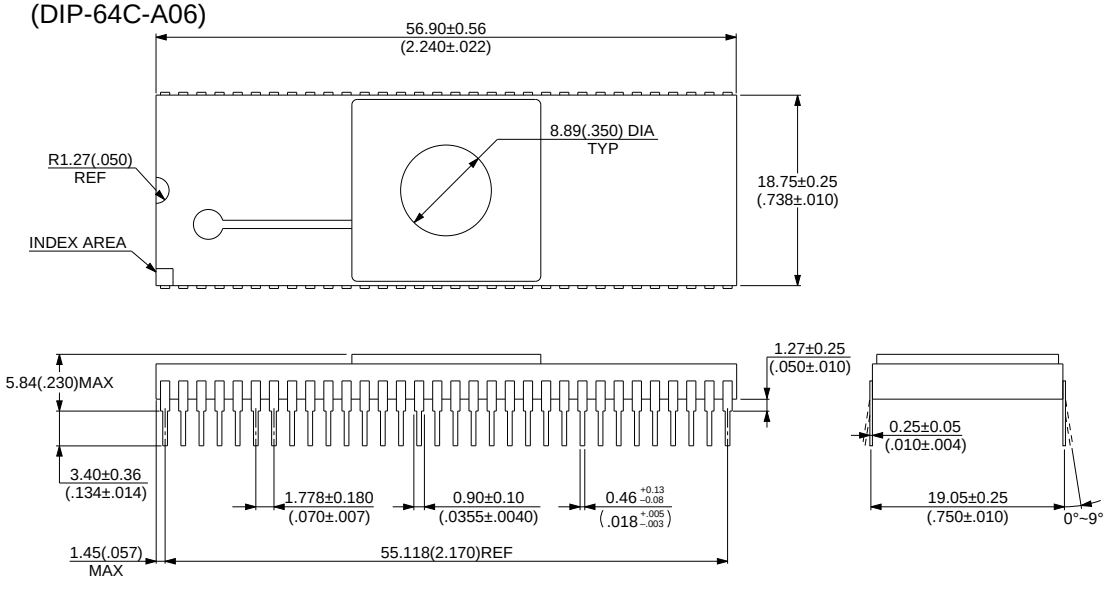
■ PACKAGE DIMENSIONS

64-pin Plastic SH-DIP
(DIP-64P-M01)



Dimensions in mm (inches)

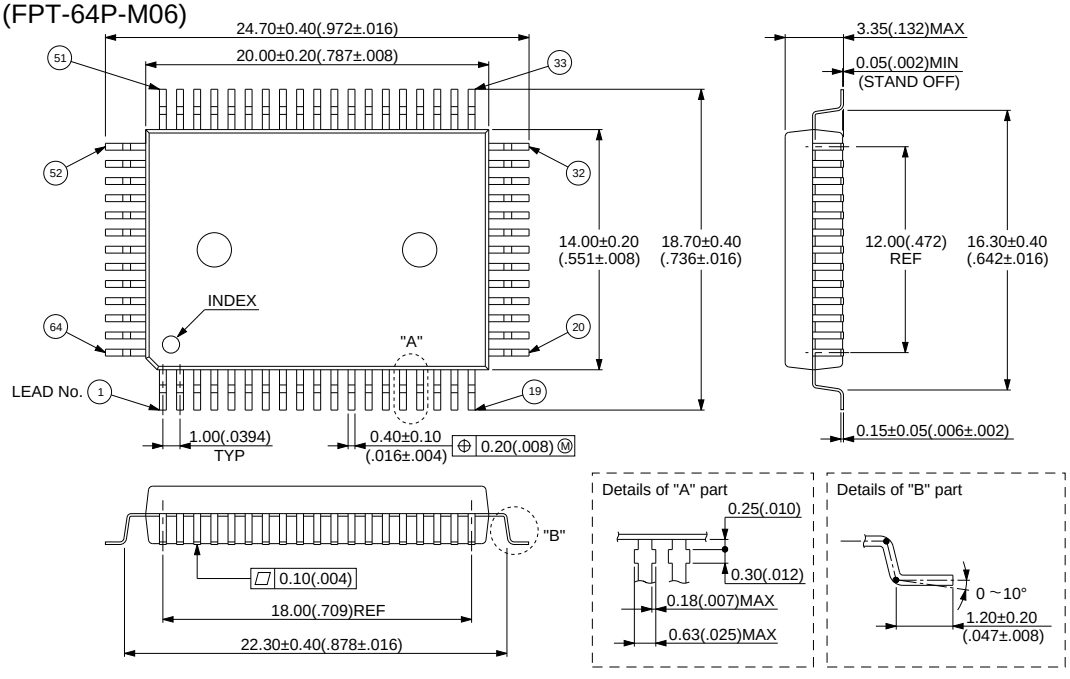
64-pin Ceramic SH-DIP
(DIP-64C-A06)



Dimensions in mm (inches)

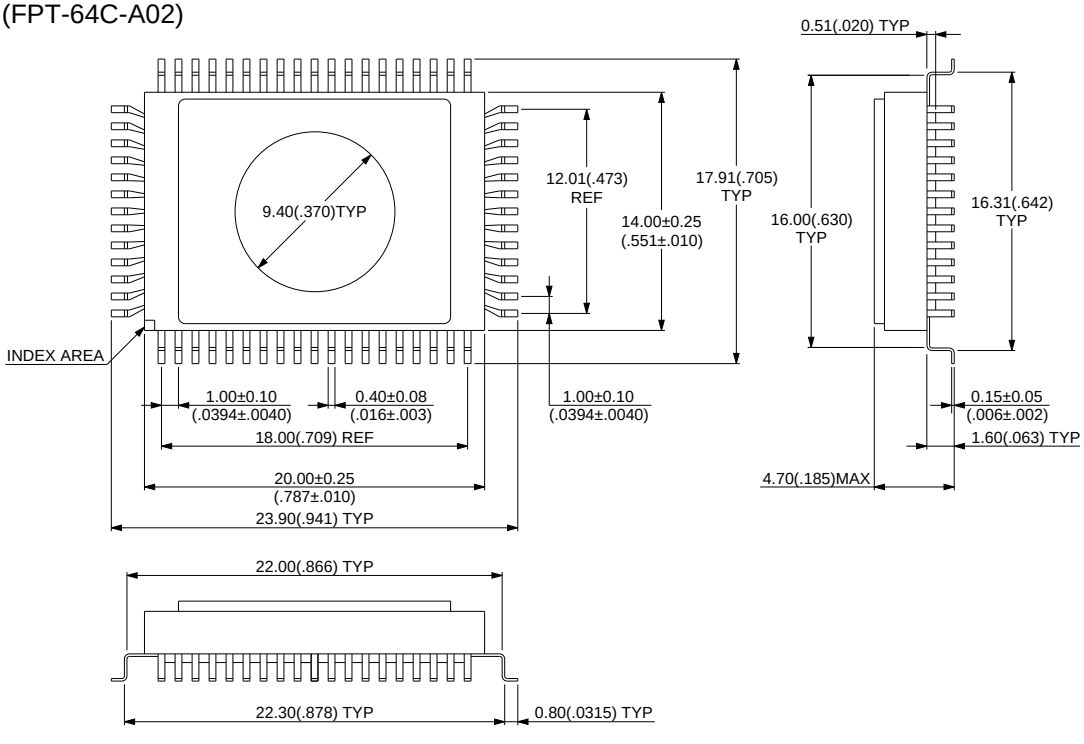
MB89850R Series

64-pin Plastic QFP
(FPT-64P-M06)



Dimensions in mm (inches)

64-pin Ceramic QFP
(FPT-64C-A02)



Dimensions in mm (inches)

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