CMOS 8-Bit Microcontroller

TMP86CP24F

The TMP86CP24 is the high-speed, high-performance and low power consumption 8-bit microcomputer, including ROM, RAM, LCD driver, multi-function timer/counter, serial interface (UART, HSIO), a 10-bit AD converter and two clock generators on chip.

| Product No. | ROM | RAM | Package | EEPROM MCU | Emulation Chip |
|-------------|---------------|--------------|---------------------|------------|----------------|
| TMP86CP24F | 48 K × 8 bits | 2 K × 8 bits | P-LQFP80-1212-0.50A | TMP86FP24F | TMP86C948XB |

Feautures

- ♦ 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (at 16 MHz)
 122 μs (at 32.768 kHz)
- ♦ 132 types and 731 basic instructions
- 19 interrupt sources (External: 5, Internal: 14)
- Input/output ports (54 pins)
 (Out of which 16 pins are also used as SEG pins)



- Timer, Event counter, Pulse width measurement, External trigger timer, Window, PPG output modes
- ♦ 8-bit timer counter: 2 ch
 - Timer, Event counter, PWM output, Programmable divider output, Capture modes
- Time base timer
- ♦ Divider output function
- Watchdog timer
 - Interrupt source/internal reset generate (programmable)



TMP86CP24

- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general
 can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer,
 when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid
 situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to
 property.

property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..

Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc.

The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.

The products described in this document are subject to the foreign exchange and foreign trade laws.

- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

86CP24-1 2003-04-15

P-LQFP80-1212-0.50A

- Serial interface
 - UART: 1ch (The function port for UART is also used as SIO function.)
 - SIO: 2ch
- ROM corrective function
 - Four register bank
 - 1 or 2 bytes replace mode
 - Address replace mode
- ♦ 10-bit successive approximation type AD converter
 - Analog input: 8 ch
- ♦ Five key-on wake-up pins
- ♦ LCD driver/controller
 - Built-in voltage booster for LCD driver
 - With display memory (12 bytes)
 - LCD direct drive capability (max 24 seg × 4 com)
 - 1/4, 1/3, 1/2duties or static drive are programmably selectable
- Dual clock operation
 - Single/dual-clock mode
- ♦ Nine power saving operating modes
 - STOP mode: Oscillation stops. Battery/capacitor back-up.

Port output hold/High-impedance.

- SLOW 1, 2 mode: Low power consumption operation using low-frequency clock (32.768 kHz)
- ullet IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of

Time-Base-Timer. Release by falling edge of TBTCR<TBTCK> setting.

IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock.

Release by interruputs.

• IDLE 2 mode: CPU stops, and peripherals operate using high and low frequency clock.

Release by interruputs.

• SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of

Time-Base-Timer. Release by falling edge of TBTCR<TBTCK> setting.

• SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock.

Release by interrupts.

• SLEEP 2 mode: CPU stops, and peripherals operate using high and low frequency clock.

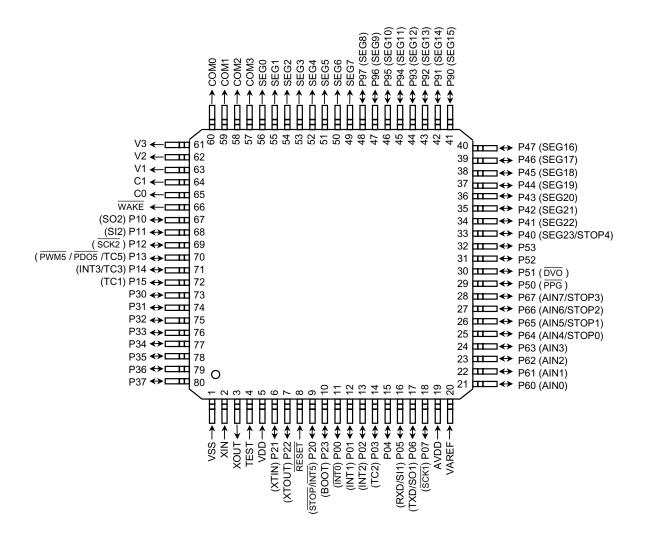
Release by interrupts.

♦ Wide operating voltage: 1.8 to 3.6V at 8 MHz/32.768 kHz

2.7 to 3.6V at 16 MHz/32.768 kHz

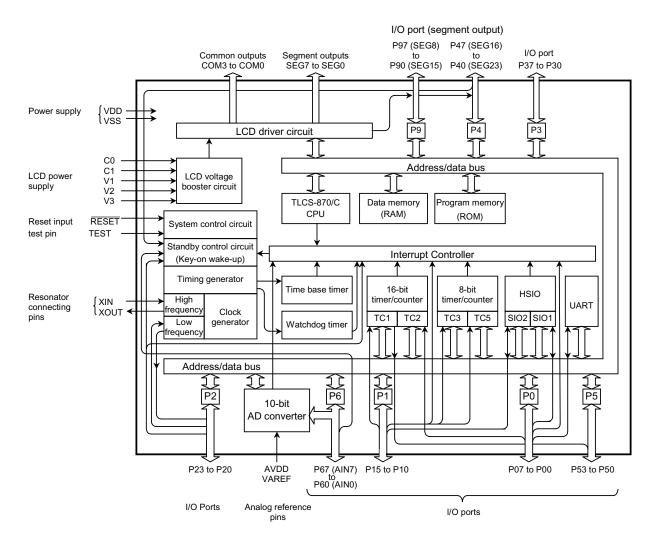
Pin Assignments (Top View)

P-LQFP80-1212-0.50A



Note: BOOT function of P23 is included in only TMP86FP24F.

Block Diagram



Pin Functions

| Pin Name | Input/Output | Fu | inctions |
|-------------------------------|--------------|--|--|
| P07 (SCK1) | I/O (I/O) | 8-bit input/output port with latch. | Serial clock input/output 1 |
| P06 (TXD, SO1) | I/O (Output) | When used as a serial interface output | UART data output, Serial data output 1 |
| P05 (RXD, SI1) | I/O (Input) | or UART output, respective output latch (P0DR) should be set to "1". | UART data input, Serial data input 1 |
| P04 | I/O | When used as an input port, an serial | |
| P03 (TC2) | I/O (Input) | interface input, UART input, timer | Timer counter 2 input |
| P02 (INT2) | I/O (Input) | counter input or an external interrupt | External interrupt 2 input |
| P01 (INT1) | I/O (Input) | input, respective output control (P0OUTCR) should be cleared to "0" | External interrupt 1 input |
| P00 (INTO) | I/O (Input) | after setting P0DR to "1". | External interrupt 0 input |
| P15 (TC1) | I/O (Input) | 6-bit input/output port with latch. | Timer counter 1 input |
| | | When used as a timer/counter output or | Timer counter 3 input, |
| P14 (TC3,INT3) | I/O (Input) | serial interface output, respective output latch (P1DR) should be set to "1". When | External interrupt 3 input |
| P13 | | used as an input port, a timer counter | PWM5 output, PDO5 output, |
| (PWM5 , PDO5 , TC5) | I/O (I/O) | input, an external interrupt input or serial | Timer/counter 5 input |
| P12 (SCK2) | I/O (I/O) | interface input, respective output control | Serial clock input/output 2 |
| P11 (SI2) | I/O (Input) | (P1OUTCR) should be cleared to "0" after setting P1DR to "1". | Serial data input 2 |
| P10 (SO2) | I/O (Output) | and setting i ibit to i . | Serial data output 2 |
| P23 | I/O | 4-bit input/output port with latch. | · |
| P22 (XTOUT) | I/O (Output) | When used as an input port or an | Resonator connecting pins (32.768 kHz) |
| P22 (X1001) | i/O (Output) | external interrupt input, respective | For inputting external clock, XTIN is used and |
| P21 (XTIN) | I/O (Input) | output control (P2OUTCR) should be cleared to "0" after setting output latch | XTOUT is opened. |
| D00 (NTE 070E) | 1/0 // 1) | (P2DR) to "1". | External interrupt input 5 or STOP mode |
| P20 (INT5, STOP) | I/O (Input) | , | release signal input |
| P37 to P30 | I/O | 8-bit input/output port with latch (Nch high current output). When used as an input port, respective output control (P3OUTCR) should be cleared to "0" after setting output latch (P3DR) to "1". | |
| P47 (SEG16) to P41 (SEG22) | I/O (Output) | 7-bit input/output port with latch. When used as an input port, respective output latch (P4DR) should be set to "1" after LCD output control (P4LCR) is cleared to "0". | LCD segment output |
| P40 (SEG23, STOP4) | I/O (I/O) | 1-bit input/output port with latch. When used as an input port, the output latch (P4DR) should be set to "1" after the LCD output control (P4LCR) is cleared to "0". When used as a LCD output, the P4LCR should be set to "1" after the STOPCR <stop4en> should be cleared to "0". When used as a key on wake up input, the STOPCR<stop4en> should be set to "1".</stop4en></stop4en> | LCD segment output STOP mode release input |
| P53 | | 4-bit input/output port with latch. When | |
| P52 | I/O | used as an input port, respective output | |
| P51 (DVO) | I/O (Output) | control (P5OUTCR) should be cleared to "0" after setting output latch (P5DR) to | Divider output |
| P50 (PPG) | I/O (Output) | "1". When used as a PPG output or divider output, respective P5DR should be set to "1". | PPG output |

| P67 (AIN7, STOP3) | I/O (Input) | 8-bit programmable input/output port (tri-state). Each bit of this port can be | STOP 3 input | | | | | |
|-------------------|--------------|--|----------------------------|---------------|--|--|--|--|
| P66 (AIN6, STOP2) | I/O (Input) | individually configured as an input or an | STOP 2 input |] | | | | |
| P65 (AIN5, STOP1) | I/O (Input) | output under software control. When | STOP 1 input |] | | | | |
| P64 (AIN4, STOP0) | I/O (Input) | used as an input port, respective input/output control (P6CR1) should be | STOP 0 input |] | | | | |
| P63 (AIN3) | I/O (Input) | cleared to "0" after setting input control | | AD converter | | | | |
| P62 (AIN2) | I/O (Input) | (P6CR2) to "1". When used as an analog input or key on wake up input, | | analog inputs | | | | |
| P61 (AIN1) | I/O (Input) | respective P6CR1 should be cleared to | | | | | | |
| P60 (AIN0) | I/O (Input) | "0" after clearing P6CR2 to "0". When used as a key on wake up input, STOPCR <stopien> should be set to "1". (i = 0 to 3)</stopien> | | | | | | |
| SEG7 to SEG0 | Output | LCD segment outputs | | | | | | |
| COM3 to COM0 | Output | LCD common outputs | | | | | | |
| V3 to V1 | LCD voltage | LCD voltage booster pin. | | | | | | |
| C1 to C0 | booster pin | Capacitors are required between C0 and | C1 pin and V1/V2/V3 pin an | d GND. | | | | |
| WAKE | Output | STOP mode monitor output. During re SLEEP0/1/2, warming-up period), it becomes the high impedance state. | • | | | | | |
| XIN, XOUT | Input output | Resonator connecting pins for high-frequ For inputting external clock, XIN is used | • | | | | | |
| RESET | Input | Reset signal input | | | | | | |
| TEST | Input | Test pin for out-going test. Be fixed to lov | V. | | | | | |
| VDD, VSS | | Power supply for operation | | | | | | |
| VAREF | Power supply | Analog reference voltage for AD conversion | | | | | | |
| AVDD | | AD circuit power supply | | | | | | |

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86CP24 memory consists of 4 blocks: ROM, RAM, DBR (Data Buffer Register) and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1.1.1 shows the TMP86CP24 memory address map. The general-purpose registers are not assigned to the RAM address space.

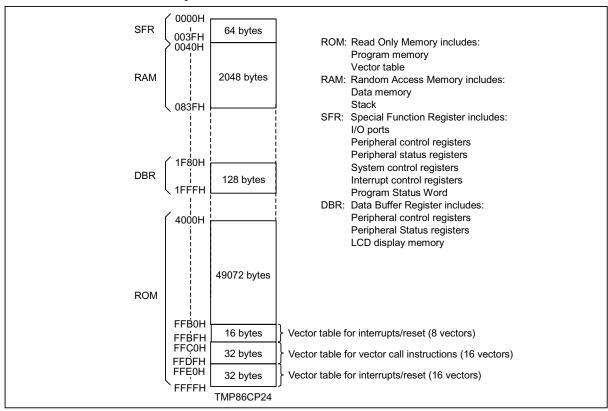


Figure 1.1.1 Memory Address Maps

1.2 Program Memory (ROM)

The TMP86CP24 has a 48 K \times 8 bits (address 4000H to FFFFH) of program memory (mask programmed ROM).

Electrical Characteristics

Absolute Maximum Ratings $| (V_{SS} = 0 V) |$

| Parameter | Symbol | Pins | Rating | Unit |
|---------------------------------|--------------------|------------------------------------|--------------------------|------|
| Supply voltage | V_{DD} | | -0.3 to 4.0 | |
| Input voltage | V _{IN} | | -0.3 to $V_{DD} + 0.3$ | V |
| Output voltage | V _{OUT1} | Except V3 pin | -0.3 to $V_{DD} + 0.3$ | v |
| Output voltage | V _{OUT2} | V3 pin | -0.3 to 4.0 | |
| | I _{OUT1} | P0, P1, P20, P23, P3, P5, P6 Ports | -2 | |
| Output current (Per 1 pin) | I _{OUT2} | P0, P1, P2, P4, P6, P9, WAKE Ports | 2 | |
| | I _{OUT3} | P3, P5 Ports | 10 | |
| | Σl _{OUT1} | P0, P1, P20, P23, P3, P5, P6 Ports | -80 | mA |
| Output current (Total) | Σl _{OUT2} | P0, P1, P2, P4, P6, P9, WAKE Ports | 80 | |
| | Σl _{OUT3} | P3, P5 Ports | 30 | |
| Power dissipation [Topr = 85°C] | PD | | 350 | mW |
| Soldering temperature (time) | Tsld | | 260 (10 s) | |
| Storage temperature | Tstg | | -55 to 125 | °C |
| Operating temperature | Topr | | -40 to 85 | |

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = -40 to 85°C)

| Parameter | Symbol | Pins | C | Condition | Min | Max | Unit |
|----------------------------------|------------------|-------------------------|--|-------------------------------------|----------------------|---|--------|
| | | | fc = 16 MHz | NORMAL1, 2 mode IDLE0, 1, 2 mode | 2.7 | | |
| Cumply voltage | \/ | | fc = 8 MHz | NORMAL1, 2 mode | 1.8 | 2.0 | |
| Supply voltage | V _{DD} | | fs = | IDLE0, 1, 2 mode SLOW1, 2 mode | | 3.6 | |
| | | | 32.768 kHz | SLEEP0, 1, 2 mode | 1.8 | | |
| | | | | STOP mode $V_{DD} \times 0.70$ | | | |
| | V _{IH1} | Except Hysteresis input | V > 2.7.V | | $V_{DD} \times 0.70$ | | |
| Input high level | V _{IH2} | Hysteresis input | V _{DD} ≥ 2.7 V | | $V_{DD} \times 0.75$ | V_{DD} | |
| | V _{IH3} | | V _{DD} < 2.7 V | | $V_{DD} \times 0.80$ | | |
| | V _{IL1} | Except Hysteresis input | V _{DD} ≥ 2.7 V | | | $V_{DD} \times 0.30$ | |
| Input low level | V_{IL2} | Hysteresis input | | | 0 | $V_{DD} \times 0.25$ | |
| | V _{IL3} | | V_{DD} < 2.7 V | | | 2.7 1.8 3.6 1.8 × 0.70 × 0.75 × 0.80 VDD × 0.30 VDD × 0.25 VDD × 0.20 8.0 16.0 0.0 34.0 0.8 1.2 1.6 2.4 | |
| | fc | XIN, XOUT | V _{DD} = 1.8 to 3.6 V | | 1.0 | 8.0 | MHz |
| Clock frequency | 10 | AIN, AOUT | $V_{DD} = 2.7 \text{ to}$ | 3.6 V | 1.0 | 3.6 VDD VDD × 0.30 VDD × 0.25 VDD × 0.20 8.0 16.0 34.0 1.2 2.4 | IVIITZ |
| | fs | XTIN, XTOUT | $V_{DD} = 1.8 \text{ to}$ | 3.6 V | 30.0 | 34.0 | kHz |
| LCD reference | V1 | | Booster circuit is enable | | 0.8 | 1.2 | V |
| voltage | V2 | | (V3 ≥ V _{DD}) | | 1.6 | 2.4 | V |
| Capacity for LCD booster circuit | C _{LCD} | | LCD booster (V3 ≥ V _{DD}) | circuit is enable | 0.1 | 0.47 | μF |

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics $(V_{SS} = 0 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Pins | Conditi | ion | Min | Тур. | Max | Unit |
|-------------------------------------|---------------------|---------------------------------------|---|----------------------|-----|----------|--------|-------|
| Hysteresis voltage | V _{HS} | Hysteresis input | $V_{DD} = 3.3 \text{ V}$ | | - | 0.4 | _ | V |
| | I _{IN1} | TEST | $V_{DD} = 3.6 \text{ V}, V_{IN} = 0 \text{ V}$ | | - | _ | -5 | |
| Input current | I _{IN2} | Sink Open Drain, Tri-state | $V_{DD} = 3.6 \text{ V}, \text{ V}_{IN}$ | = 3.6 V/0 V | - | _ | ±5 | μА |
| | I _{IN4} | RESET | $V_{DD}=3.6\;V,\;V_{IN}$ | = 3.6 V | _ | _ | +5 | |
| | R _{IN1} | TEST Pull-down | $V_{DD}=3.6\ V,\ V_{IN}$ | = 3.6 V | - | 70 | - | |
| Input resistance | R _{IN2} | RESET Pull-Up P21,P22 Ports | $V_{DD} = 3.6 \text{ V}, V_{IN}$ | = 0 V | 100 | 220 | 450 | kΩ |
| | R _{IN3} | Programmable Pull-down (P4, P9 Ports) | | | - | T.B.D. | - | |
| High frequency feedback resister | R _{FB} | хоит | V _{DD} = 3.6 V | | - | 1.2 | - | MO |
| Low frequency feedback resister | R _{FBT} | хтоит | V _{DD} = 3.6 V | | - | 14 | - | ΜΩ |
| Output leakage current | I _{LO} | Sink Open Drain, Tri-state | $V_{DD} = 3.6 \text{ V}$ $V_{OUT} = 3.4 \text{V} / 0.2$ | 2 V | _ | - | ±10 | μА |
| Output high voltage | V _{OH} | C-MOS, Tri-state | $V_{DD} = 3.6 \text{ V}, I_{OH}$ | | 3.2 | - | - | |
| Output low voltage | V _{OL} | Except XOUT,P3 and P5 Ports | V _{DD} = 3.6 V, I _{OL} | = 0.9 mA | - | - | 0.4 | V |
| Output low current | l _{OL} | P3, P5 Ports | $V_{DD} = 3.6 \text{ V}, V_{OL}$ $V3 \ge V_{DD}$ | = 1.0 V | - | 6 | 1 | mA |
| LCD output voltage | V _{2-3OUT} | V2 pin | V2 pin V3 ≥ V _{DD} Reference supply pin: V1 | | - | V1 × 2 | _ | |
| LCD output voltage (LCD booster is | | V3 pin | SEG/COM pin: No-l | | _ | V1×3 | _ | V |
| enable) | V _{1-30UT} | V1 pin | V3 ≥ V _{DD} Reference supply pin: V2 | | - | V2 × 1/2 | - | _ v |
| oriabio) | V1-3001 | V3 pin | | SEG/COM pin: No-load | | V2 × 3/2 | _ | |
| | | | V _{DD} = 3.6 V | <vfsel> = 00</vfsel> | _ | T.B.D. | _ | |
| | | | fc = 16 MHz CLCD = 0.1 μF | <vfsel> = 01</vfsel> | _ | T.B.D. | - | |
| LCD output current | | | Reference supply pin: | <vfsel> = 10</vfsel> | _ | T.B.D. | _ | |
| capacity | I _{LCDV3} | V3 pin | V1 = 1 V | <vfsel> = 11</vfsel> | _ | T.B.D. | - | mV/μA |
| (LCD booster is | LODVO | | V _{DD} = 3.6 V | <vfsel> = 00</vfsel> | _ | T.B.D. | _ | 1 |
| enable) | | | fc = 16 MHz CLCD= 0.1 μF | <vfsel> = 01</vfsel> | | T.B.D. | _ | |
| | | | Reference supply pin: | <vfsel> = 10</vfsel> | | T.B.D. | _ | |
| | | | V2 = 2V | <vfsel> = 11</vfsel> | _ | T.B.D. | _ | |
| Supply current in NORMAL 1, 2 mode | | | $V_{DD} = 3.6 \text{ V}$ $V_{IN} = 3.4 \text{ V}/0.2 \text{ V}$ | | - | T.B.D. | T.B.D. | |
| Supply current in IDLE 0, 1, 2 mode | | | fc = 16 MHz fs = 32.768 kHz | | - | T.B.D. | T.B.D. | mA |
| Supply current in SLOW 1 mode | | | V 20V | | - | T.B.D. | T.B.D. | |
| Supply current in SLEEP 1 mode | I _{DD} | | $V_{DD} = 3.6 \text{ V}$ $V_{IN} = 3.4 \text{ V}/0.2 \text{ V}$ fs = 32.768 kHz | | - | T.B.D. | T.B.D. | ^ |
| Supply current in SLEEP 0 mode | | | 13 – 32.700 KHZ | fs = 32.768 kHz | | T.B.D. | T.B.D. | μА |
| Supply current in STOP mode | | | V _{DD} = 3.6 V V _{IN} = 3.4 V/0.2 V | | - | T.B.D. | T.B.D. | |

- Note 1: Typical values show those at Topr = 25° C, $V_{DD} = 3.3 \text{ V}$
- Note 2: Input current (I_{IN1}, I_{IN2}); The current through pull-up or pull-down resistor is not included.
- Note 3: I_{DD} does not include I_{REF} current.
- Note 4: The supply currents of SLOW 2 and SLEEP 2 modes are equivalent to IDLE 0, 1, 2.
- Note 5: Current capacity indicates the drop in pin V3 output voltage per 1μA. Select an appropriate booster frequency setting in LCDCR<VFSEL> according to LCD panel. To maintain stable operation, the current capacity for the reference pin must be more than ten times that of the output current capacity.

AD Conversion Characteristics

 $(V_{SS} = 0.0 \text{ V}, 2.7 \text{ V} \le V_{DD} \le 3.6 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|--|------------------|---|------------------------|----------|-------------------|------|
| Analog reference voltage | VAREF | | A _{VDD} – 1.0 | - | A _{VDD} | |
| Power supply voltage of analog control circuit | A _{VDD} | | | V_{DD} | | V |
| Analog reference voltage range (Note 4) | ΔVAREF | | 2.5 | - | - | V |
| Analog input voltage | V_{AIN} | | V _{SS} | - | V _{AREF} | |
| Power supply current of analog reference voltage | I _{REF} | $V_{DD} = A_{VDD} = V_{AREF} = 3.6 \text{ V}$ $V_{SS} = 0.0 \text{ V}$ | - | T.B.D. | T.B.D. | mA |
| Non linearity error | | V== - A. (== - 2.7.V | _ | - | ±2 | |
| Zero point error | | $V_{DD} = A_{VDD} = 2.7 \text{ V}$ | _ | _ | ±2 | LSB |
| Full scale error | | V _{SS} = 0.0 V | _ | _ | ±2 | LOB |
| Total error | | V _{AREF} = 2.7 V | _ | _ | ±2 | |

(V_{SS} = 0.0 V, 2.0 V \leq V_{DD} < 2.7 V, Topr = -40 to 85°C)

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|--|--------------------|--|------------------------|----------|-------------------|------|
| Analog reference voltage | V _{AREF} | | A _{VDD} – 0.6 | - | A _{VDD} | |
| Power supply voltage of analog control circuit | A _{VDD} | | | V_{DD} | | V |
| Analog reference voltage range (Note 4) | ΔV _{AREF} | | 2.0 | - | - | V |
| Analog input voltage | V_{AIN} | | V _{SS} | - | V _{AREF} | |
| Power supply current of analog reference voltage | I _{REF} | $V_{DD} = A_{VDD} = V_{AREF} = 2.0V$ $V_{SS} = 0.0 \text{ V}$ | - | T.B.D. | T.B.D. | mA |
| Non linearity error | | V _{DD} = A _{VDD} = 2.0 V | _ | - | ±4 | |
| Zero point error | | 35 135 | _ | - | ±4 | LSB |
| Full scale error | | V _{SS} = 0.0 V | _ | _ | ±4 | LOD |
| Total error | | V _{AREF} = 2.0 V | _ | - | ±4 | |

 $(V_{SS} = 0.0 \text{ V}, 1.8 \text{ V} \le V_{DD} < 2.0 \text{ V}, \text{Topr} = -10 \text{ to } 85^{\circ}\text{C}) \text{ (Note 5)}$

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|--|-------------------|--|------------------------|----------|-------------------|------|
| Analog reference voltage | V _{AREF} | | A _{VDD} – 0.1 | ı | A _{VDD} | |
| Power supply voltage of analog control circuit | A _{VDD} | | | V_{DD} | | V |
| Analog reference voltage range (Note 4) | ΔV_{AREF} | | 1.8 | - | _ | V |
| Analog input voltage | V _{AIN} | | V _{SS} | ı | V _{AREF} | |
| Power supply current of analog reference voltage | I _{REF} | $V_{DD} = A_{VDD} = V_{AREF} = 1.8V$ $V_{SS} = 0.0 \text{ V}$ | - | T.B.D. | T.B.D. | mA |
| Non linearity error | | V _{DD} = A _{VDD} = 1.8 V | _ | _ | ±4 | |
| Zero point error | | 155 | _ | ı | ±4 | LSB |
| Full scale error | | V _{SS} = 0.0 V | _ | ı | ±4 | LOD |
| Total error | | V _{AREF} = 1.8 V | _ | _ | ±4 | |

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.12.2 Register configuration".
- Note 3: Please use input voltage to AIN input Pin in limit of V_{AREF} V_{SS}.

 When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: Analog Reference Voltage Range: $\Delta V_{AREF} = V_{AREF} V_{SS}$
- Note 5: When AD is used with V_{DD} < 2.0 V, the guaranteed temperature range varies with the operating voltage.
- Note 6: When AD converter is not used, fix the AVDD pin on the VDD level.

AC Characteristics

 $(V_{SS} = 0 \text{ V}, V_{DD} = 2.7 \text{ to } 3.6 \text{ V}, \text{Topr} = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|------------------------------|--------|------------------------------------|-------|-------|-------|------|
| | | NORMAL1, 2 mode | | _ | 4 | |
| Machine cycle time | tcy | IDLE1, 2 mode | | | · | ue |
| Machine Cycle time | icy | SLOW1, 2 mode | 117.6 | | 133.3 | μ\$ |
| | | SLEEP1, 2 mode | 117.0 | | | |
| High level clock pulse width | twcH | For external clock operation (XIN | | | | |
| Low level clock pulse width | twcL | input) | - | 31.25 | - | ns |
| Low level clock pulse width | IWCL | fc = 16 MHz | | | | |
| High level clock pulse width | twcH | For external clock operation (XTIN | | | | |
| Low level clock pulse width | twcL | input) fs = 32.768 kHz | - | 15.26 | - | μS |

 $(V_{SS} = 0 \text{ V}, V_{DD} = 1.8 \text{ to } 3.6 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

| Parameter | Symbol | Condition | Min | Тур. | Max | Unit |
|---|--------------|---|-------|-------|-------|------|
| | | NORMAL1, 2 mode IDLE1, 2 mode | 0.5 | - | 4 | |
| Machine cycle time | tcy | SLOW1, 2 mode SLEEP1, 2 mode | 117.6 | - | 133.3 | μ\$ |
| High level clock pulse width Low level clock pulse width | twcH twcL | For external clock operation (XIN input) fc = 8 MHz | - | 62.5 | - | ns |
| High level clock pulse width Low level clock pulse width | twcH twcL | For external clock operation (XTIN input) fs = 32.768 kHz | - | 15.26 | - | μѕ |

Recommended Oscillating Conditions

- Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following http://www.murata.co.jp/search/index.html