TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT   SILICON MONOLITHIC

T6L02

SOURCE DRIVER FOR TFT LCD PANELS

The T6L02 is a 64 gray-level, 300 / 309-channel-output source driver for TFT LCD panels. To meet the need for large-sized LCD panels, it allows a maximum operating frequency of 55MHz. The device accepts 6-bit digital data inputs which, combined with the internal D/A converter and 11 external power supplies, allows display of up to 260,000 color tones.

Based on high-speed CMOS, the T6L02 offers both low power consumption and high-speed operation.

Combined with the T6C58 gate driver, the T6L02 allows configuration of an SVGA-or XGA-compatible, high-performance TFT LCD module.

Unit: mm

T6L02	USER AREA PITCH	
	IN	OUT
(SAN, 6FS)	0.48	0.075
(SCN, 6FS)	0.48	0.075

Please contact Toshiba or a distributor for the latest TCP specification and product line-up.

TCP (Tape Carrier Package)

FEATURES

- Grayscale data : 18-bit digital (3 outputs × 6 bits) parallel transfer method, selectable write direction

- Panel drive outputs : 300 / 309 outputs, 64 gray levels, DAC system, 11 reference analog voltage inputs

- Fast operation : Max 55MHz

- Power supply voltage : Digital power supply voltage ...... 3.0 to AV_{DD}
  Analog power supply voltage ..... 4.5 to 5.5V

- Operating temperature : − 20 to 75°C

- Package : Tape carrier package (TCP)

- Cascading multiple devices

BLOCK DIAGRAM

PIN ASSIGNMENT

D1	42			
D2	43			
D3	44	41	AV$_{SS}$	
D4	45	40	AV$_{DD}$	
D5	46	39	V9	
D6	47	38	V7	
D7	48	37	V5	
D8	49	36	V3	
D9	50	35	V1	
D10	51	34	DF1	
		33	DE1	
		32	DD1	
		31	DC1	
		30	DB1	
		29	DA1	
		28	DF2	
		27	DE2	
		26	DD2	
		25	DC2	
		24	DB2	
		23	DA2	
		22	DI / O	
		21	DV$_{SS}$	
		20	MODE	
		19	CPH	
		18	DV$_{DD}$	
		17	DO / I	
		16	LOAD	
		15	DF3	
		14	DE3	
		13	DD3	
		12	DC3	
		11	DB3	
		10	DA3	
		9	U / D	
		8	V0	
D300	341	7	V2	
D301	342	6	V4	
D302	343	5	V6	
D303	344	4	V8	
D304	345	3	V10	
D305	346	2	AV$_{DD}$	
D306	347	1	AV$_{SS}$	
D307	348			
D308	349			
D309	350			

T 6 L 0 2

(TOP VIEW)

The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or a distributor for the latest TCP specification.

PIN FUNCTION

PIN NAME	I / O	FUNCTION
DI / O DO / I	I / O	Data transfer enable pin These pins, become active at the high signal, initiated the transferred data into the sampling register of the device. One is configured as an input and the other is configured as an output of which directions are determined by U / D as shown below. | U / D	DI / O	DO / I
H	Input	Output
L	Output	Input | When set for input A high on DI / O or DO / I is latched into the internal logic synchronously with the rising edge of CPH. When the internal circuit is in standby state, the device is ready to transfer data. The grayscale data is latched in sequentially, starting at the next rise of CPH. When set for output The pin is used to transfer the enable signal to the T6L02 at the next stage of the LCD driver. The pin enters standby state after outputting a high.
U / D	Input	Transfer direction select pin This pin controls the direction in which the data is transferred into the sampling register. Data is transferred synchronously with each rising edge of CPH in one of the following sequences: When U / D is high, data is transferred in the order D1 to D3, D4 to D6, D7 to D9 ····· When U / D is low, the direction is reversed to give D307 to D309, D304 to D306, D301 to D303 ····· The voltage applied to this pin must be a DC-level voltage that is either high or low.
CPH	Input	Sampling clock input This clock input is used to transfer grayscale data.
DA1 to 3 DB1 to 3 DC1 to 3 DD1 to 3 DE1 to 3 DF1 to 3	Input	Grayscale data bus The data inputs consist of 6-bit word for each three channel that are transferred in parallel at the rising edge of CPH. The relationship between the grayscale data and the weight of each bit is as follows: Grayscale data $= 32 \times DFn + 16 \times DEn + 8 \times DDn + 4 \times DCn + 2 \times DBn + DAn$ where $n = 1$ to 3 The relationship between the grayscale data and the output pins is as follows: DA1, DB1, DC1, DD1, DE1, DF1 ····· D (3m-2) DA2, DB2, DC2, DD2, DE2, DF2 ····· D (3m-1) DA3, DB3, DC3, DD3, DE3, DF3 ····· D (3m) where $m = 1$ to 103

PIN NAME	I / O	FUNCTION

MODE	Input	Output select pin
		This signal selects either 300-pin mode or 309-pin mode for the LCD panel driver.
		    When MODE = high, 300-output-pin mode is selected, in which case D151 through D159 are not used. (voltages appearing at D151 through D159 are indeterminate).
		    When MODE = low, 309-output-pin mode is selected.

LOAD	Input	Data load input pin
		    When a high voltage supplys to the load input, the data is transferred from the Sampling register to the Load register synchronously at the rising edge of CPH. All 300 or 309 LCD panel drive pin outputs are simultaneously updated.
		    The selected analog voltage corresponding to the data are send the LCD.

V0 to V10		Reference analog input pins
		    These pins are used to input the voltage used for the DAC.
		    Conditions: $AV_{SS} < V0 \leqq V1 \leqq V2 \leqq V3 \leqq V4 \leqq V5 \leqq V6 \leqq V7 \leqq V8 \leqq V9 \leqq V10 < AV_{DD}$ or $AV_{SS} < V10 \leqq V9 \leqq V8 \leqq V7 \leqq V6 \leqq V5 \leqq V4 \leqq V3 \leqq V2 \leqq V1 \leqq V0 < AV_{DD}$

D1 to D309	Output	LCD panel drive pins
AV_{DD}		Analog power supply pin
AV_{SS}		Analog GND pin This pin must be at the same potential level as the digital GND pin.
DV_{DD}		Digital power supply pin
DV_{SS}		Digital GND pin This pin must be at the same potential level as the analog GND pin.

DEVICE OPERATION

(1) Starting data transfer

A high input to the data transfer enable pin (DI / O or DO / I) is latched into the internal logic synchronously with the rising edge of CPH, setting the device ready to transfer data. Data transfer starts at the next rise of CPH (see Fig. 1-1 and 2-1).
This enable input must not be held high for more than one CPH period.

(2) Data transfer method

The data is latched in the grayscale data bus to the sampling register (REG1) synchronously with each rising edge of CPH.
Grayscale data for three outputs are latched into the device simultaneously in one transfer.
Therefore, the data is latched in 300-output mode by performing 100 transfer, and data is latched in 309-output mode by performing 103 transfer. When the data loading is completed, the device enters a standby state.

(3) Terminating data transfer

The data transfer enable pin (DO / I or DI / O) output goes high synchronously with the rising edge of CPH one clock period before the last data is latched in. It is held high until the next rise of CPH (see Fig. 1-1 and 2-1).
The output from this pin can be connected directly as input to the data transfer enable pin (DI / O or DO / I) of the next stage LCD driver. In this way, multiple devices can easily be cascaded to drive a large screen.

(4) Panel drive output

When a high voltage supplys to the load input, the data in the sampling register (REG1) is transferred to the load register (REG2) and device starts updating output to the LCD panel drive pins.
CPH may be held at the DC level for the duration from three CPH periods after a high input on LOAD is latched in until one clock period before CPH goes high after a high on the data transfer enable pin is latched in following a 1H period (see Fig. 1-2).

(5) Reference power supply circuit

The connection between the device and the external reference power supply for Reference analog supply is configured with 7 or 8 resistors of the same specification in series (total of 64 resistor ladders).
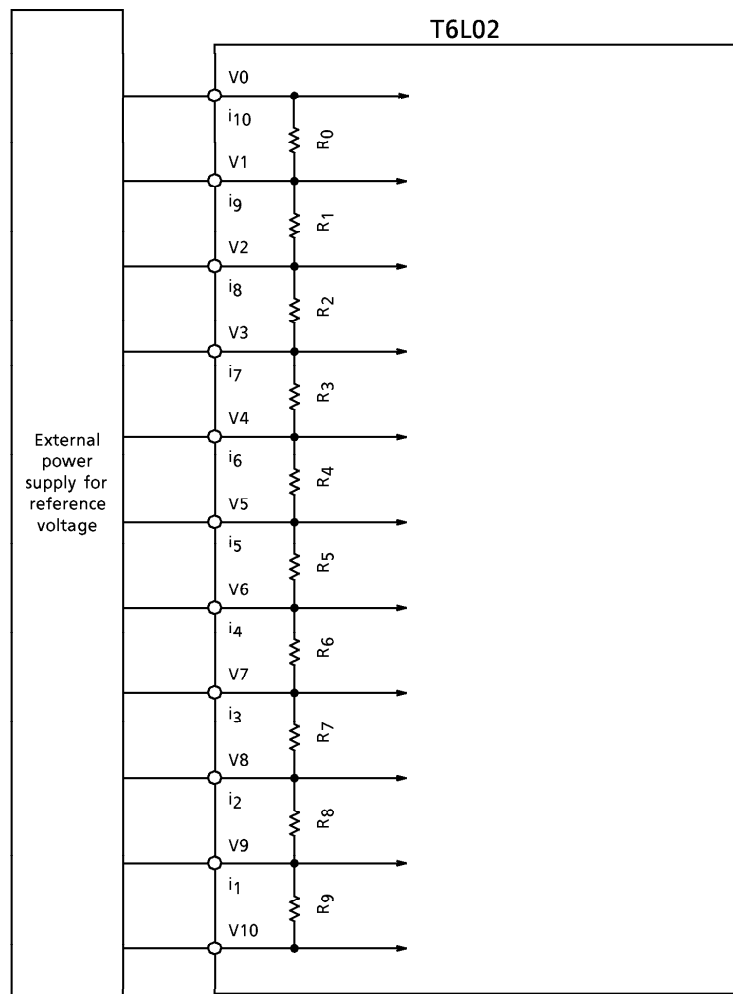
(6) Grayscale data and output voltages

The LCD drive output voltages are determined by the grayscale data values and the 11 reference analog inputs line voltages (V0 to V10).

The three high-order data bits select a pair of reference analog voltages. Calculation of the output voltage involves multiplying a value derived from the selected reference analog values by a factor determined by the values of the three low-order bits and dividing by either seven or eight.

DFn (MSB)	DEn	DDn	DCn	DBn	DAn (LSB)

Three high-order bits of data :
Selection of reference analog voltage

Three low-order bits of data :
D / A converted voltage

*n = 1, 2, 3
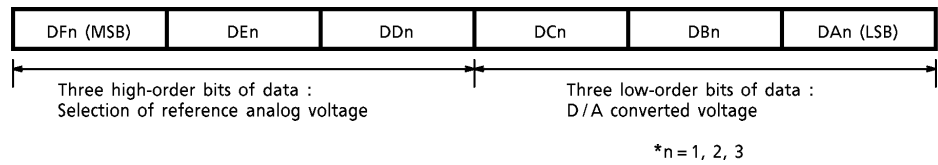
● Three high-order data bits

DFn	DEn	DDn	SELECTED REFERENCE VOLTAGES
0	0	0	V0 or V1 and V2
0	0	1	V2 and V3
0	1	0	V3 and V4
0	1	1	V4 and V5
1	0	0	V5 and V6
1	0	1	V6 and V7
1	1	0	V7 and V8
1	1	1	V8 and V9 or V10

● Three low-order data bits

$(DFn, DEn, DDn) = (0, 0, 0)$

V0
V1

V2
000 001 010 011 100 101 110 111
(DCn, DBn, DAn)

$(DFn, DEn, DDn) = (0, 0, 1)$ to $(1, 1, 0)$

Vd

Vd + 1
111 000 001 010 011 100 101 110 111
(DCn, DBn, DAn)
*d = 2 to 7

$(DFn, DEn, DDn) = (1, 1, 1)$

V8

V9
V10
111 000 001 010 011 101 100 110 111
(DCn, DBn, DAn)
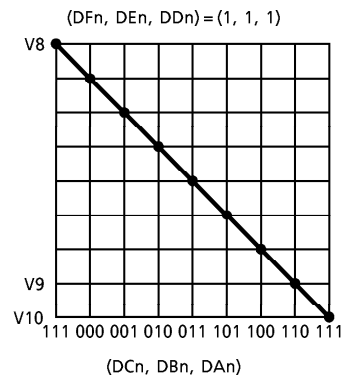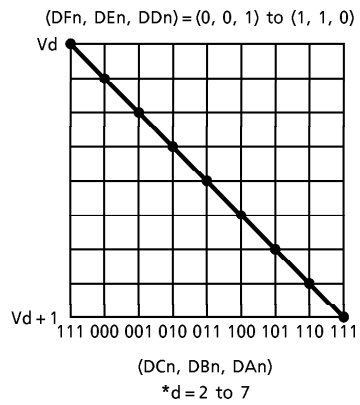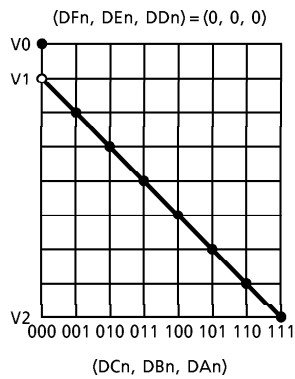
● Grayscale data and output voltages

(*) n = 1 to 3

GRAY-SCALE DATA	DFn	DEn	DDn	DCn	DBn	DAn	OUTPUT VOLTAGE	GRAY-SCALE DATA	DFn	DEn	DDn	DCn	DBn	DAn	OUTPUT VOLTAGE
00H	0	0	0	0	0	0	V_0	20H	1	0	0	0	0	0	$V_6 + (V_5 - V_6) \times 7/8$
01H	0	0	0	0	0	1	$V_2 + (V_1 - V_2) \times 6/7$	21H	1	0	0	0	0	1	$V_6 + (V_5 - V_6) \times 6/8$
02H	0	0	0	0	1	0	$V_2 + (V_1 - V_2) \times 5/7$	22H	1	0	0	0	1	0	$V_6 + (V_5 - V_6) \times 5/8$
03H	0	0	0	0	1	1	$V_2 + (V_1 - V_2) \times 4/7$	23H	1	0	0	0	1	1	$V_6 + (V_5 - V_6) \times 4/8$
04H	0	0	0	1	0	0	$V_2 + (V_1 - V_2) \times 3/7$	24H	1	0	0	1	0	0	$V_6 + (V_5 - V_6) \times 3/8$
05H	0	0	0	1	0	1	$V_2 + (V_1 - V_2) \times 2/7$	25H	1	0	0	1	0	1	$V_6 + (V_5 - V_6) \times 2/8$
06H	0	0	0	1	1	0	$V_2 + (V_1 - V_2) \times 1/7$	26H	1	0	0	1	1	0	$V_6 + (V_5 - V_6) \times 1/8$
07H	0	0	0	1	1	1	V_2	27H	1	0	0	1	1	1	V_6
08H	0	0	1	0	0	0	$V_3 + (V_2 - V_3) \times 7/8$	28H	1	0	1	0	0	0	$V_7 + (V_6 - V_7) \times 7/8$
09H	0	0	1	0	0	1	$V_3 + (V_2 - V_3) \times 6/8$	29H	1	0	1	0	0	1	$V_7 + (V_6 - V_7) \times 6/8$
0AH	0	0	1	0	1	0	$V_3 + (V_2 - V_3) \times 5/8$	2AH	1	0	1	0	1	0	$V_7 + (V_6 - V_7) \times 5/8$
0BH	0	0	1	0	1	1	$V_3 + (V_2 - V_3) \times 4/8$	2BH	1	0	1	0	1	1	$V_7 + (V_6 - V_7) \times 4/8$
0CH	0	0	1	1	0	0	$V_3 + (V_2 - V_3) \times 3/8$	2CH	1	0	1	1	0	0	$V_7 + (V_6 - V_7) \times 3/8$
0DH	0	0	1	1	0	1	$V_3 + (V_2 - V_3) \times 2/8$	2DH	1	0	1	1	0	1	$V_7 + (V_6 - V_7) \times 2/8$
0EH	0	0	1	1	1	0	$V_3 + (V_2 - V_3) \times 1/8$	2EH	1	0	1	1	1	0	$V_7 + (V_6 - V_7) \times 1/8$
0FH	0	0	1	1	1	1	V_3	2FH	1	0	1	1	1	1	V_7
10H	0	1	0	0	0	0	$V_4 + (V_3 - V_4) \times 7/8$	30H	1	1	0	0	0	0	$V_8 + (V_7 - V_8) \times 7/8$
11H	0	1	0	0	0	1	$V_4 + (V_3 - V_4) \times 6/8$	31H	1	1	0	0	0	1	$V_8 + (V_7 - V_8) \times 6/8$
12H	0	1	0	0	1	0	$V_4 + (V_3 - V_4) \times 5/8$	32H	1	1	0	0	1	0	$V_8 + (V_7 - V_8) \times 5/8$
13H	0	1	0	0	1	1	$V_4 + (V_3 - V_4) \times 4/8$	33H	1	1	0	0	1	1	$V_8 + (V_7 - V_8) \times 4/8$
14H	0	1	0	1	0	0	$V_4 + (V_3 - V_4) \times 3/8$	34H	1	1	0	1	0	0	$V_8 + (V_7 - V_8) \times 3/8$
15H	0	1	0	1	0	1	$V_4 + (V_3 - V_4) \times 2/8$	35H	1	1	0	1	0	1	$V_8 + (V_7 - V_8) \times 2/8$
16H	0	1	0	1	1	0	$V_4 + (V_3 - V_4) \times 1/8$	36H	1	1	0	1	1	0	$V_8 + (V_7 - V_8) \times 1/8$
17H	0	1	0	1	1	1	V_4	37H	1	1	0	1	1	1	V_8
18H	0	1	1	0	0	0	$V_5 + (V_4 - V_5) \times 7/8$	38H	1	1	1	0	0	0	$V_9 + (V_8 - V_9) \times 6/7$
19H	0	1	1	0	0	1	$V_5 + (V_4 - V_5) \times 6/8$	39H	1	1	1	0	0	1	$V_9 + (V_8 - V_9) \times 5/7$
1AH	0	1	1	0	1	0	$V_5 + (V_4 - V_5) \times 5/8$	3AH	1	1	1	0	1	0	$V_9 + (V_8 - V_9) \times 4/7$
1BH	0	1	1	0	1	1	$V_5 + (V_4 - V_5) \times 4/8$	3BH	1	1	1	0	1	1	$V_9 + (V_8 - V_9) \times 3/7$
1CH	0	1	1	1	0	0	$V_5 + (V_4 - V_5) \times 3/8$	3CH	1	1	1	1	0	0	$V_9 + (V_8 - V_9) \times 2/7$
1DH	0	1	1	1	0	1	$V_5 + (V_4 - V_5) \times 2/8$	3DH	1	1	1	1	0	1	$V_9 + (V_8 - V_9) \times 1/7$
1EH	0	1	1	1	1	0	$V_5 + (V_4 - V_5) \times 1/8$	3EH	1	1	1	1	1	0	V_9
1FH	0	1	1	1	1	1	V_5	3FH	1	1	1	1	1	1	V_{10}

Reference analog resistance rate ($R_0 = 2.31\text{k}\Omega$)

R_0	R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_8	R_9
1.00	2.00	2.77	1.50	0.90	0.84	0.66	0.84	1.42	1.05

TIMING DIAGRAMS

● In 300-output mode

(*) D1/D307 : U/D = high→D1
U/D = low→D307
(See pin description (U/D) on page 4.)
(Note) Except for D151 to D159.
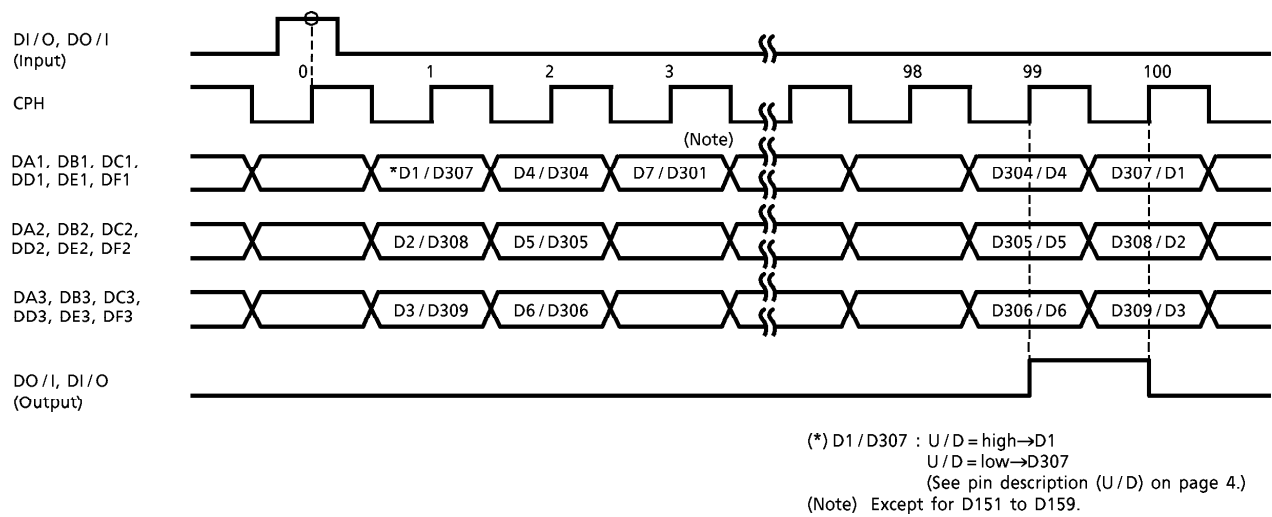
Fig. 1-1

Fig. 1-2

● In 309-output mode

(*) D1 / D307 : U / D = high→D1
U / D = low→D307
(See pin description (U / D) on page 4.)
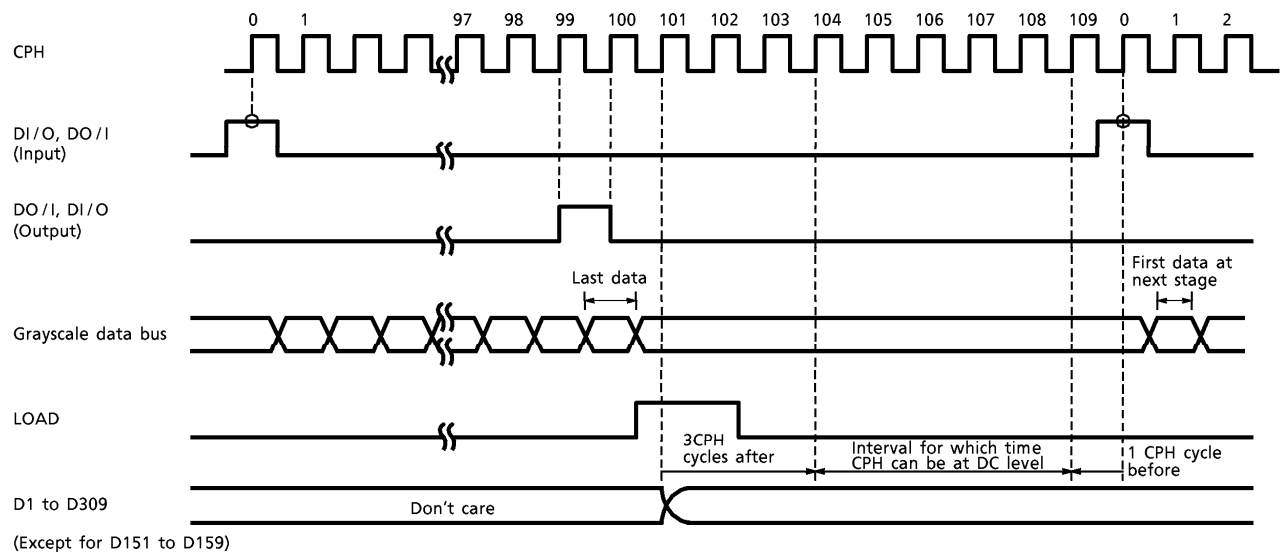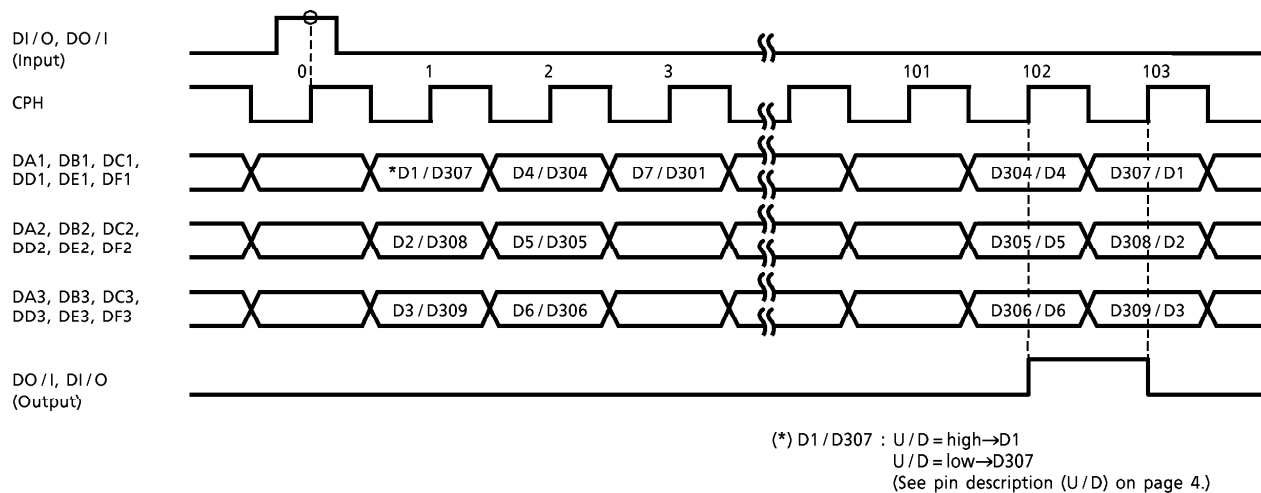
Fig. 2-1
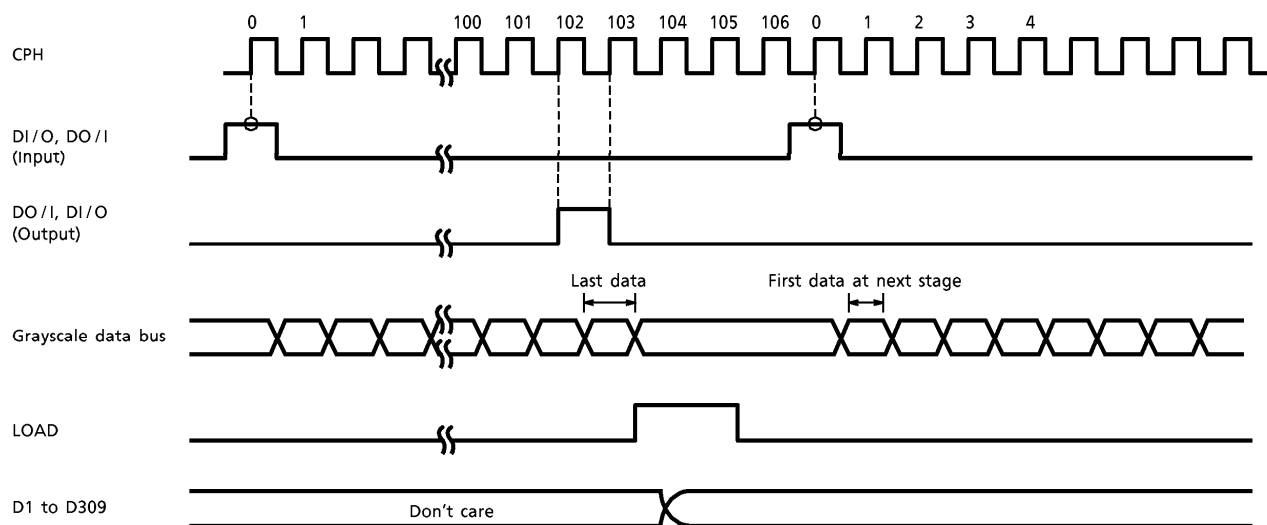
Fig. 2-2

ABSOLUTE MAXIMUM RATINGS ($AV_{SS} = DV_{SS} = 0V$)

PARAMETER	SYMBOL	RATING	UNIT	RELEVANT PIN
Analog Supply Voltage	AV_{DD}	-0.3 to 6.5	V	
Digital Supply Voltage	DV_{DD}	-0.3 to $AV_{DD} + 0.3$	V	
Input Voltage	V_{IN}	-0.3 to $DV_{DD} + 0.3$	V	
Reference Analog Voltage	$V (0:10)$	-0.3 to $AV_{DD} + 0.3$	V	V0 to V10
Storage Temperature	T_{stg}	-55 to 125	°C	

RECOMMENDED OPERATING CONDITIONS ($AV_{SS} = DV_{SS} = 0V$)

PARAMETER	SYMBOL	TEST CONDITION	RATING	UNIT	RELEVANT PIN
Analog Supply Voltage	AV_{DD}		4.5 to 5.5	V	
Digital Supply Voltage	DV_{DD}		3.0 to AV_{DD}	V	
Reference Analog Voltage-1 (Note)	V1 to V9		$AV_{SS} + 0.1$ to $AV_{DD} - 0.1$	V	
Reference Analog Voltage-2 (Note)	V0	Case 1	V1 to AV_{DD}	V	
	V0	Case 2	AV_{SS} to V1		
	V10	Case 1	AV_{SS} to V9		
	V10	Case 2	V9 to AV_{DD}		
Driver Unit Output Voltage	V_{OUT}		$AV_{SS} + 0.1$ to $AV_{DD} - 0.1$	V	D1 to D309
Operating Temperature	T_{OP}		-20 to 75	°C	
Operating Frequency	f_{CPH}		DC to 55	MHz	CPH
Output Load Capacitance	C_L		150 (max)	pF / pin	D1 to D309

(Note) The following shows the relative magnitude of each reference analog voltage:
- For case 1
  $AV_{SS} < V10$, $Vd \leqq Vd - 1$, $V0 < AV_{DD}$ (where $d = 9$ to 1)
- For case 2
  $AV_{SS} < V0$, $Vd \leqq Vd + 1$, $V10 < AV_{DD}$ (where $d = 1$ to 9)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS $\left(\begin{array}{l}\text{Referenced to } AV_{DD} = 4.5 \text{ to } 5.5V,\ DV_{DD} = 3.0 \text{ to } AV_{DD},\ AV_{SS} = DV_{SS} = 0V \\ Ta = -20 \text{ to } 75°C \text{ unless otherwise noted}\end{array}\right)$

PARAMETER		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT	RELEVANT PIN
Input Voltage	Low Level	V_{IL}	—		0		$0.3 \times DV_{DD}$	V	Logic input
	High Level	V_{IH}			$0.7 \times DV_{DD}$		DV_{DD}		
Output Voltage	Low Level	V_{OL}	—	$I_{OL} = 1.0mA$	DV_{SS}		$DV_{SS} + 0.5$	V	Logic output
	High Level	V_{OH}		$I_{OH} = -1.0mA$	$DV_{DD} - 0.5$		DV_{DD}		
Output Current		Ichg	—	$V_{out} = AV_{DD} = 5V$ $V_X = 4V$ (Note)			-0.3	mA	D1 to D309
		Idis		$V_{out} = 0V$ $AV_{DD} = 5V, V_X = 1V$ (Note)	0.5				
Resistance Between Reference Analog Voltage Pins		R_{GMA}	—			30		$k\Omega$	V0 to V10
Output Voltage Deviation		V_{DO}	—			± 20		mV	D1 to D309
Leakage Current		I_{IN}	—		-1.0		1.0	μA	Logic input
Standby Current		ID_{STB}	—	fCPH = DC	-5.0	0.0	5.0	μA	DV_{DD}
Current Consumption		AI_{DD}	—	fCPH = 30MHz 1H = $30\mu s$, non-load Checkerboard pattern		7.0	10.0	mA	AV_{DD}
		DI_{DD}		fCPH = 30MHz 1H = $30\mu s$, non-load Checkerboard pattern		6.0	8.0		DV_{DD}

(Note) V_X denotes the voltage applied to the LCD panel drive pin.

AC CHARACTERISTICS $\left(\text{Referenced to } AV_{DD} = 4.5 \text{ to } 5.5V, DV_{DD} = 3.3V \text{ to } AV_{DD}, DV_{SS} = AV_{SS} = 0V\right.$
$\left.Ta = -20 \text{ to } 75°C \text{ unless otherwise noted}\right)$

PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
CPH Pulse Width H	tCWH	—		4.0			ns
CPH Pulse Width L	tCWL	—		4.0			ns
Enable Set-up Time	tsDI	—		4.0			ns
Enable Hold Time	thDI	—		0			ns
Enable Pulse Width H	tDWH	—			1.0		CPH period
Data Set-up Time	tsDD	—		4.0			ns
Data Hold Time	thDD	—		0			ns
Output Delay Time 1	tpdDO	—	$C_L = 35pF$			14.0	ns
Output Delay Time 2	tpdDE	—	$C_L = 2k\Omega + 75pF \times 2$ Target output voltage $+ AV_{DD} \times 0.1$			3.0	μs
Output Delay Time 3	tpdDX	—	$C_L = 2k\Omega + 75pF \times 2$ Target output voltage $\pm V_{DO}$			10.0	μs
LOAD Set-up Time 1	tsLD1	—		1.0			CPH period
LOAD Set-up Time 2	tsLD2	—		7.0			ns
LOAD Pulse Width H	tLWH	—		2.0			CPH period

CPH

tCWH

tCWL

$0.7 \times DV_{DD}$

$0.7 \times DV_{DD}$

$0.3 \times DV_{DD}$

$0.3 \times DV_{DD}$

DI / O, DO / I
(Input)

$0.7 \times DV_{DD}$

tsDI

thDI

$0.7 \times DV_{DD}$

CPH

$0.7 \times DV_{DD}$

DAn, DBn, DCn,
DDn, DEn, DFn
*n = 1 to 3

tsDD

thDD

$0.7 \times DV_{DD} / 0.3 \times DV_{DD}$

CPH

$0.7 \times DV_{DD}$

tpdDO

tDWH

DO / I, DI / O
(Output)

$0.7 \times DV_{DD}$

$0.7 \times DV_{DD}$

DAn, DBn, DCn,
DDn, DEn, DFn
*n = 1 to 3

VALID

LAST VALID

INVALID

CPH

$0.7 \times DV_{DD}$

DI / O, DO / I
(Input)

$0.7 \times DV_{DD}$

DAn, DBn, DCn,
DDn, DEn, DFn
*n = 1 to 3

VALID

VALID

LAST VALID

INVALID

tsLD2

tsLD1

LOAD

$0.7 \times DV_{DD}$

$0.7 \times DV_{DD}$

tLWH

tpdDE

D1 to D309

90%
10%

tpdDX   Target output voltage ± VDO