TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6B92

ROW DRIVER FOR A DOT MATRIX LCD

The T6B92 is a 100-channel output row driver for a STN dot matrix LCD. The T6B92 feature −30V LCD drive voltage. The T6B92 is able to drive LCD panels with a duty ratio up to 1/240. It is recommended to use with the T6B61A.

Unit : mm

T6B92	LEAD PITCH	
	IN	OUT
(UAN, 3NS)	1.00	0.23
(UBN, 3NS)	0.9	0.18

Please contact with TOSHIBA Agents for each Packaging Outline Dimensions.

TCP (Tape Carrier Package)

FEATURES

- Display duty application : ~1/240
- LCD drive signal : 100
- Data transfer : 1bit bidirectional
  ① O1→O100
  ② O1←O100
  ③ O1→O50, O51→O100
  ④ O1←O50, O51←O100
- LCD drive voltage : −11~−30V
- Power supply voltage : 2.7~5.5V
- Operating temperature : −20~75°C
- LCD drive output resistance : 800Ω MAX. (20V, 1/13 bias)
- Display off function : When /DSPOF is "L", All LCD drive outputs (O1~O100) stop on V_0 level
- LCD drive output timing : Change on fall edge of LP

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- Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do , that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.
- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
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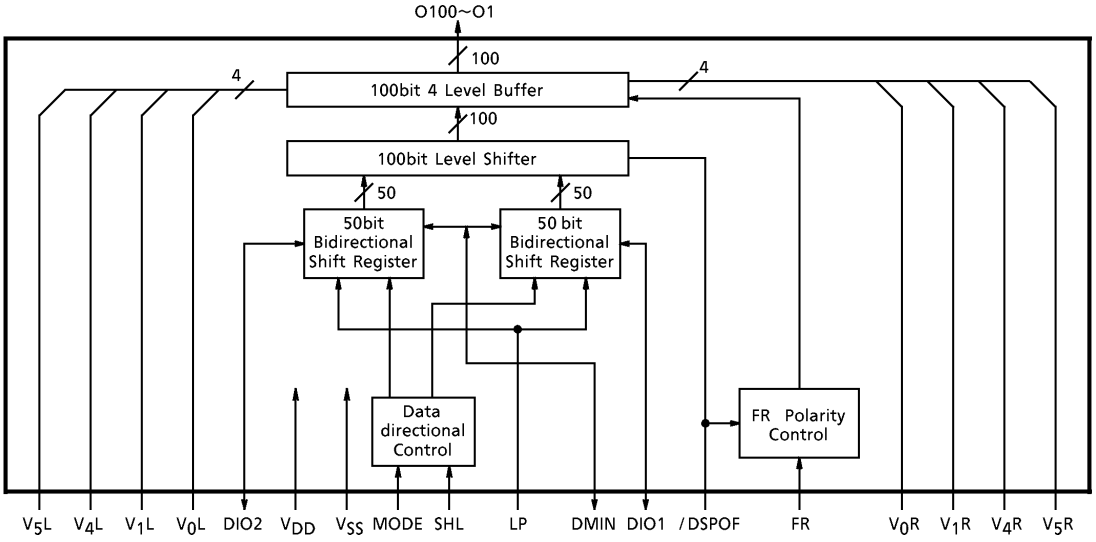
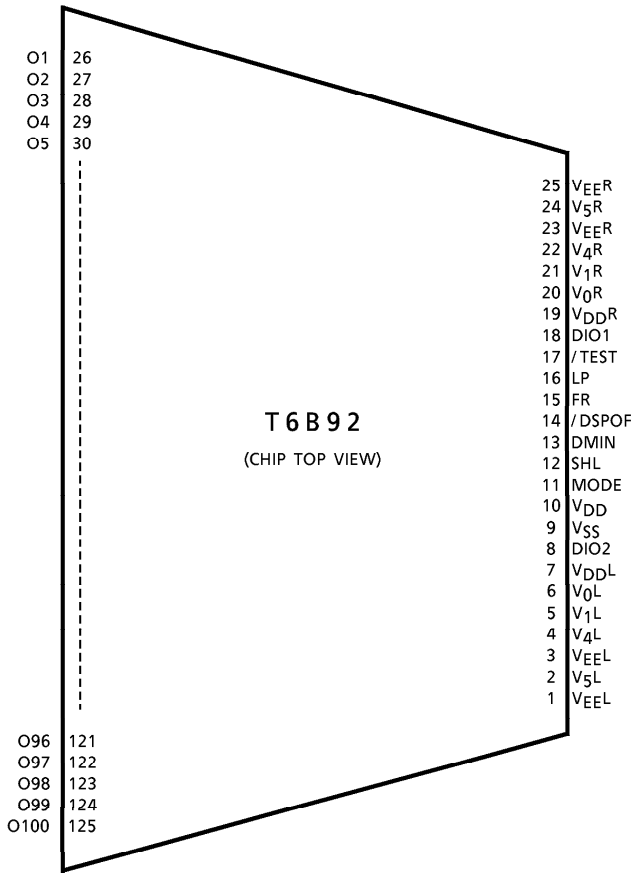
BLOCK DIAGRAM



PIN CONNECTION



* Above drawing describes pin configuration of the LSI chip, but of the tape carrier package.

PIN FUNCTIONS

PIN NAME	I/O	FUNCTIONS	LEVEL
O1~O100	O	Output for LCD drive signal	V_0-V_5
DIO1, DIO2	I/O	Input/Output for shift data SHL = "L" : DIO1 input, DIO2 output SHL = "H" : DIO1 output, DIO2 input	V_{DD}-V_{SS}
DMIN	I	Dual Mode Input/Output for shift data Single Mode = V_{DD} or V_{SS} select	
LP	I	(Shift Clock Pulse) Input for Shift Clock Pulse	
FR	I	(Frame) Input for frame signal	
MODE	I	(Dual Mode) Terminal for dual input mode ("H") or single input mode select ("L")	
SHL	I	(Direction) Input for data flow direction select	
/DSPOF	I	(Display Off) /DSPOF = "L": Display off mode, (O1~O100) stop on V_0 level. /DSPOF = "H": Display on mode, (O1~O100) operate.	
/TEST	I	(Test) /Test : "H"	
V_{DD}	—	Power supply for internal logic (5V)	—
V_{SS}	—	Power supply for internal logic (0V)	
V_{DD}L·R	—	Ditto	
V_5L·R	—	Ditto	
V_4L·R	—	Ditto	
V_1L·R	—	Ditto	
V_0L·R	—	Ditto	
V_{EE}L·R	—	Ditto	

FORMAT FOR FR, DATA INPUT AND OUTPUT LEVEL

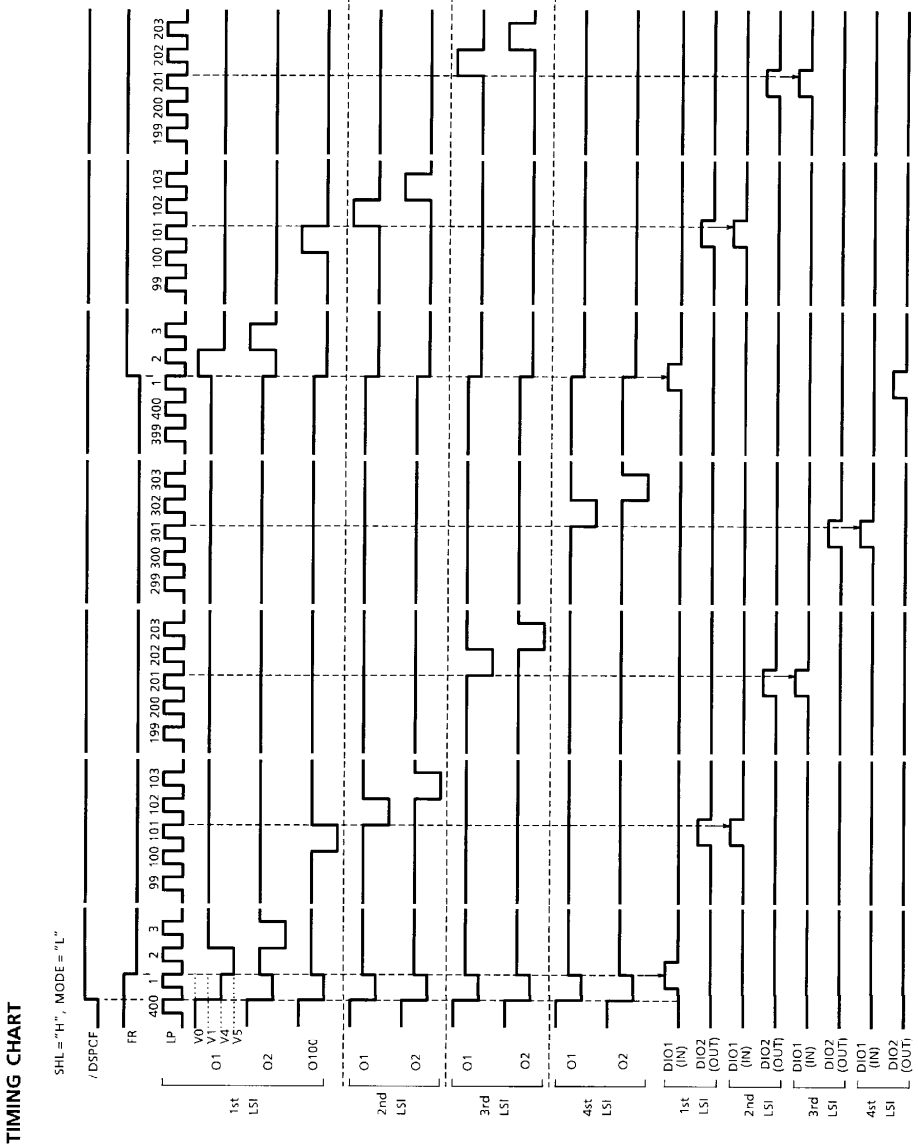
F R	DATA INPUT (DIO1, DIO2, DMIN)	/ DSPOF	OUTPUT LEVEL
L	L	H	V_1
L	H	H	V_5
H	L	H	V_4
H	H	H	V_0
*	*	L	V_0

* Don't Care

FORMAT FOR DATA INPUT

MODE	SHL	DATA FLOW	DATA INPUT TERMINALS		
			DIO1	DIO2	DMIN
L	L	O1→O100	IN	OUT	*
L	H	O100→O1	OUT	IN	*
H	L	O1→O50	IN	OUT	IN
		O51→O100	IN	OUT	IN
H	H	O50→O1	OUT	IN	IN
		O100→O51	OUT	IN	IN

TIMING CHART



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MAXIMUM RATINGS

(Keep the following conditions, $V_{DD} \geqq V_0 \geqq V_1 \geqq V_4 \geqq V_5 \geqq V_{EE}$)

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	V_{DD}	V_{DD}	−0.3~7.0	V
Supply Voltage 2	V_{EE}	V_{EE}L / R	V_{DD} − 32.0~V_{DD} + 0.3	V
Supply Voltage 3	V_0	V_0L / R	V_{DD} − 32.0~V_{DD} + 0.3	V
Supply Voltage 4	V_1	V_1L / R	V_{EE} − 32.0~V_{DD} + 0.3	V
Supply Voltage 5	V_4, V_5	V_4L / R, V_5L / R	V_{EE} − 32.0~V_{DD} + 0.3	V
Input Voltage	V_{in}	(*1)	−0.3~V_{DD} + 0.3	V
Operating Temperature	T_{opr}	—	−20~75	°C
Storage Temperature	T_{stg}	—	−55~125	°C

(*1) FR, DIO1, DIO2, LP, / DSPOF, / TEST

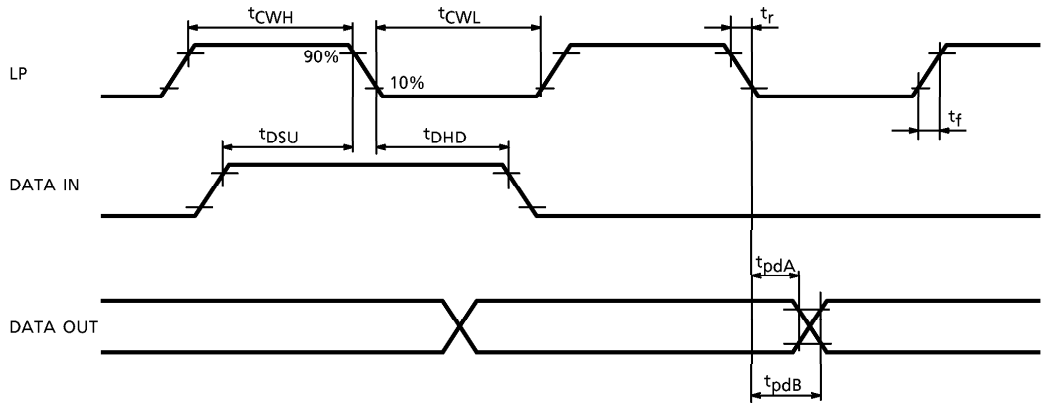
ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Unless otherwise noted, V_{SS} = 0V, V_{DD} = 2.7~5.5V, Ta = −20~75°C)

ITEM		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	PIN NAME
Supply Voltage 1		V_{DD}	—		2.7	5.0	5.5	V	V_{DD}
Supply Voltage 2		V_{EE}	—		V_{DD} − 30.0	—	V_{DD} − 11.0	V	V_{EE}L / R
Input Voltage	"H" Level	V_{IH}	—		0.8 V_{DD}	—	V_{DD}	V	FR, SHL, DIO1, DIO2, DMIN, MODE, LP, / DSPOF, / TEST
	"L" Level	V_{IL}			0	—	0.2 V_{DD}		
Output Voltage	"H" Level	V_{OH}	—	I_{OH} = −0.5mA	V_{DD} − 0.5	—	V_{DD}	V	DIO1, DIO2
	"L" Level	V_{OL}		I_{OL} = 0.5mA	V_{SS}	—	0.5		
Output Resistance	"H" Level	R_{OH}	—	$V_{OUT} = V_0 - 0.5V$ (*2)	—	450	800	Ω	O1~O100
	"M" Level	R_{OM}		$V_{OUT} = V_1 \pm 0.5V$ (*2)	—	450	800		
		R_{OM}		$V_{OUT} = V_4 \pm 0.5V$ (*2)	—	450	800		
	"L" Level	R_{OL}		$V_{OUT} = V_5 + 0.5V$ (*2)	—	450	800		
Current Consumption		I_{SS}	—	V_{DD} = 5.5V V5 = −24.5V f_{FR} = 40Hz f_{LP} = 19.2kHz f_{DIO} = 80Hz V_{IH} = 5.5V, V_{IL} = 0V	—	—	10	μA	V_{SS}

(*2) V_{EE} = 20V, 1 / 13 bias

AC CHARACTERISTICS



TEST CONDITIONS 1 (V_{SS} = 0V, V_{DD} = 2.7~4.5V, V_5 = (V_{DD} – 30)~(V_{DD} – 11) V, Ta = – 20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Clock Pulse	t_C	LP	500	—	ns
LP Pulse Width "H"	t_{CWH}	LP	60	—	ns
LP Pulse Width "L"	t_{CWL}	LP	170	—	ns
Input Rise / Fall Time	t_r, t_f	LP, FR, DIO1, DIO2, DMIN	—	(*4)	ns
Data Set Up Time	t_{DSU}	DIO1, DIO2	100	—	ns
Data Hold Time	t_{DHD}	DIO1, DIO2	0	—	ns
Output Data Delay Time A (*3)	tpdA	DIO1, DIO2	40	—	ns
Output Data Delay Time B (*3)	tpdB	DIO1, DIO2	—	350	ns

(*3) C_L = 10pF

(*4) t_r, $t_f \leqq (t_C - t_{CWH} - t_{CWL}) / 2$ and t_r, $t_f \leqq 50$ns

TEST CONDITIONS 2 (V_{SS} = 0V, V_{DD} = 4.5~5.5V, V_5 = (V_{DD} – 30)~(V_{DD} – 11) V, Ta = – 20~75°C)

ITEM	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Clock Pulse	t_C	LP	330	—	ns
LP Pulse Width "H"	t_{CWH}	LP	40	—	ns
LP Pulse Width "L"	t_{CWL}	LP	150	—	ns
Input Rise / Fall Time	t_r, t_f	LP, FR, DIO1, DIO2, DMIN	—	(*6)	ns
Data Set Up Time	t_{DSU}	DIO1, DIO2	50	—	ns
Data Hold Time	t_{DHD}	DIO1, DIO2	0	—	ns
Output Data Delay Time A (*5)	tpdA	DIO1, DIO2	20	—	ns
Output Data Delay Time B (*5)	tpdB	DIO1, DIO2	—	200	ns

(*5) C_L = 10pF

(*6) t_r, $t_f \leqq (t_C - t_{CWH} - t_{CWL}) / 2$ and t_r, $t_f \leqq 50$ns

NOTE

Insert the bypass capacitor (0.1μF) between V_{DD} and V_{SS} to decrease the noise on power supply. Place the bypass capacitor as closer to the LSI as possible.