

TC74AC521P, TC74AC521F, TC74AC521FW

8-BIT EQUALITY COMPARATOR

The TC74AC521 is an advanced high speed CMOS 8-BIT DIGITAL COMPARATOR fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It compares two 8-bit binary or BCD words applied inputs P₀~P₇, and inputs Q₀~Q₇, and indicates whether or not they are equal.

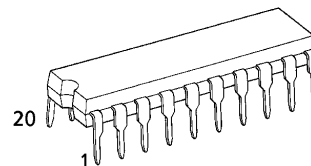
A signal active low enable is provided to facilitate cascading of several packages to compare of words greater than 8 bits.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

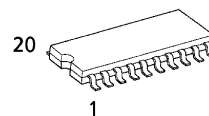
FEATURES:

- High Speed..... $t_{pd} = 6.4ns(typ.)$ at $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 8\mu A(Max.)$ at $T_a = 25^\circ C^*$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (Min.)$
- Symmetrical Output Impedance... $|I_{OH}| = |I_{OL}| = 24mA(Min.)$
Capability of driving 50 Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range... $V_{CC}(opr.) = 2V \sim 5.5V$
- Pin and Function Compatible with 74F521

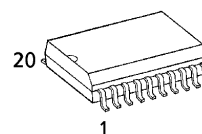
(Note) The JEDEC SOP (FW) is not available in Japan.



P (DIP20-P-300-2.54A)
Weight : 1.30g (Typ.)

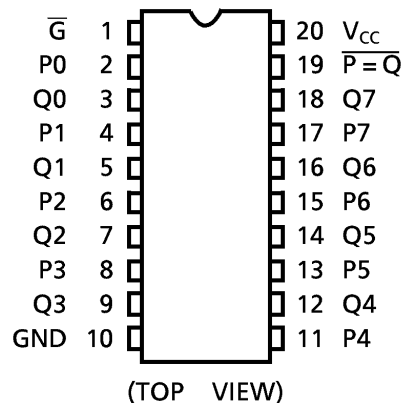


F (SOP20-P-300-1.27)
Weight : 0.22g (Typ.)



FW (SOL20-P-300-1.27)
Weight : 0.46g (Typ.)

PIN ASSIGNMENT



TRUTH TABLE

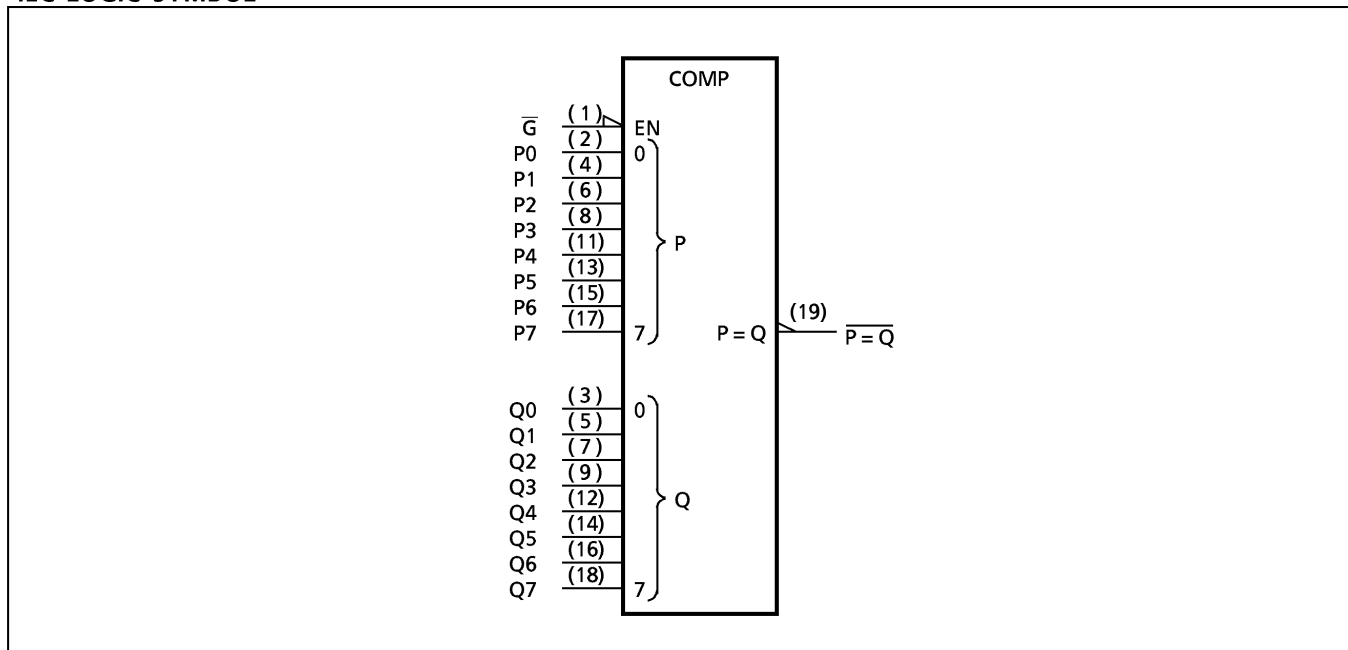
INPUTS		OUTPUT
P, Q	$\bar{G}$	$\bar{P} = \bar{Q}$
$P = Q$	L	L
$P \neq Q$	L	H
X	H	H

X : Don't Care

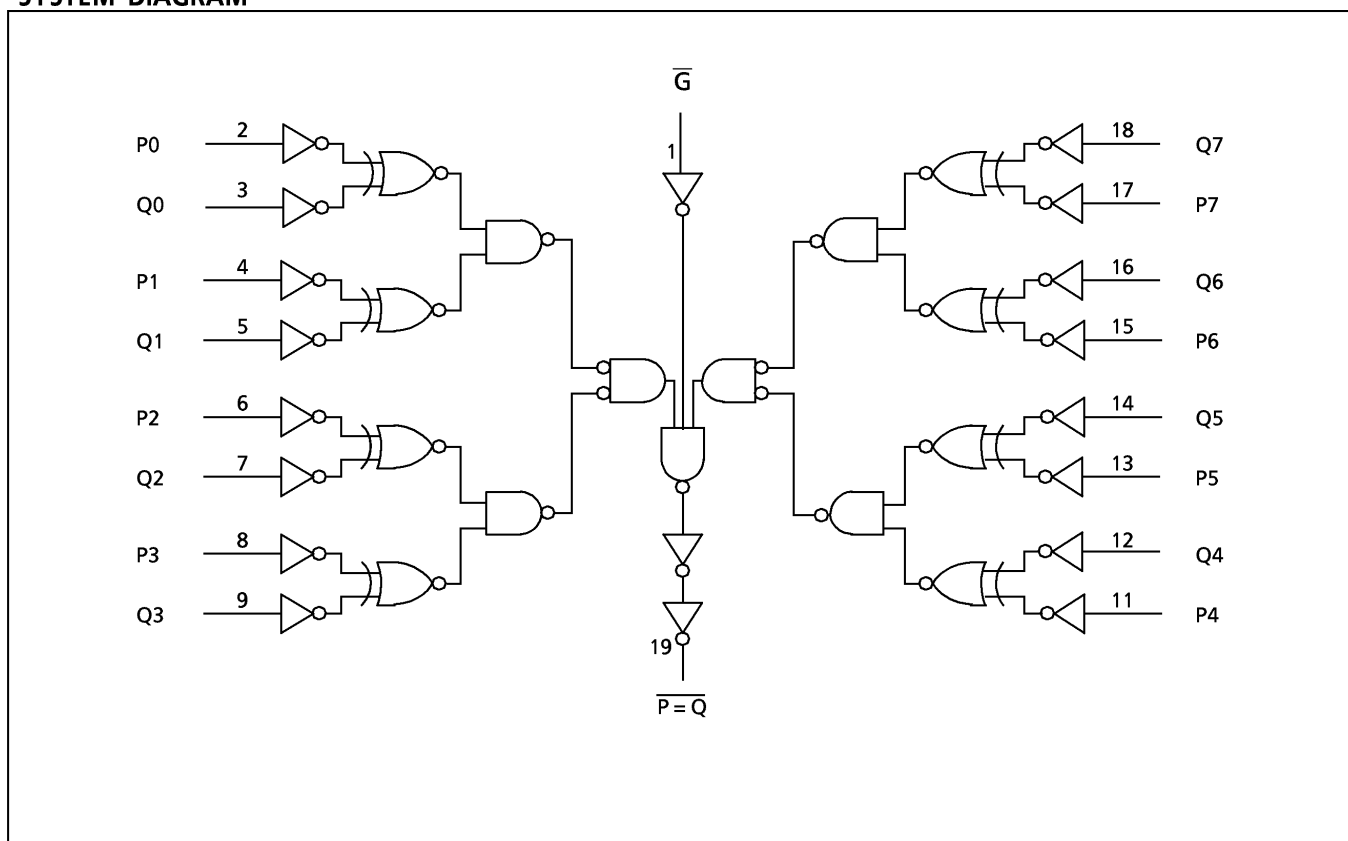
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IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	dt/dV	$0 \sim 100$ ($V_{CC} = 3.3 \pm 0.3\text{V}$) $0 \sim 20$ ($V_{CC} = 5 \pm 0.5\text{V}$)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V
			3.0	2.10	—	—	2.10	—	
			5.5	3.85	—	—	3.85	—	
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V
			3.0	—	—	0.90	—	0.90	
			5.5	—	—	1.65	—	1.65	
High - Level Output Voltage	V_{OH}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OH} = -50\mu\text{A}$	2.0	1.9	2.0	—	1.9	V
				3.0	2.9	3.0	—	2.9	
		$I_{OH} = -4\text{mA}$ $I_{OH} = -24\text{mA}$ $I_{OH} = -75\text{mA}^*$		4.5	4.4	4.5	—	4.4	
				3.0	2.58	—	—	2.48	
				4.5	3.94	—	—	3.80	
				5.5	—	—	—	3.85	
Low - Level Output Voltage	V_{OL}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OL} = 50\mu\text{A}$	2.0	—	0.0	0.1	—	V
				3.0	—	0.0	0.1	—	
		$I_{OL} = 12\text{mA}$ $I_{OL} = 24\text{mA}$ $I_{OL} = 75\text{mA}^*$		4.5	—	0.0	0.1	—	
				3.0	—	—	0.36	—	
				4.5	—	—	0.36	—	
				5.5	—	—	—	—	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	—	80.0	

* : This spec indicates the capability of driving 50Ω transmission lines.

One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.
Propagation Delay Time ($P_n, Q_n - \overline{P} = \overline{Q}$)	t_{pLH} t_{pHL}		3.3 ± 0.3	—	10.5	17.5	1.0	20.0
			5.0 ± 0.5	—	7.2	11.0	1.0	12.5
Propagation Delay Time ($\overline{G} - \overline{P} = \overline{Q}$)	t_{pLH} t_{pHL}		3.3 ± 0.3	—	7.2	11.5	1.0	13.0
			5.0 ± 0.5	—	4.8	7.0	1.0	8.0
Input Capacitance	C _{IN}			—	5	10	—	10
Power Dissipation Capacitance	C _{PD} (1)			—	34	—	—	—

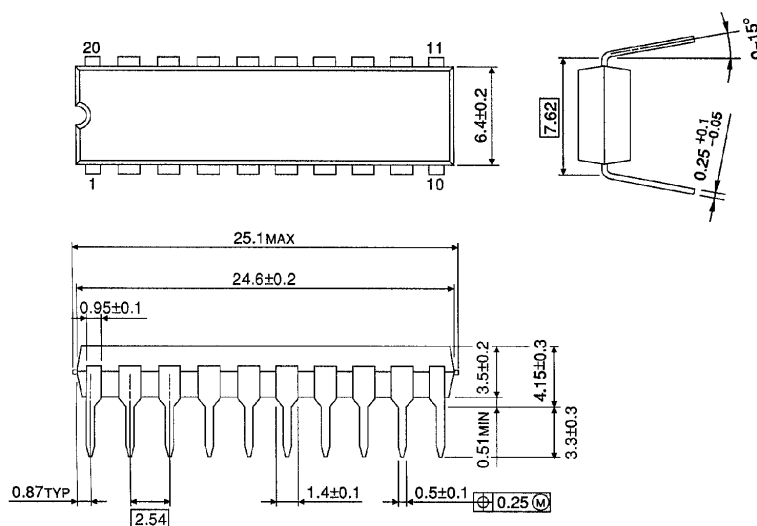
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)

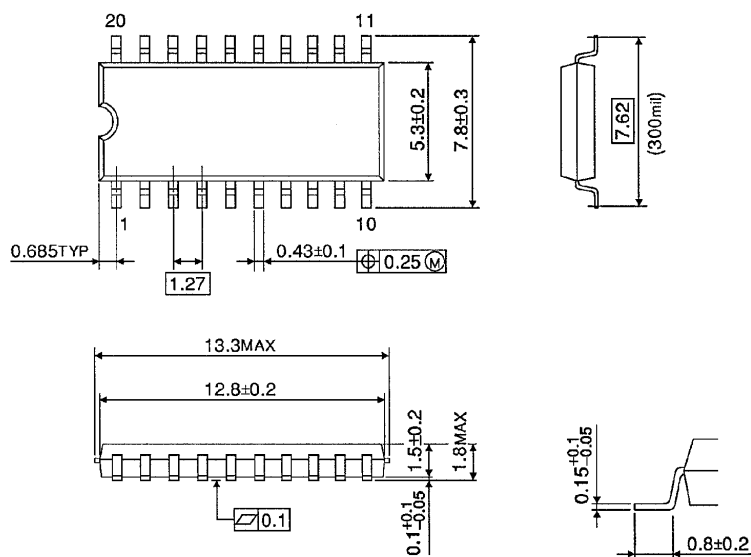
Unit in mm



Weight : 1.30g (Typ.)

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)

Unit in mm

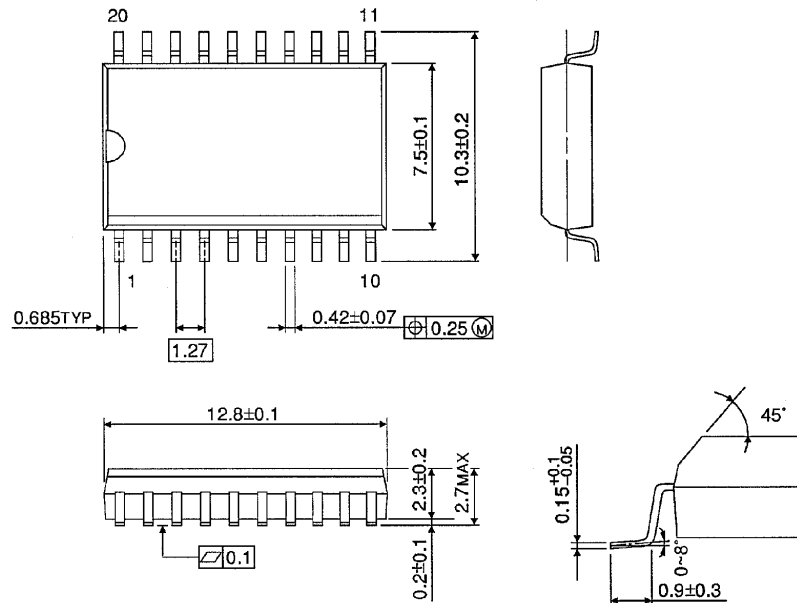


Weight : 0.22g (Typ.)

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)