TOSHIBA

8-bit Microcontroller
TLCS-870/C Series
Application Note
(TMP86CM29)

Rev.1.0 22-May-2000

TOSHIBA CORPORATION

Preface

Thank you very much for making use of TOSHIBA semiconductor products.

Toshiba has a broad range of microcomputers which are applicable to various fields ranging from consumer to industrial. The microcomputers have the development support systems and the reference application software to reduce application software development periods.

Toshiba 4-bit and 8-bit single chip microcomputers include wide range lineups from small-scale system 4-bit microcomputers, TLCS-47E series and 4-bit microcomputers, TLCS-47, 470 and 470A series which have various peripheral circuits and abundant types to 8-bit microcomputers, TLCS-870, 870/X, and 90 series which have large memory and realize high-level processing to support diverse applications and satisfy various needs.

This document describes the specifications of the demonstration set for Toshiba original 8-bit microcontroller TMP86Cx29. Specific examples that can be referred to for software development are also provided.

TLCS-870/C series attains design optimization with TLCS-870/X series at a base, and has realized further low power consumption. In addition, it adopts the command system which has improved an object efficiency of the C language, and offers the high cost performance.

Toshiba intends the microcomputers which have one-time PROM to add to the lineup, which are used for program debugging, system evaluation and pre-production at the application system development stage. It enables operating in low voltage and low power consumption.

For any engineering questions of the product described in this document, please do not hesitate to contact the local Toshiba sales representative.

Toshiba endeavors to write exactly and includes the latest information in this document.

If any idea that may occur to your mind regarding this documentation, please do not hesitate to point out.

Contents

1. Overview

This system is used to perform demonstrations and tests for the TMP86Cx29. There are three types of operating modes as shown below:

- Voltmeter mode
- Test mode
- ROM/RAM Check mode

The operating mode of the system can be judged by LED1. When LED1 is "ON", the system is in Voltmeter mode. When LED1 is "OFF", the system is either in Test mode or ROM/RAM Check mode. For the position of LEDs , see "3.2 Display Section".

1.1 Overview of Voltmeter Mode

In Voltmeter mode, a voltmeter is realized by using a 10-bit AD converter, LCD driver, etc.

Voltmeter mode has the following four types of modes:

- Standard voltmeter mode
- Voltage level monitor mode
- Voltage change monitor mode
- Voltage level compare mode

Note also that if no key input is made for a fixed period of time (ca. 60 seconds), Voltage mode shifts to the "power-saving mode" to temporarily suspend the functions of the microcontroller.

1.2 Overview of Test Mode

In Test mode, the waveforms of timer cycle, serial communication data, etc are measured by using an external connecting pin so that the system can check whether each function of the microcontroller is operating according to the set values.

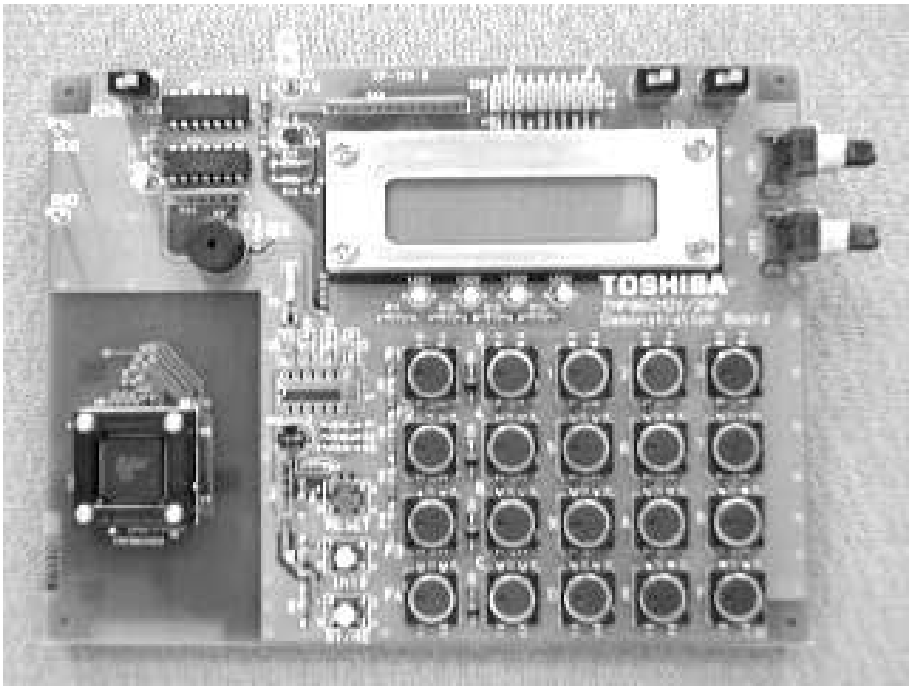
Tests can be made on the following functions:

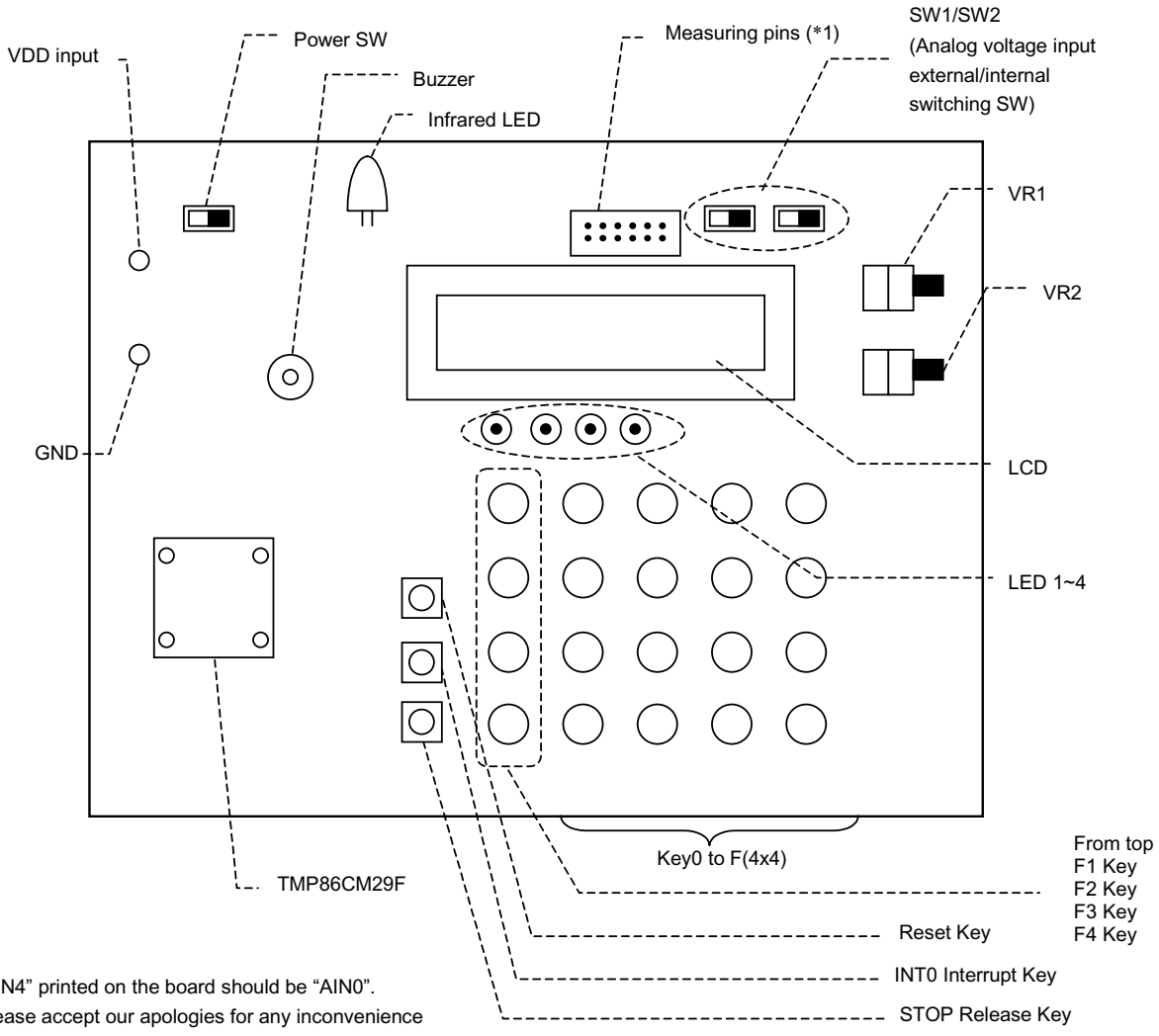
- TBT
- WDT
- TC1
- TC3
- TC4
- 16bit TC3 + 4
- TC5
- TC6
- 16bit TC5+6
- UART
- SIO
- AD converter
- Continuous test

1.3 Overview of ROM/RAM Check Mode

ROM/RAM Check mode is used to display the check sum of internal ROM and address in RAM where Read/Write are not performed properly.

Key operation is not available in this mode. After the check sum and abnormal RAM address are displayed, only "Reset Key" is accepted.





(*1) "AIN4" printed on the board should be "AIN0".
Please accept our apologies for any inconvenience this may have caused you.

2. Setting Operating Mode

The operating mode can be selected by pressing an appropriate key at power-up/reset. When **Key0** is pressed at power-up/reset, it becomes Test mode. When **Key1** is pressed, it becomes ROM/RAM Check mode. When one of other keys or no key is pressed, Voltmeter mode is selected.

For the placement of keys, see "3.1 Key Placement and Names".

3. Display and Key Placement

3.1 Key Placement and Names

Figure 3.1.1 shows the key placement and key names.

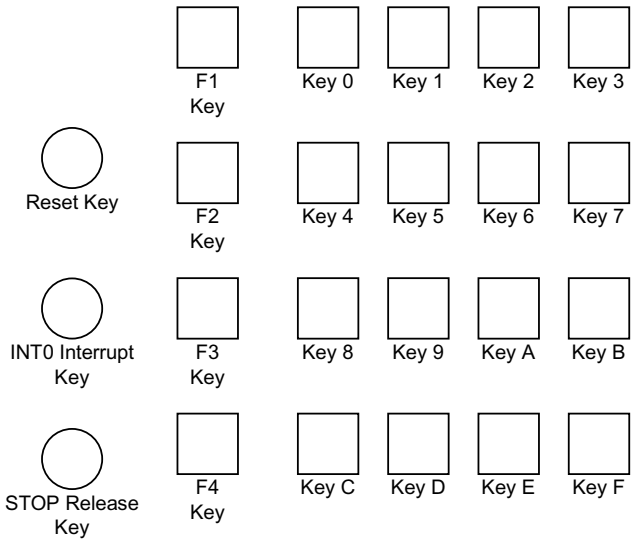


Figure 3.1.1 Key Placement

3.2 Display Section

Figure 3.2.1 shows an external view of the display section.

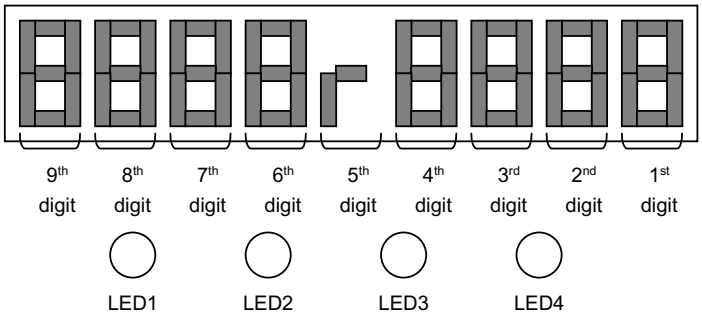


Figure 3.2.1 External View of Display Section

4. I/O Port

4.1 Pin Assignments

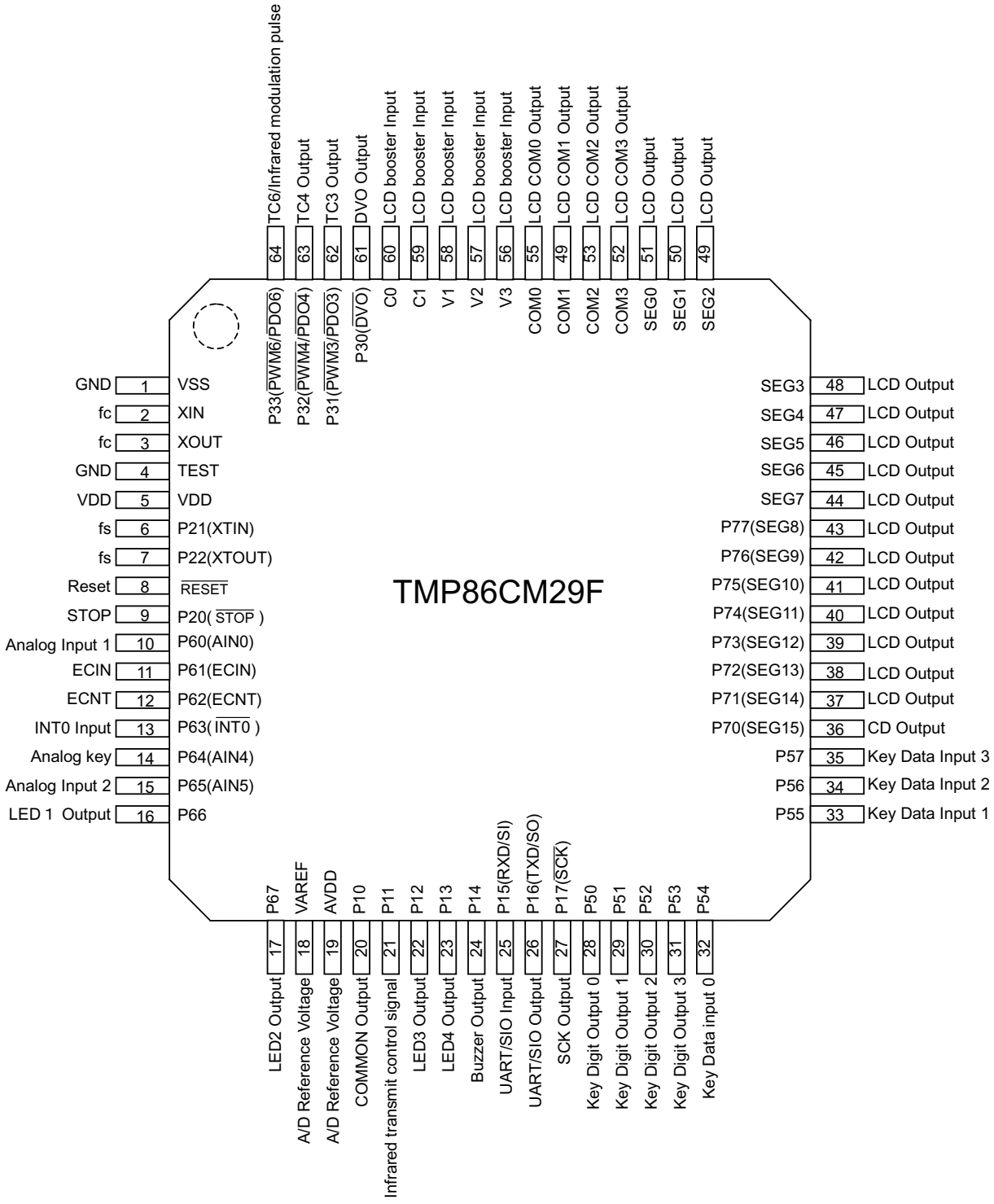


Figure 4.1.1 Pins for Measurement

4.2 Pin Functions (TMP86CM29F)

No	Pin Name	Signal Name	Structure (Initial Value)	Remarks
1	VSS	Ground	—	
2	XIN	High-frequency Resonator Connection	—	8MHz
3	XOUT	High-frequency Resonator Connection	—	8MHz
4	TEST	Test Input	—	Not used (GND)
5	VDD	Power Supply Input	—	VDD = 5[V]
6	P21(XTIN)	Low-frequency Resonator Connection	SkOd(Z)	32.768KHz
7	P22(XTOUT)	Low-frequency Resonator Connection	SkOd(Z)	
8	$\overline{\text{RESET}}$	Reset Input	—	Reset input
9	P20($\overline{\text{INT5}}$ / $\overline{\text{STOP}}$)	STOP Input	SkOd(Z)	
10	P60(AIN0)	Analog Input 1	TriS(Z)	VR/external input to be switched by SW1
11	P61(AIN1/ECIN)	ECIN Output	TriS(Z)	
12	P62(AIN2/ECNT)	ECNT Output	TriS(Z)	
13	P63(AIN3/ $\overline{\text{INT0}}$)	INT0 Input	TriS(Z)	
14	P64(AIN4/STOP2)	Analog Key Input (AIN4)	TriS(Z)	
15	P65(AIN5/STOP3)	Analog Input 2	TriS(Z)	VR/external input to be switched by SW2
16	P66(AIN6/STOP4)	LED 1 Output	TriS(Z)	
17	P67(AIN7/STOP5)	LED 2 Output	TriS(Z)	
18	VAREF	AD Reference Voltage	—	
19	AVDD	AD Reference Voltage	—	
20	P10(SEG31)	COMMON Output	SkOd(Z)	
21	P11(SEG30)	Infrared Transmit Control Signal	SkOd(Z)	
22	P12(SEG29/INT1)	LED3 Output	SkOd(Z)	
23	P13(SEG28/INT2)	LED4 Output	SkOd(Z)	
24	P14(SEG27/INT3)	Buzzer Output	SkOd(Z)	
25	P15(SEG26/RXD/SI)	UART/SIO Input	SkOd(Z)	
26	P16(SEG25/TXD/SO)	UART/SIO Output	SkOd(Z)	
27	P17(SEG24/ $\overline{\text{SCK}}$)	SCK Output	SkOd(Z)	
28	P50(SEG23)	Key Digit Output 0	SkOd(Z)	
29	P51(SEG22)	Key Digit Output 1	SkOd(Z)	
30	P52(SEG21)	Key Digit Output 2	SkOd(Z)	
31	P53(SEG20)	Key Digit Output 3	SkOd(Z)	
32	P54(SEG19)	Key Data Input 0	SkOd(Z)	
33	P55(SEG18)	Key Data Input 1	SkOd(Z)	
34	P56(SEG17)	Key Data Input 2	SkOd(Z)	
35	P57(SEG16)	Key Data Input 3	SkOd(Z)	
36	P70(SEG15)	LCD Data Output	SkOd(Z)	
37	P71(SEG14)	LCD Data Output	SkOd(Z)	
38	P72(SEG13)	LCD Data Output	SkOd(Z)	
39	P73(SEG12)	LCD Data Output	SkOd(Z)	
40	P74(SEG11)	LCD Data Output	SkOd(Z)	
41	P75(SEG10)	LCD Data Output	SkOd(Z)	
42	P76(SEG9)	LCD Data Output	SkOd(Z)	
43	P77(SEG8)	LCD Data Output	SkOd(Z)	

Sk0d (Z) Sink Open Drain (Z)
TriS (Z) Tri-state (Z)
PcPp (Z) Push Pull with P-channel Control (Z)

No	Pin Name	Signal Name	Structure (Initial Value)	Remarks
44	SEG7	LCD Data Output	—	
45	SEG6	LCD Data Output	—	
46	SEG5	LCD Data Output	—	
47	SEG4	LCD Data Output	—	
48	SEG3	LCD data Output	—	
49	SEG2	LCD data Output	—	
50	SEG1	LCD data Output	—	
51	SEG0	LCD data Output	—	
52	COM3	LCD COM3 Output	—	
53	COM2	LCD COM2 Output	—	
54	COM1	LCD COM1 Output	—	
55	COM0	LCD COM0 Output	—	
56	V3	Booster Pin for LCD Drive	—	
57	V2	Booster Pin for LCD Drive	—	
58	V1	Booster Pin for LCD Drive	—	
59	C1	Booster Pin for LCD Drive	—	
60	C0	Booster Pin for LCD Drive	—	
61	P30($\overline{\text{DVO}}$)	DVO Output	PcPp(Z)	
62	P31($\overline{\text{PWM3}}$ / $\overline{\text{PDO3}}$ / TC3)	TC3 Output	PcPp(Z)	
63	P32($\overline{\text{PWM4}}$ / $\overline{\text{PDO4}}$ / $\overline{\text{PPG4}}$ / TC4)	TC4 Output	PcPp(Z)	
64	P33($\overline{\text{PWM6}}$ / $\overline{\text{PDO6}}$ / $\overline{\text{PPG6}}$ TC6)	TC6/Infrared Modulation Pulse	PcPp(Z)	38KHz carrier output

Sk0d (Z) Sink Open Drain (Z)
TriS (Z) Tri-state (Z)
PcPp (Z) Push Pull with P-channel Control (Z)

5. Software Specifications

5.1 Digital Voltmeter by AD Converter

5.1.1 Overview

A digital voltmeter is realized by using Analog Input 1 and Analog Input 2 of the 10-bit AD converter.

Analog Input 1 and Analog Input 2 are connected to the AIN0 and AIN5 pins of the microcontroller, respectively. With the AD input switching switches (SW1/SW2), "input from voltage value divided by VR1/VR2" and "external input" can be switched. The maximum input voltage to the AD converter is VDD.

This voltmeter has the four main modes:

- Standard voltmeter mode
- Voltage level monitor mode
- Voltage change monitor mode
- Voltage level compare mode

Analog Input 1 and Analog Input 2 can be selected in the standard mode and the voltage change monitor mode, respectively.

In the AD converter, the reference voltage is 0 to 5V, and the input voltage is sampled as shown in the following equation:

$$AD\ conversion\ value[bit] = 10[bit] \times Input\ voltage\ [V]/5[V]$$

Each analog input gets a sampling value per 0.1[ms] and a mean value is calculated after a certain times. Then processing is executed.

Values measured in each mode can be displayed on LCD. They can also be transmitted with "F4Key" input by using infrared LED. While data is transmitted, Key input is suspended. The infrared transmit data format will be shown in the description of each mode.

In this voltmeter, if no key operation is made for more than 1 minute, the power-saving mode is entered to suspend AD conversion, key operation, and LCD display. Only by pressing "STOP Release Key" can the power-saving mode be released to return to normal processing.

- Some infrared transmit data may cause other home appliance to malfunction. Please check before using this voltmeter.
- This voltmeter uses VDD input voltage (5V) as a reference voltage of AD conversion (VAREF). Note therefore that there may be a difference between an actual voltage and displayed voltage due to VDD input voltage.

5.1.2 Mode Transition Diagram

Figure 5.1.1 shows the transition of voltmeter modes.

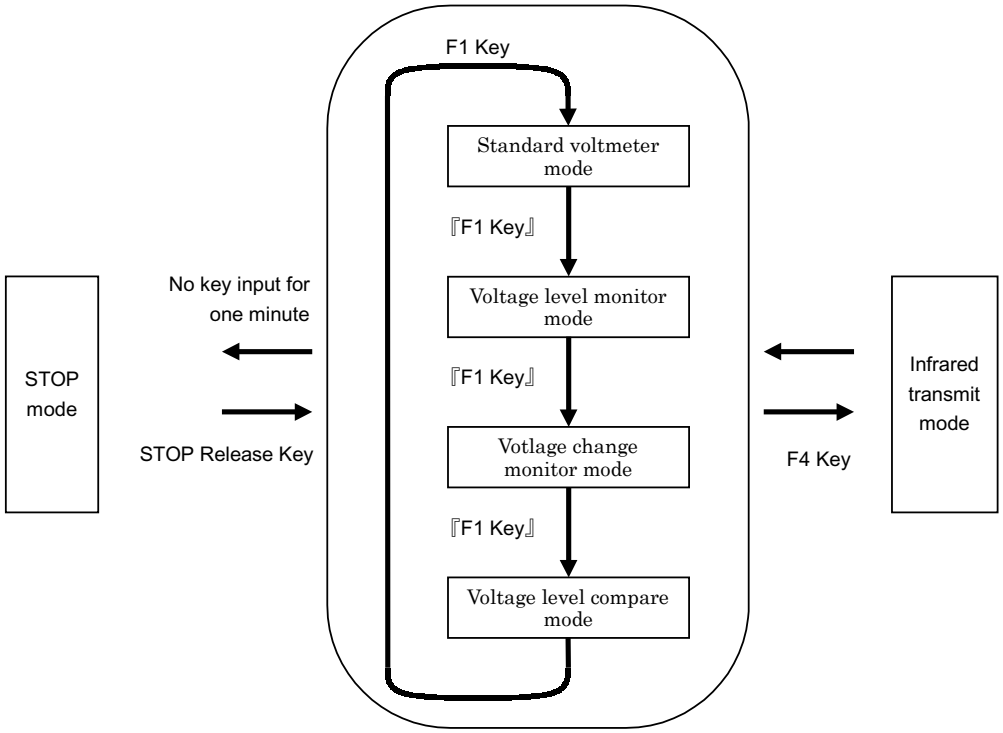


Figure 5.1.1 Mode Transition Diagram

5.1.3 Detailed Description of Each Mode of Voltmeter

5.1.3.1 Voltmeter Mode

In this mode, a voltage from the specified analog input is measured and displayed on LCD.

LED/LCD display

Only LED1 is "ON" and LED 2 to LED 4 are "OFF".

The 8th digit on LCD displays the analog input number currently selected. The 6th digit displays the first digit of a voltage measurement value, which is followed by up to the third decimal place.

In the initial state, Analog Input 1 is selected for analog input.

Figure 5.1.2 shows an example of LED/LCD display with Analog Input 1 and a voltage measurement value of 3.267[V].

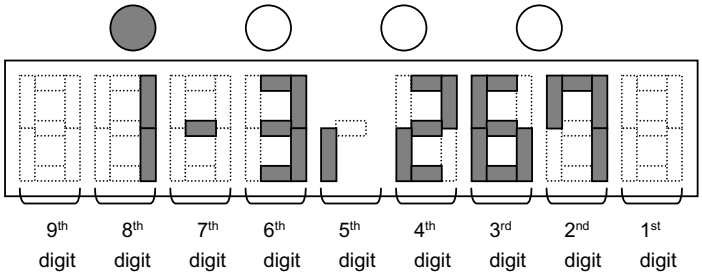


Figure 5.1.2 Example of Display in Voltmeter Mode

Key operation

"F1 Key" input ends the voltmeter mode and the mode changes to the voltage level monitor mode.

"F2 Key" input can be used to switch between Analog Input 1 and Analog Input 2. Switching updates the 8th digit on LCD and it displays the number of analog input currently used.

"F4 Key" input can be used to transmit the analog input number currently selected and a 10-bit AD measurement value by using infrared LED. For the transmit format, see "5.1.4 Infrared Transmit Format".

Figure 5.1.3 shows an example of display when "F2 Key" input is made.

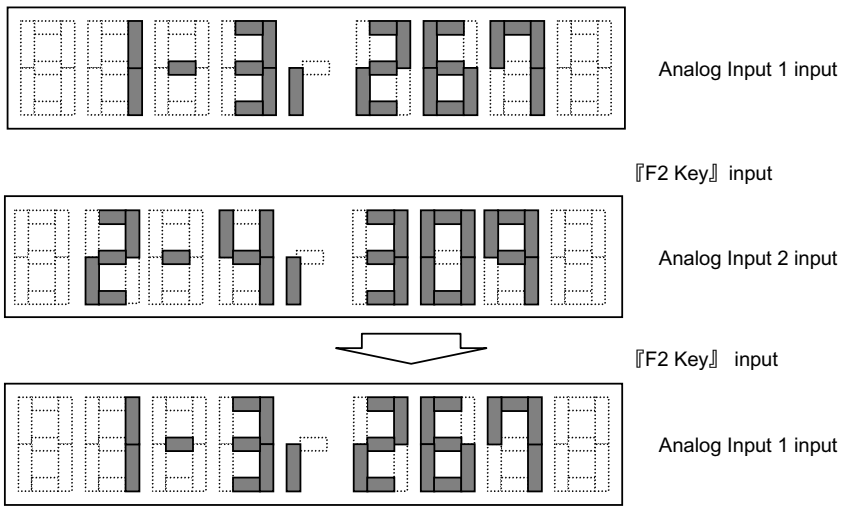


Figure 5.1.3 Example of Switching Input in Voltmeter Mode

5.1.3.2 Voltage Level Monitor Mode

In this mode, measurement values from analog input are monitored. When the value gets lower than the voltage monitor level, a buzzer sounds and LED 2 blinks as a warning.

LED/LCD display

LED2 is "ON" and LED 3 and LED 4 are "OFF".

The 9th digit on LCD displays the first digit of the voltage monitor level, which is followed by up to the second decimal place. The 4th digit displays the first digit of a voltage measurement value, which is followed by up to the second decimal place. In the voltage level monitor mode, the analog input number is fixed to Analog Input 1.

Upon power-up and reset, the voltage monitor level is cleared to 0.00[V].

Figure 5.1.4 shows an example of LED/LCD display when the voltage monitor level is 2.13[V] and the voltage measurement value is 3.47[V].

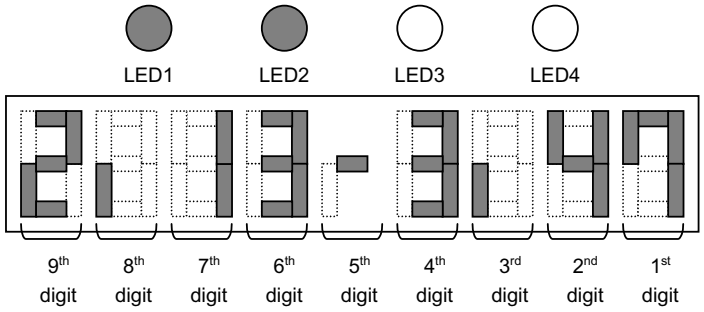


Figure 5.1.4 Example of Display in Voltage Level Monitor Mode

Key operation

"F1 Key" input ends the voltage monitor mode and the mode changes to the voltage change monitor mode. At this time, the voltage monitor level that has been set is maintained.

"F3 Key" input is used to enter the monitor level setting state. When this state is entered, monitoring of voltage level is stopped and the 9th digit on LCD starts blinking. The 4th to 1st digits that normally display a voltage measurement value are all lit during the monitor level setting state. When one of the keys from "Key0" to "Key9" is pressed while LCD is blinking ("Key0 – Key5" while the 9th digit is blinking), the number of pressed key is input to the blinking digit and is temporarily set and displayed as the monitor level.

The voltage monitor level can be set to 0.00 to 5.00.

Once in the monitor level setting state, by further pressing "F3Key", the position of blinking digit moves from the 9th to the lower digits so that the 7th and 6th digits can be set. Note that when "5" is input to the 9th digit, "0" is automatically set to both the 7th and 6th digits.

When "F3 Key" is input while the 6th digit is blinking or "F3 Key" is input after "5" is input to while the 9th digit is blinking, LCD stops blinking and the values set to the 9th to 6th digits are fixed as the monitor level. The state then goes back to the voltage level monitor state.

The voltage monitor level is not fixed until "F3 Key" is input on the 6th digit or "F3 Key" is input after "5" is set to the 9^{th} digit. Therefore, if "F1Key" is pressed to enter the voltage change monitor mode while the monitor level setting is performed, the monitor level before change is saved.

"F4 Key" input can be used to transmit a current voltage monitor level and a 10-bit A/D measurement value from Analog Input 1 by using infrared LED. For the transmit format, see "5.1.4 Infrared Transmit Format".

Figure 5.1.5 shows an example for setting the monitor level by "F3 Key" input.

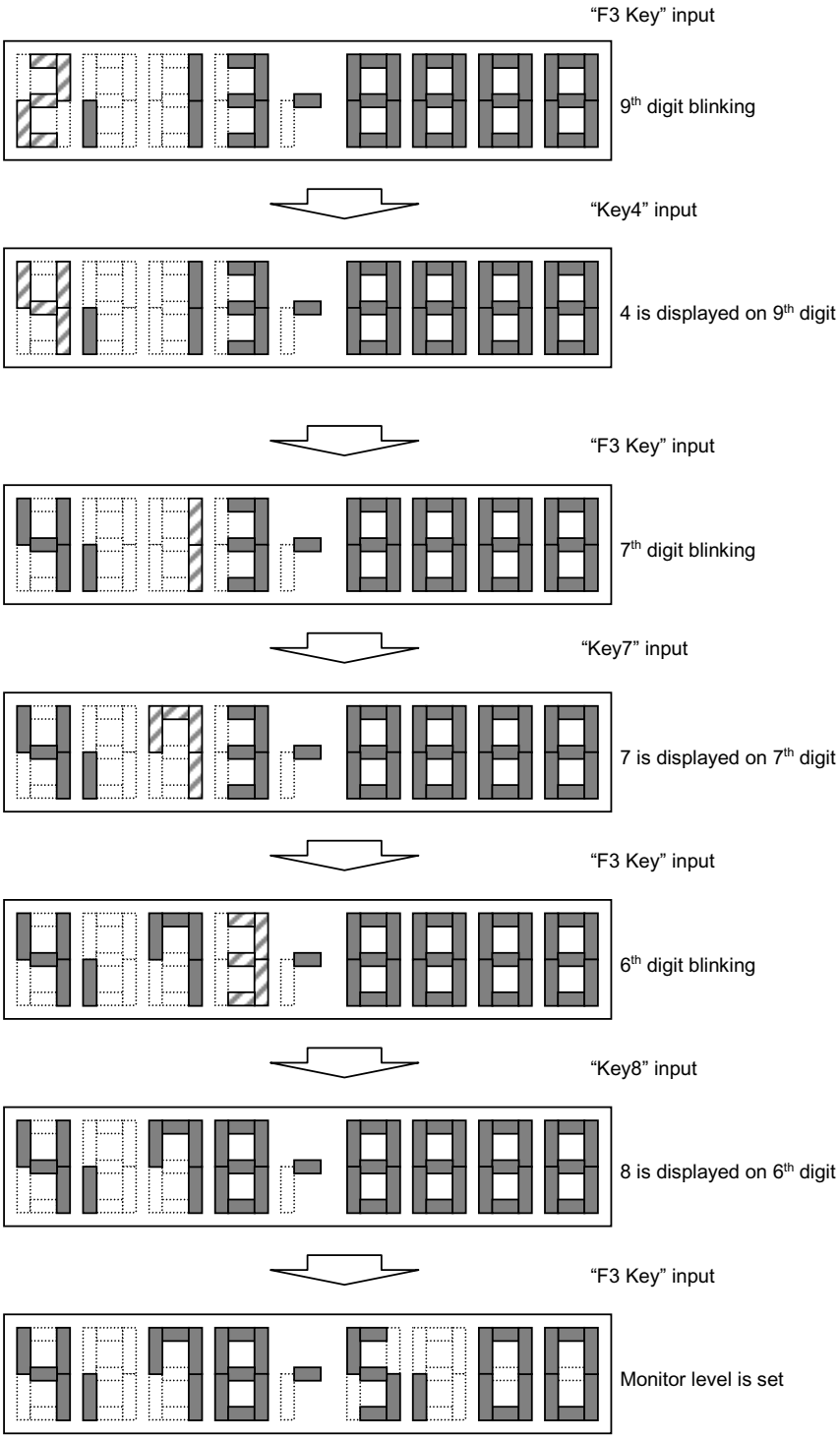


Figure 5.1.5 Example of Setting Monitor Level

5.1.3.3 Voltage Change Monitor Mode

In this mode, changes in the voltage measurement value from analog input are measured. If there is a change of more than fixed amount, a warming is issued.

In the voltage change monitor mode, the voltage AD value of the last sampling is always held. This value is compared with the new sampling value and if a difference is 0.04[V] or more, a buzzer sounds and LED3 blinks as a warning.

LED/LCD display

LED1 and LED3 are "ON" and LED2 and LED 4 are "OFF".

The 6th digit on LCD displays the analog input number currently selected. The 4th digit displays the first digit of a voltage measurement value from analog input, which is followed by up to the second decimal place.

Figure 5.1.6 shows an example of LED/LCD display with Analog Input 1 and a voltage measurement value of 2.96[V].

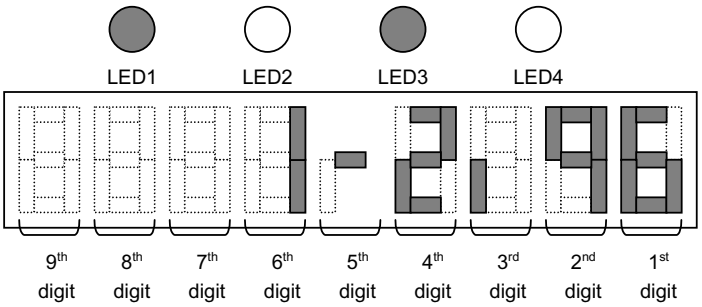


Figure 5.1.6 Example of Display in Voltage Change Monitor Mode

Key operation

"F1 Key" input ends the voltage change monitor mode and the mode changes to the voltage level compare mode.

"F2 Key" input can be used to switch between Analog Input 1 and Analog Input 2. Switching updates the 8the digit on LCD and it displays the number of analog input currently used.

"F4 Key" input can be used to transmit the analog input number currently selected and a 10-bit AD measurement value by using infrared LED. For the transmit format, see "5.1.4 Infrared Transmit Format".

Figure 5.1.7 shows an example of "F2 Key" input.

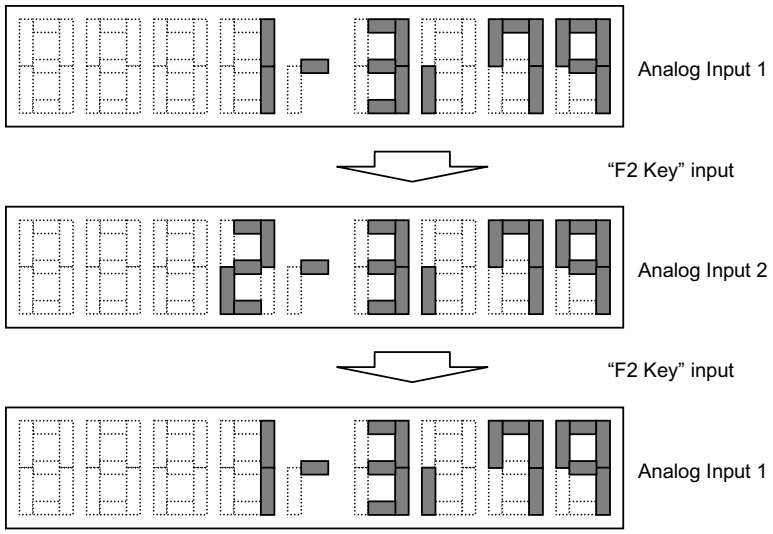


Figure 5.1.7 Example of Switching Input in Voltage Change Monitor Mode

5.1.3.4 Voltage Level Compare Mode

In this mode, a voltage from Analog Input 1 and Analog Input 2 are measured. When measurement values of both inputs are the same, a buzzer sounds and LED4 blinks.

LED/LCD display

In the voltage level compare mode, LED1 and LED4 are "ON" and LED 2 and LED3 are "OFF".

The 9th digit on LCD displays the first digit of a measurement value of Analog Input 1, which is followed by up to the second decimal place.

Figure 5.1.8 shows an example of LEC/LCD display when Analog Input 1 is 3.64[V] and Analog Input 2 is 1.85[V].

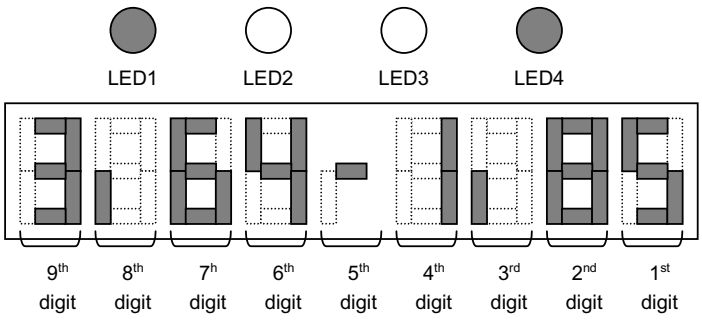


Figure 5.1.8 Example of Display in Voltage Level Compare Mode

Key operation

"F4 Key" input can be used to transmit 10-bit AD measurement values of Analog Input 1 and Analog Input 2 by using infrared LED. For the transmit format, see "5.1.4 Infrared Transmit Format".

"F1 Key" input ends the voltage level compare mode and the mode changes to the voltmeter mode.

5.1.3.5 Power-Saving Mode

This voltmeter enters the power-saving mode when no key operation is made for about one minute. The power-saving mode suspends AD conversion, key input, and LCD/LED display. In this mode, only "STOP Release Key" input is accepted. By pressing "STOP Release Key", the voltmeter is restored to the previous Voltmeter mode and processing is continued.

5.1.4 Infrared Transmit Format

5.1.4.1 Basic Format of Header and Data Sections

Figure 5.1.9 shows the basic format of transmit header and transmit data.

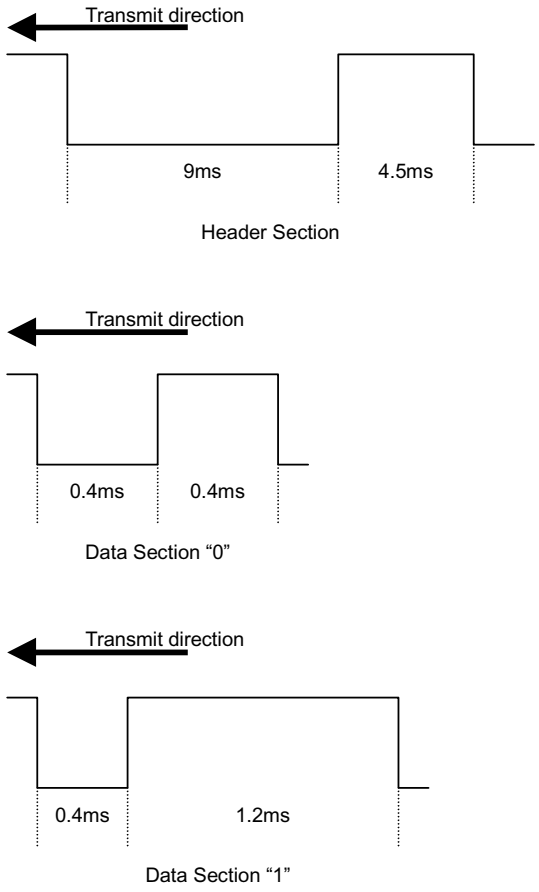


Figure 5.1.9 Infrared Transmit Data Format

In transmitting, the transmit header is firstly transmitted. Then, 6-byte data (3-byte data + 3-byte inverted data) is transmitted according to the infrared transmit data format of each Voltmeter mode.

5.1.4.2 Common Rules of Infrared Transmit Data Format

- Measurement data is transmitted from the upper bit.
- Every1-byte data transmitted is followed by its inverted value. This method enables the receiving end to check if there is any data error.
- "1" is transmitted as a reserved bit.
- 10-bit AD measurement values are transmitted in the original format before being converted to volt units.

5.1.4.3 Infrared Transmit Data Format in Voltmeter Mode

Figure 5.1.10 shows the infrared transmit data format in the voltmeter mode.

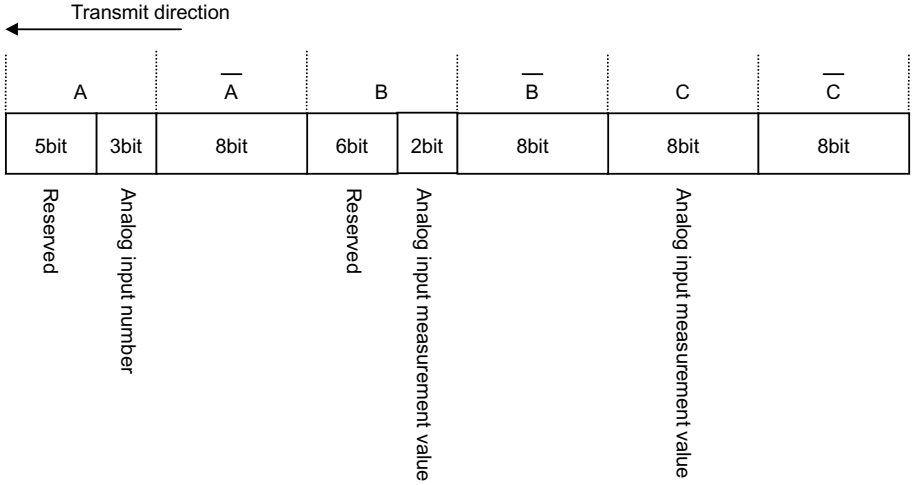


Figure 5.1.10 Infrared Transmit Format in Voltmeter Mode

For the analog input number, "001" is transmitted for Analog Input 1 and "010" is transmitted for Analog Input 2.

5.1.4.4 Infrared Transmit Data Format in Voltage Level Monitor Mode

Figure 5.1.11 shows the infrared transmit data format in the voltage level monitor mode.

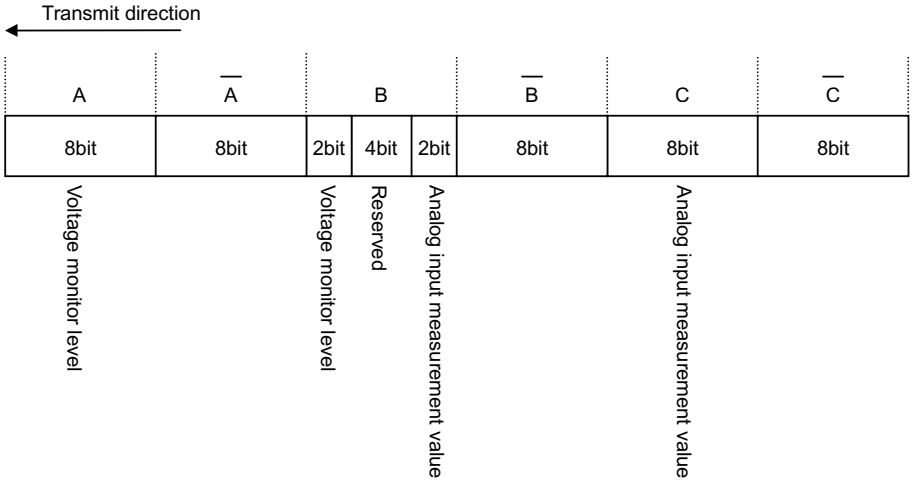


Figure 5.1.11 Infrared Transmit Format in Voltage Level Monitor Mode

For the voltage monitor level, the voltage value that is input at monitor level setting is transmitted after being converted to a 10-bit value. Conversion is performed by dividing the voltage value by 1024 with a reference voltage of 0 to 5V.

The voltage monitor level and measurement data are both transmitted from the upper bit.

5.1.4.5 Infrared Transmit Data Format in Voltage Change Monitor Mode

Figure 5.1.12 shows the infrared transmit data format in the voltage change monitor mode.

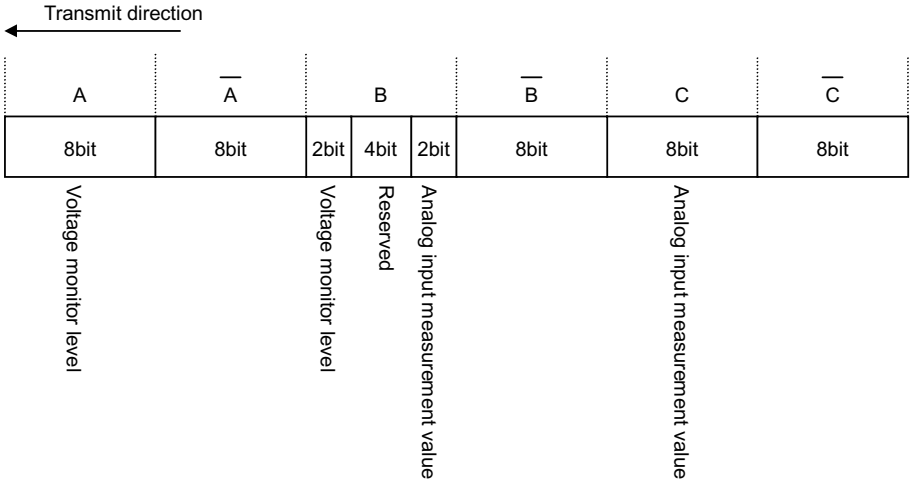


Figure 5.1.12 Infrared Transmit Format in Voltage Change Monitor Mode

For the analog input number, “001” is transmitted for Analog Input 1 and “010” is transmitted for Analog Input 2.

5.1.4.6 Infrared Transmit Data Format in Voltage Level Compare Mode

Figure 5.1.13 shows the infrared transmit data format in the voltage change compare mode.

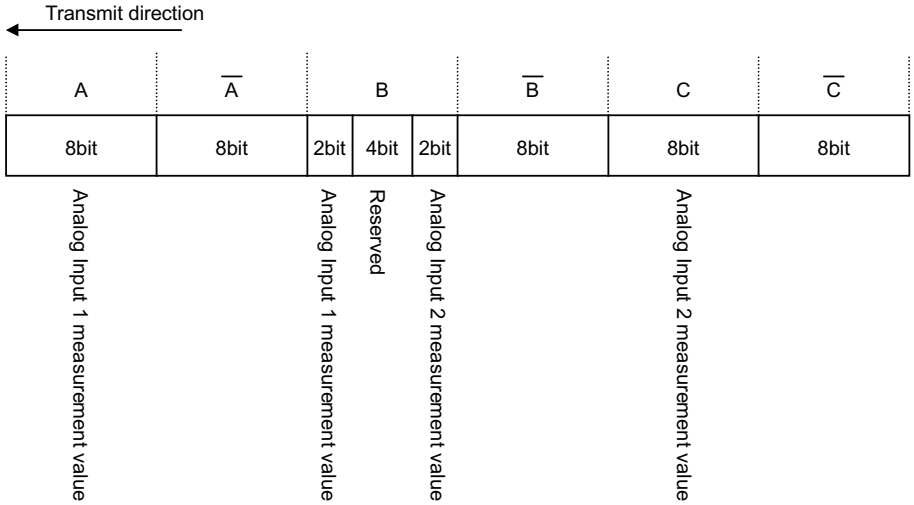


Figure 5.1.13 Infrared Transmit Data Format in Voltage Level Compare Mode

5.2 Test Mode

5.2.1 Overview

5.2.1.1 Operation State in Test Mode

In Test mode, the three types of state are available: “test item setting state”, “test in progress state”, and “test completed state”. The current state of Test mode is displayed by LED.

5.2.1.2 Description of LED Display in Test Mode

LED display indicates the Test mode state in the following manner:

- LED1 off = Test mode
- LED2 on = Test item setting state
- LED3 on = Test in progress state
- LED4 on = Test completed state

Note that the 2nd to 4th digits are all “ON” when the interrupt cycle is shorter than the interrupt processing time and interrupts are continuously generated in the timer counter test, etc. This enables interrupt cycle errors to be detected.

5.2.1.3 LCD Display in Test Mode

Figure 5.2.1 shows the initial display in Test mode.

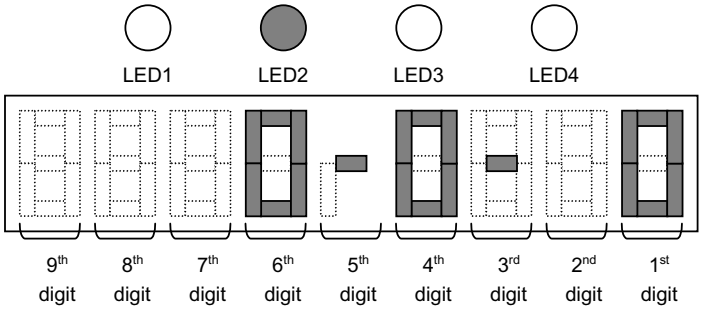


Figure 5.2.1 External View of Test Mode

The 6th and 7th digits on LCD display the test number currently selected.

The 4th digit displays the mode number which shows the operating mode of the selected test.

Table 5.2.1 on the next page shows the test numbers and the test details for each mode number.

Displayed on the 1st and 2nd digits is the setting number for test execution, which enables the register values to be selected and set from predetermined settings when the test specified by the test and mode numbers is executed.

Table 5.2.1 Description of Tests

Test No	Mode No	Description of Test		Output Pin	Input Pin
0	0	TBT test	Time Base Timer	COMMON	—
1	0	WDT test	Interrupt request	COMMON	—
	1		Reset output	RESET	—
2	0	DVO test	DVO	DVO	—
3	0	TC1 test	18bit timer	COMMON	—
	1		18bit event counter	COMMON	ECIN
	2		Pulse width measurement	COMMON, LCD display	ECIN
	3		Frequency measurement	COMMON, LCD display	ECIN, ECNT
4	0	TC3 test	8bit timer	COMMON	—
	1		8bit event counter	COMMON	TC3
	2		8bit PDO	COMMON, TC3	—
	3		8bit PWM	COMMON, TC3	—
5	0	TC4 test	8bit timer	COMMON	—
	1		8bit event counter	COMMON	TC4
	2		8bit PDO	COMMON, TC4	—
	3		8bit PWM	COMMON, TC4	—
6	0	TC3 + 4 test	16bit timer	COMMON	—
	1		16bit event counter	COMMON	TC3
	2		16bit PWM	COMMON,TC4	—
	3		16bit PPG	COMMON,TC4	—
7	0	TC5 test	8bit timer	COMMON	—
8	0	TC6 test	8bit timer	COMMON	—
	1		8bit event counter	COMMON	TC6
	2		8bit PDO	COMMON, TC6	—
	3		8bit PWM	COMMON,TC6	—
9	0	TC5 + 6 test	16bit timer	COMMON	—
	1		16bit PWM	COMMON, TC6	—
	2		16bit PPG	COMMON,TC6	—
10	0	UART test	Tx	TxD, LCD display	—
	1		Rx	LCD display	RxD
11	0	SIO test	SIO Tx	SO, SCK, LCD display	SCK
	1		SIO Rx	SCK, LCD display	SI, SCK
	2		SIO TxRx	SO, SCK, LCD display	SI, SCK
12	0	ADC test	Single mode	COMMON, LCD display	AIN0
	1		Repeat mode	COMMON, LCD display	AIN0
13	0	LCD test	LCD operation check test	LCD display	—
14	0	Continuous test	Continuous test	COMMON, DVO, TC3, TC4, TC6, TxD, SO, SCK, LCD display	ECIN, ECNT, TC3, TC4, TC6, RxD, SCK, SI, AIN0

5.2.1.4 Key Input in Test Mode

In Test mode, "F1 Key" input is used to select the test number. Each time "F1 Key" is pressed, the test number on the 6th and 7th digits is incremented. The display number reaches 14, then it returns to 0.

"F2 Key" input is used to select the mode number. The mode number is selected on the 4th digit in the same manner as the test number and each test number has its own range of numbers to choose from.

The setting number can be assigned for 16 settings (0 to 15) according to the combination of test number and mode number. The setting number can be set by using "Key 0 to Key F" and the specified number (0 to 15) is displayed on the 1st and 2nd digits on LCD.

"F3 Key" input sets each register value according to the selected test details and executes an operation test. When it is necessary to display register values to check operation results as in the case of pulse width measurement, frequency measurement, and serial transmit/receive, the test completed state is entered after each measurement or serial transmit/receive is completed. At this time, data is displayed on LCD so that operation can be checked.

For tests that include the test completed state, data displayed on LCD can be switched with "F4 Key" input after test completion.

While tests are executed, only "INT0 Interrupt Key" is accepted. When "INT0 Interrupt Key" is pressed during test execution, the test is immediately stopped and the test item setting state is entered.

When "INT0 Interrupt Key" is pressed for more than 3 seconds, 'Int0 Err' is displayed on LCD and the test is stopped. In this case, press "Reset Key" and execute the test again.

5.2.2 Transition of Test Mode State

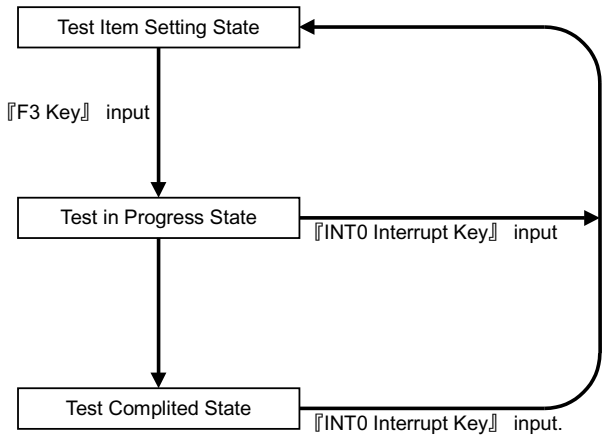


Figure 5.2.2 Transition of Test Mode State

5.2.3 Specifications of Test Mode Test Items

5.2.3.1 Time Base Timer Test [Test number: 0]

In the Time Base Timer (TBT) test, TBT interrupts are generated and COMMON pin outputs are inverted in interrupt processing. By monitoring the COMMON pin, the interrupt cycle can be measured to check whether the TBT is operating according to the setting.

The test number of TBT test is 0. No mode selection is performed.

In the TBT test, each setting pattern specifies the operating mode (SYSCR2, NORMAL/SLOW), high-/low-frequency selection (DV7CK), and TBT interrupt frequency (TBTCR).

Table 5.2.2 shows the register set values for each setting pattern.

Table 5.2.2 Register Set Values for TBT Test

Setting No	Operating Mode (SYSCR2)	Selected Output Frequency (TBTCR)	TBT Interrupt Cycle
0	NORMAL (0xC0)	(0x08)	1.047s
1		(0x09)	262ms
2		(0x0A)	8.19ms
3		(0x0B)	2.04ms
4		(0x0C)	1.023ms
5		(0x0D)	512μs
6		(0x0E)	256μs
7		(0x0F)	64ms
8		(0x1A)	7.81ms
9		(0x1B)	1.95ms
10		(0x1C)	977μs
11		(0x1D)	488μs
12		(0x1E)	244μs
13		(0x1F)	64μs
14	SLOW (0xE0)	(0x08)	1s
15		(0x09)	250ms

5.2.3.2 Watchdog Timer Test [Test number: 1]

The watchdog timer (WDT) test has the following two modes:

- WDT Output－Interrupt Request Mode
  WDT interrupts are generated and the COMMON pin is inverted in WDT interrupt processing. By monitoring the COMMON pin, the WDT interrupt cycle is measured to check whether the WDT is operating according to the setting.
- WDT Output－ Reset Output Mode
  After the WDT test is started, not clearing the WDT counter activates the WDT and resets internal hardware. By measuring the time between test start and reset operation, whether operation is performed according to the setting can be checked.

The test number of WDT test is 1. Table 5.2.3 shows the mode numbers and setting items of WDT test.

Table 5.2.3 Modes and Setting Items of WDT Test

Mode Name	Mode No	Setting Item
Interrupt request	0	Operating mode, High-/Low-frequency selection, Watchdog timer detecting time
Reset output	1	Operating mode, High-/Low-frequency selection, Watchdog timer detecting time

Table 5.2.4 and Table 5.2.5 show the register set values for each setting pattern.

Table 5.2.4 Register Set Values for WDT Reset Output

Setting No	Operating Mode (SYSCR2)		High-/Low-Frequency Selection (TBTCR)	(WDTCR1)	WDT Reset Cycle
0	NORMAL(0xC0)		fc (0x00)	(0x08)	4.194s
1				(0x0A)	1.049s
2				(0x0C)	262ms
3				(0x0E)	65.5ms
4			fs (0x10)	(0x08)	4s
5				(0x0A)	1s
6				(0x0C)	250ms
7				(0x0E)	62.5ms
8	SLOW(0xE0)		fc (0x00)	(0x08)	4s
9				(0x0A)	1s
10				(0x0C)	250ms
11				(0x0E)	62.5ms
12	For continuous test	NORMAL (0xC0)	fc (0x00)	(0x0A)	1.049s
13					
14					
15					

Table 5.2.5 Register Set Values for WDT Interrupt Request

Setting No	Operating Mode (SYSCR2)		High-/Low-Frequency Selection (TBTCR)	(WDTCR1)	WDT Reset Cycle
0	NORMAL(0xC0)		fc (0x00)	(0x08)	4.194s
1				(0x0A)	1.049s
2				(0x0C)	262ms
3				(0x0E)	65.5ms
4			fs (0x10)	(0x08)	4s
5				(0x0A)	1s
6				(0x0C)	250ms
7				(0x0E)	62.5ms
8	SLOW(0xE0)		fc (0x00)	(0x08)	4s
9				(0x0A)	1s
10				(0x0C)	250ms
11				(0x0E)	62.5ms
12	For continuous test	NORMAL (0xC0)	fc (0x00)	(0x0A)	1.049s
13					
14					
15					

5.2.3.3 Divider Output Test [Test number: 2]

In the divider output test, duty-50% pulses are output from the DVO pin. By monitoring the DVO pin, whether the divider output is operating according to the setting can be checked.

The test number of divider output test is 2. No mode selection is performed.

In this test, each setting pattern specifies the operating mode (SYSCR2, NORMAL/SLOW), high-/low-frequency selection (DV7CK), and DVO output frequency.

Table 5.2.6 shows the register set values for the divider output test.

Table 5.2.6 Register Set Values for Divider Output Test

Setting No	Operating Mode (SYSCR2)		Output Frequency Selection (TBTCR)	Divider Output Frequency/Cycle
0	NORMAL(0xC0)		976.5Hz (0x80)	1.024ms
1			1.953KHz (0xA0)	512µs
2			3.9065KHz (0xC0)	256µs
3			7.8125KHz (0xE0)	128µs
4			1.024KHz (0x90)	977µs
5			2.048KHz (0xB0)	488µs
6			4.096KHz (0xD0)	244µs
7			8.192KHz (0xF0)	122µs
8	SLOW(0xE0)		1.024KHz (0x80)	977µs
9			2.048KHz (0xA0)	488µs
10			4.096KHz (0xC0)	244µs
11			8.192KHz (0xE0)	122µs
12	For continuous test	NORMAL (0xC0)	976.5Hz (0x80)	1.024ms
13				
14				
15				

5.2.3.4 TC1 Test [Test number: 3]

The timer counter 1 (TC1) test has the following four modes:

- 18-bit Timer Mode
  By activating the 18-bit timer, TC1 interrupts are generated and COMMON pin outputs are inverted in TC1 interrupt processing. By monitoring the COMMON pin, the TC1 interrupt cycle can be measured to check whether the TC1 18-bit timer counter is operating according to the setting.
- Event Counter Mode
  By using the counter by input pulses from the ECIN pin, TC1 interrupts are generated and COMMON pin outputs are inverted in TC1 interrupt processing. By monitoring the COMMON pin, the TC1 interrupt cycle can be measured to check whether the TC1 event counter is operating according to the setting.

- Pulse Width Measurement Mode
  By input pulse width measurements from the ECIN pin, TC1 interrupts are generated and COMMON pin outputs are inverted in TC1 interrupt processing. By displaying on LCD the pulse width measurement value of pulses input from the ECIN pin, whether TC1 pulse width measurement is operating according to the setting can be checked.
- Frequency Measurement Mode
  By input pulse frequency measurements from the ECIN pin, TC1 interrupts are generated and COMMON pin outputs are inverted in TC1 interrupt processing. By displaying on LCD the frequency measurement value of pulses input from the ECIN pin, whether TC1 frequency measurement is operating according to the setting can be checked.

The test number of TC1 test is 3. Table 5.2.7 shows the mode numbers and setting items of TC1 test.

Table 5.2.7 Modes and Setting Items of TC1 Test

Mode Name	Mode No	Setting Item
TC1 18bit Timer	0	Operating mode, High-/Low-frequency selection, TREG1A、TC1 source clock
TC1 Event Counter	1	Operating mode, TREG1A
TC1 Pulse Width Measurement	2	Operating mode, High-/Low-frequency selection, Window gate pulse interrupt edge
TC1 Frequency Measurement	3	High-/Low-frequency selection, ECIN edge selection, Window gate pulse selection, Window gate pulse interrupt edge, Internal window gate pulse set register, TC6 operation clock, TC6 operating mode, TTREG6, PWREG6

In the TC1 pulse width measurement and TC1 frequency measurement modes, the test completed state is entered after measurement is performed three times. LCD displays the TREG1A value, which is the measurement result.

The display number (1 to 3) indicates the number of measurements and selected by "F4 Key" input.

If an overflow error occurs during a test, the 6th digit displays "E". In this case, change the set value and perform measurement again.

By pressing "INT0 Interrupt Key" in the test completed state, the state returns to the test item setting state.

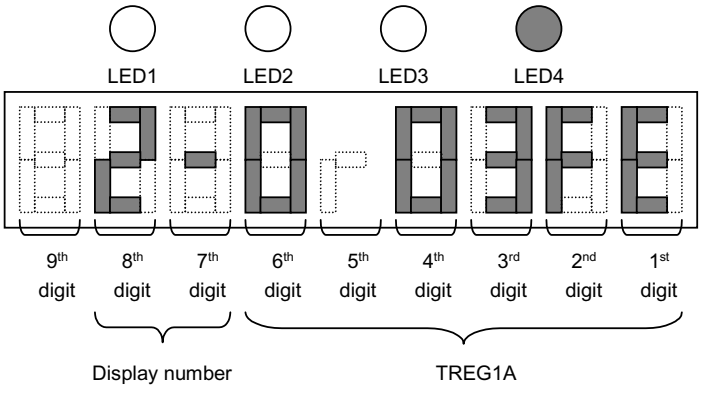


Figure 5.2.3 TC1 Test Result Display

Table 5.2.8 to Table 5.2.11 show the register set values for each setting pattern.

Table 5.2.8 Register Set Values for TC1 18-bit Timer

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC1CR1)	(TREG1A)	TC1 Interrupt Cycle
0	NORMAL(0xC0)	fc (0x00)	$fc/2^3$(0x58)	(0x0001F4)	500μs
1				(0x00C350)	50ms
2				(0x0186A0)	100ms
3				(0x00000A)	10μs(*)
4			$fc/2^7$(0x54)	(0x000019)	400μs
5			$fc/2^{11}$(0x50)	(0x000028)	10.24ms
6			$fc/2^{13}$(0x4C)	(0x00000A)	10.24ms
7			$fc/2^{23}$(0x48)	(0x000002)	2.096s
8			fs(0x44)	(0x000020)	976μs
9		fs (0x10)	$fs/2^3$(0x50)	(0x000029)	10ms
10			$fs/2^5$(0x4C)	(0x000033)	49.776ms
11			$fs/2^{15}$(0x48)	(0x000002)	2s
12	SLOW(0xE0)	fc (0x00)	$fs/2^3$(0x50)	(0x000052)	20ms
13			$fs/2^5$(0x4C)	(0x000033)	49.776ms
14			$fs/2^{15}$(0x48)	(0x000002)	2s
15			fc(0x40)	(0x027100)	20ms

* In this setting, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the setting.

Table 5.2.9 Register Set Values for TC1 18-bit Event Counter

Setting No	Operating Mode (SYSCR2)	(TC1CR1)	(TREG1A)
0	NORMAL(0xC0)	(0x5C)	(0x03FFFF)
1			(0x010000)
2			(0x00FFFF)
3			(0x00F000)
4			(0x000F00)
5			(0x0000FF)
6			(0x00000F)
7			(0x000001)
8	SLOW(0xE0)		(0x03FFFF)
9			(0x010000)
10			(0x00FFFF)
11			(0x00F000)
12			(0x000F00)
13			(0x0000FF)
14			(0x00000F)
15			(0x000001)

Table 5.2.10 Register Settings for TC1 Pulse Width Measurement

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC1CR1)	Interrupt Edge (TC1CR2)	Internal Clock
0	NORMAL(0xC0)	fc (0x00)	fc(0x42)	rising edge (0x00)	8MHz
1				both edges (0x10)	
2			fs(0x46)	falling edge (0x00)	32.768KHz
3			$fc/2^{23}$(0x4A)		0.953Hz
4			$fc/2^{13}$(0x4E)		976.56Hz
5			$fc/2^{11}$(0x52)		3.906KHz
6			$fc/2^{7}$(0x56)		62.5KHz
7			$fc/2^{3}$(0x5A)		4.096KHz
8		fs (0x00)	$fs/2^{15}$(0x4A)		1Hz
9				both edges (0x10)	
10			$fs/2^{5}$(0x4E)	falling edge (0x00)	1.024KHz
11			$fs/2^{3}$(0x52)		4.096KHz
12	SLOW(0xE0)	fc (0x00)	$fs/2^{15}$(0x4A)		1Hz
13				both edges (0x10)	
14			$fs/2^{5}$(0x4E)	falling edge (0x00)	1.024KHz
15			$fs/2^{3}$(0x52)		4.096KHz

Table 5.2.11 Register Settings for TC1 Frequency Measurement

Setting No	Operating Mode (SYSCR2)	(TC1CR1)	(TC1CR2)				(TREG1B)	(TC6CR)	(TTREG6)	(PWREG6)
				SEG	SEGDG	WGP				
0	NORMAL(0xC0)	(0x5F)	(0x00)	falling	falling	ECNT	(0x00)	(0x00)	(0x00)	(0x00)
1			(0x90)	both	both					
2			(0x10)	falling	both					
3			(0x80)	both	falling					
4			(0x20)	falling	falling	2^{12}/fc	(0xFF)			
5			(0xB0)	both	both	2^{12}/fc				
6			(0x34)	falling	both	2^{13}/fc				
7			(0xA8)	both	falling	2^{14}/fc				
8			(0x22)	falling	falling	TC6	(0x00)	(0x09)	(0xFF)	(0x00)
9			(0xD2)	both	both			(0xB9)	(0xFF)	(0x00)
10			(0x52)	falling	both			(0x19)	(0xFF)	(0x00)
11			(0xC2)	both	falling			(0x2A)	(0x00)	(0xFF)
12	SLOW(0xE0)		(0x00)	falling	falling	ECNT	(0x00)	(0x00)	(0x00)	(0x00)
13			(0x90)	both	both		(0xFF)	(0x00)		
14			(0x34)	falling	both	2^{5}/fs	(0xFF)	(0x00)		
15			(0xC2)	both	falling	TC6	(0x00)	(0x09)	(0xFF)	(0x00)

5.2.3.5 TC3 Test [Test number: 4]

The TC3 test has the following four modes:

- 8-bit Timer Mode
  The 8-bit timer is activated and COMMON pin outputs are inverted in TC3 interrupt processing. By monitoring the COMMON pin, the TC3 interrupt cycle can be measured to check whether the TC3 8-bit timer mode is operating according to the setting.
- 8-bit Event Counter Mode
  By using the counter by input pulses from the ECIN pin, TC3 interrupts are generated and COMMON pin outputs are inverted in TC3 interrupt processing. By monitoring the COMMON pin, the TC3 interrupt cycle can be measured to check whether the TC3 event counter mode is operating according to the setting.

- 8-bit PDO Mode
  8-bit PDO is output to the TC3 pin and COMMON pin outputs are inverted in TC3 interrupt processing. By monitoring signals output from the COMMON and TC3 pins, whether the TC3 interrupt cycle and PDO output are operating according to the setting can be checked.
- 8-bit PWM Mode
  8-bit PWM is output to the TC3 pin and COMMON pin outputs are inverted in TC3 interrupt processing. By monitoring signals output from the COMMON and C3 pins, whether the TC3 interrupt cycle and PWM output are operating according to the setting can be checked.

The test number of TC3 test is 4. Table 5.2.12 shows the mode numbers and setting items of TC3 test.

Table 5.2.12 Modes and Setting Items of TC3 Test

Mode Name	Mode No	Setting Item
8bit Timer	0	Operating mode, High-/Low-frequency selection, TTREG3, TC3 source clock
8bit Event Counter	1	TTREG3
8bit PDO	2	Operating mode, High-/Low-frequency selection, TTREG3, TC3 source clock, TTF
8bit PWM	3	Operating mode, High-/Low-frequency selection, TTREG3, TC3 source clock, TTF

Table 5.2.13 to Table 5.2.16 show the register set values for each setting pattern.

Table 5.2.13 Register Setting for TC3 8-bit Timer

Setting Item	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC3CR)	(TTREG3)	TC3 Interrupt Cycle
0	NORMAL(0xC0)	fc (0x00)	$fc/2^{11}$(0x08)	(0x04)	1.024ms
1				(0xC8)	51.2ms
2			$fc/2^{7}$(0x18)	(0x19)	400μs
3				(0x3F)	1.0008ms
4			$fc/2^{5}$(0x28)	(0x0E)	60μs
5				(0x32)	200μs
6			$fc/2^{3}$(0x38)	(0x01)	1μs(*)
7				(0x05)	5μs(*)
8				(0x32)	50μs
9				(0x64)	100μs
10				(0xC8)	200μs
11				(0xFF)	255μs
12		fs (0x10)	$fs/2^{3}$(0x08)	(0x01)	244μs
13				(0x29)	10.004ms
14	SLOW(0xE0)	fc (0x00)	$fs/2^{3}$(0x08)	(0x01)	244μs(*)
15				(0x29)	10.004ms

* In these settings, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the setting.

Table 5.2.14 Register Settings for TC3 8-bit Event Counter

Setting No	Operating Mode (SYSCR2)	(TC3CR)	(TTREG3)
0	NORMAL(0xC0)	(0x78)	(0xFF)
1			(0x7F)
2			(0x3F)
3			(0x1F)
4			(0x0F)
5			(0x08)
6			(0x02)
7			(0x01)
8	SLOW(0xE0)		(0xFF)
9			(0x7F)
10			(0x3F)
11			(0x1F)
12			(0x0F)
13			(0x08)
14			(0x02)
15			(0x01)

Table 5.2.15 Register Settings for TC3 8-bit PDO Mode

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC3CR)			(TTREG3)	Inversion interval
				Frequency	TFF		
0	NORMAL(0xC0)	fc (0x00)	(0x09)	$fc/2^{11}$	CLR	(0x04)	1.024ms
1			(0x89)		SET		
2			(0x09)		CLR	(0x28)	10.24ms
3						(0x64)	25.6ms
4						(0xC8)	51.2ms
5			(0x19)	$fc/2^{7}$		(0x3F)	1ms
6						(0xFA)	4ms
7			(0x29)	$fc/2^{5}$		(0x05)	20μs(*)
8						(0x32)	200μs
9			(0x39)	$fc/2^{3}$		(0x02)	2μs(*)
10						(0xC8)	200μs
11		fs (0x10)	(0x09)	$fs/2^{3}$		(0x29)	10ms
12						(0xCD)	50ms
13	SLOW(0xE0)	fc (0x00)	(0x09)			(0x29)	10ms
14			(0x89)		SET		
15			(0x09)		CLR	(0xCD)	50ms

* In these settings, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the setting.

Table 5.2.16 Register Settings for TC3 8-bit PWM

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	(TC3CR)			(PWREG3)	Inversion Interval
				fc	TTF		
0	NORMAL(0xC0)	fc (0x00)	(0x0A)	$fc/2^{11}$	CLR	(0x40)	16.38ms
1			(0x8A)		SET		
2			(0x2A)	$fc/2^{5}$	CLR		256μs
3			(0xAA)		SET		
4			(0x5A)	$fc/^{2}$	CLR		16μs(*)
5			(0xDA)		SET		
6			(0x4A)	fs	CLR		1.95ms
7			(0xCA)		SET		
8			(0x6A)	fc	CLR		8μs(*)
9			(0xEA)		SET		
10		fs (0x10)	(0x0A)	$fs/2^{3}$	CLR		15.616ms
11			(0x8A)		SET		
12	SLOW(0xE0)	fc (0x00)	(0x0A)	$fs/2^{3}$	CLR		
13			(0x8A)		SET		
14			(0x4A)	fs	CLR		1.95ms
15			(0xCA)		SET		

* In these settings, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the settng.

5.2.3.6 TC4 Test [Test number: 5]

The TC4 test has the following four modes:

- 8-bit Timer Mode
  The 8-bit timer is activated and COMMON pin outputs are inverted in TC4 interrupt processing. By monitoring the COMMON pin, the TC4 interrupt cycle can be measured to check whether the TC4 8-bit timer mode is operating according to the setting.
- 8-bit Event Counter Mode
  By using the counter by input pulses from the ECIN pin, TC4 interrupts are generated and COMMON pin outputs are inverted in TC4 interrupt processing. By monitoring the COMMON pin, the TC4 interrupt cycle can be measured to check whether the TC4 event counter mode is operating according to the setting.
- 8-bit PDO Mode
  8-bit PDO is output to the TC4 pin and COMMON pin outputs are inverted in TC4 interrupt processing. By monitoring signals output from the COMMON and TC4 pins, whether the TC4 interrupt cycle and PDO output are operating according to the setting can be checked.
- 8-bit PWM Mode
  8-bitPWM is output to the TC4 pin and COMMON pin outputs are inverted in TC4 interrupt processing. By monitoring signals output from the COMMON and C4 pins, whether the TC4 interrupt cycle and PWM output are operating according to the setting can be checked.

The test number of TC4 test is 5. Table 5.2.17 shows the mode numbers and setting items of TC4 test.

Table 5.2.17 Modes and Setting Items of TC4 Test

Mode Name	Mode No	Setting Item
8bit Timer	0	Operating mode, High-/Low-frequency selection, TTREG4, TC4 source clock
8bit Event Counter	1	Operating mode, TTREG4
8bit PDO	2	Operating mode, High-/Low-frequency selection, TTREG4, TC4 source clock, TTF
8bit PWM	3	Operating mode, High-/Low-frequency selection, TREG4, TC4 source clock, TTF

Table 5.2.18 to Table 5.2.21 show the register set values for each setting pattern.

Table 5.2.18 Register Set Values for TC4 8-bit Timer

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC4CR)	(TTREG4)	TC4 Interrupt Cycle
0	NORMAL(0xC0)	fc (0x00)	$fc/2^{11}$(0x08)	(0x04)	1.024ms
1				(0xC8)	51.2ms
2			$fc/2^{7}$(0x18)	(0x19)	400μs
3				(0x3F)	1.0008ms
4			$fc/2^{5}$(0x28)	(0x0E)	60μs
5				(0x32)	200μs
6			$fc/2^{3}$(0x38)	(0x01)	1μs(*)
7				(0x05)	5μs(*)
8				(0x32)	50μs
9				(0x64)	100μs
10				(0xC8)	200μs
11				(0xFF)	255μs
12		fs (0x10)	$fs/2^{3}$(0x08)	(0x01)	244μs
13				(0x29)	10.004ms
14	SLOW(0xE0)	fc (0x00)	$fs/2^{3}$(0x08)	(0x01)	244μs(*)
15				(0x29)	10.004ms

* In these settings, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not geneated acording to the setting.

Table 5.2.19 Register Settings for TC4 8-bit Event Counter

Setting No	Operating Mode (SYSCR2)	(TC4CR)	(TTREG4)
0	NORMAL(0xC0)	(0x78)	(0xFF)
1			(0x7F)
2			(0x3F)
3			(0x1F)
4			(0x0F)
5			(0x08)
6			(0x02)
7			(0x01)
8	SLOW(0xE0)		(0xFF)
9			(0x7F)
10			(0x3F)
11			(0x1F)
12			(0x0F)
13			(0x08)
14			(0x02)
15			(0x01)

Table 5.2.20 Register Settings for TC4 8-bit PDO Mode

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC4CR)			(TTREG4)	Inversion Interval
				Frequency	TFF		
0	NORMAL(0xC0)	fc (0x00)	(0x09)	$fc/2^{11}$	CLR	(0x04)	1.024ms
1			(0x89)		SET		
2			(0x09)		CLR	(0x28)	10.24ms
3						(0x64)	25.6ms
4						(0xC8)	51.2ms
5			(0x19)	$fc/2^{7}$		(0x3F)	1ms
6						(0xFA)	4ms
7			(0x29)	$fc/2^{5}$		(0x05)	20μs(*)
8						(0x32)	200μs
9			(0x39)	$fc/2^{3}$		(0x02)	2μs(*)
10						(0xC8)	200μs
11		fs (0x10)	(0x09)	$fs/2^{3}$		(0x29)	10ms
12						(0xCD)	50ms
13	SLOW(0xE0)	fc (0x00)	(0x09)			(0x29)	10ms
14			(0x89)		SET		
15			(0x09)		CLR	(0xCD)	50ms

* In these settings, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the seting.

Table 5.2.21 Register Settings for TC4 8-bit PWM

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	(TC4CR)			(PWREG4)	Inversion Interval
				fc	TTF		
0	NORMAL(0xC0)	fc (0x00)	(0x0A)	$fc/2^{11}$	CLR	(0x40)	16.38ms
1			(0x8A)		SET		
2			(0x2A)	$fc/2^{5}$	CLR		256μs
3			(0xAA)		SET		
4			(0x5A)	$fc/^{2}$	CLR		16μs(*)
5			(0xDA)		SET		
6			(0x4A)	fs	CLR		1.95ms
7			(0xCA)		SET		
8			(0x6A)	fc	CLR		8μs(*)
9			(0xEA)		SET		
10		fs (0x10)	(0x0A)	$fs/2^{3}$	CLR		15.616ms
11			(0x8A)		SET		
12	SLOW(0xE0)	fc (0x00)	(0x0A)	$fs/2^{3}$	CLR		
13			(0x8A)		SET		
14			(0x4A)	fs	CLR		1.95ms
15			(0xCA)		SET		

* In these settings, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the seting.

5.2.3.7 16-bit TC3 + 4 Test [Test number: 6]

The 16-bit TC3 + 4 test has the following four modes:

- 16-bit Timer Mode
  The 16-bit timer is activated and COMMON pin outputs are inverted in TC4 interrupt processing. By monitoring the COMMON pin, the TC4 interrupt cycle can be measured to check whether the 16-bit timer mode is operating according to the setting.
- 16-bit Event Counter Mode
  By using the counter by input pulses from the ECIN pin, TC4 interrupts are generated and COMMON pin outputs are inverted in TC4 interrupt processing. By monitoring the COMMON pin, the TC4 interrupt cycle can be measured to check whether the 16-bit event counter mode is operating according to the setting.
- 16-bit PWM Mode
  16-bit PWM is output to the TC4 pin and COMMON pin outputs are inverted in TC4 interrupt processing. By monitoring signals output from the COMMON and TC4 pins, the TC4 interrupt cycle and PWM output can be measured to check whether the 16-bit PWM mode is operating according to the setting.
- 16-bit PPG Mode
  16-bit PPG is output to the TC4 pin and COMMON pin outputs are inverted in TC4 interrupt processing. By monitoring signals output from the COMMON and TC4 pins, the TC4 interrupt cycle and PPG output can be measured to check whether the 16-bit PPG mode is operating according to the setting.

The test number of 16-bit TC3 + 4 test is 6. Table 5.2.22 shows the mode numbers and setting items of 16-bit TC3 + 4 test.

Table 5.2.22 Modes and Setting Items of 16-bit TC3 + 4 Test

Mode Name	Mode No	Setting Item
16-bit Timer Mode	0	Operating mode, High-/Low-frequency selection, TTREG3, TTREG4, TC4 source clock
16-bit Event Counter Mode	1	Operating mode, TTREG3, TTREG4
16-bit PDO Mode	2	Operating mode, High-/Low-frequency selection, PWREG3, PWREG4, TC4 source clock, TTF
16-bit PPG Mode	3	Operating mode, High-/Low-frequency selection, TTREG3, TTREG4, PWREG3, PWREG4, TC4 source clock, TTF

Table 5.2.23 to Table 5.2.26 show the register set values for each setting pattern.

Table 5.2.23 Register Set Values for TC3 + 4 16-bit Timer

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC3CR)	(TC4CR)	(TTREG34)	TC34 Interrupt Cycle
0	NORMAL(0xC0)	fc (0x00)	$fc/2^{11}$(0x08)	(0x0C)	(0x0001)	256μs
1					(0x0F42)	1s
2			$fc/2^{7}$(0x18)		(0x0001)	16μs
3					(0xF424)	1s
4			$fc/2^{5}$(0x28)		(0x0005)	20μs
5					(0xC350)	200ms
6			$fc/2^{3}$(0x38)		(0x0100)	1μs(*)
7					(0x0014)	20μs
8					(0x0064)	100μs
9					(0x03E8)	1ms
10					(0x2710)	10ms
11					(0xC350)	50ms
12		fs (0x10)	$fs/2^{3}$(0x08)		(0x0001)	244μs
13					(0x1002)	1s
14	SLOW(0xE0)	fc (0x00)			(0x0001)	244μs(*)
15					(0x1002)	1s

* In these settngs, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not genrated according to the setting.

Table 5.2.24 Register Set Values for TC3 + 4 16-bit Event Counter

Setting No	Operating Mode (SYSCR2)	(TC3CR)	(TC4CR)	(TTREG34)
0	NORMAL(0xC0)	(0x78)	(0x0C)	(0xFFFF)
1				(0x7FFF)
2				(0x3FFF)
3				(0x1FFF)
4				(0x0FFF)
5				(0x07FF)
6				(0x03FF)
7				(0x01FF)
8				(0x00FF)
9				(0x007F)
10				(0x001F)
11				(0x000F)
12				(0x0002)
13	SLOW(0xE0)			(0xFFFF)
14				(0x7FFF)
15				(0x00FF)

Table 5.2.25 Register Set Values for TC3 + 4 16-bit PWM

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC3CR)	TTF (TC4CR)	(TTREG 34)	Inversion Interval
0	NORMAL(0xC0)	fc (0x00)	$fc/2^{11}$(0x0B)	CLR(0x0E)	(0x4000)	4.19s
1			$fc/2^{7}$(0x1B)			262.144ms
2			$fc/2^{5}$(0x2B)			65.536ms
3			$fc/2^{3}$(0x3B)			16.384ms
4				SET(0x8E)		
5				CLR(0x0E)	(0x2000)	8.191ms
6					(0x1000)	4.0955ms
7					(0x0800)	2.04775ms
8					(0x0400)	1.023875ms
9					(0x0200)	511.9375μs
10			fs(0x4B)		(0x4000)	499.712ms
11			fc/2(0x5B)			4.096ms
12			fc(0x6B)			2.048ms
13		fs (0x10)	$fs/2^{3}$(0x0B)			3.997696s
14	SLOW(0xE0)	fc (0x00)	$fs/2^{3}$(0x0B)			3.997696s
15			fs(0x4B)			499.712ms

Table 5.2.26 Register Set Values for TC3 + 4 16-bit PWM

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC3CR)	TFF (TC4CR)	(TTREG 34)	(PWREG 34)	Inversion Interval	Interrupt Cycle
0	NORMAL (0xC0)	fc (0x00)	$fc/2^{11}$(0x0B)	CLR(0x0F)	(0x0640)	(0x0190)	100ms	400ms
1				SET(0x8F)				
2			$fc/2^{7}$(0x1B)	CLR(0x0F)	(0x09c4)	(0x0271)	10ms	40ms
3				SET(0x8F)				
4			$fc/2^{5}$(0x2B)	CLR(0x0F)	(0x2710)	(0x09C4)	10ms	40ms
5				SET(0x8F)				
6			$fc/2^{3}$(0x3B)	CLR(0x0F)	(0x9C40)	(0x2710)	10ms	40ms
7				SET(0x8F)				
8				CLR(0x0F)		(0x1388)	5ms	40ms
9				SET(0x8F)	(0x4E20)	(0x2710)	10ms	20ms
10				CLR(0x0F)	(0x0014)	(0x000A)	10μs	20μs
11				SET(0x8F)	(0x0005)	(0x0001)	1μs(*)	5μs
12		fs (0x10)	$fs/2^{3}$(0x0B)	CLR(0x0F)	(0x0668)	(0x019A)	100ms	400ms
13				SET(0x8F)				
14	SLOW (0xE0)	fc (0x00)		CLR(0x0F)				
15				SET(0x8F)				

* Because the inversion interval is short, inversion waveforms may not be output properly. Also, interrupts may not be generated according to the setting.

5.2.3.8 TC5 Test [Test number: 7]

The TC5 test has only the TC5 timer mode.

In this test, by activating the 8-bit timer, TC5 interrupts are generated and COMMON pin outputs are inverted in TC5 interrupt processing. By monitoring the COMMON pin output, the TC5 interrupt cycle can be measured to check whether TC5 is operating according to the setting.

The test number of TC5 test is 7. No mode selection is performed.

In this test, each setting pattern specifies the operating mode, high-/low-frequency selection, TTREG5, and TC5 source clock.

Table 5.2.27 shows the register set values for each setting pattern.

Table 5.2.27 Register Set Values for TC5 Test

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC5CR)	(TTREG5)	TC5 Interrupt Cycle
0	NORMAL(0xC0)	fc (0x00)	$fc/2^{11}$(0x08)	(0x04)	1.024ms
1				(0xC8)	51.2ms
2			$fc/2^{7}$(0x18)	(0x19)	400μs
3				(0x3F)	1.0008ms
4			$fc/2^{5}$(0x28)	(0x0E)	60μs
5				(0x32)	200μs
6			$fc/2^{3}$(0x38)	(0x01)	1μs(*)
7				(0x05)	5μs(*)
8				(0x32)	50μs
9				(0x64)	100μs
10				(0xC8)	200μs
11				(0xFF)	255μs
12		fs (0x10)	$fs/2^{3}$(0x08)	(0x01)	244μs
13				(0x29)	10.004ms
14	SLOW(0xE0)	fc (0x00)	$fs/2^{3}$(0x08)	(0x01)	244μs(*)
15				(0x29)	10.004ms

* In these settings, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the setting.

5.2.3.9 TC6 Test [Test number: 8]

The TC6 test has the following four modes:

- 8-bit Timer Mode
  The 8-bit timer is activated and COMMON pin outputs are inverted in TC6 interrupt processing. By monitoring the COMMON pin, the TC6 interrupt cycle can be measured to check whether the 8-bit timer mode is operating according to the setting.
- 8-bit Event Counter Mode
  By using the counter by input pulses from the ECIN pin, TC6 interrupts are generated and COMMON pin outputs are inverted in TC6 interrupt processing. By monitoring the COMMON pin, the TC6 interrupt cycle can be measured to check whether the 8-bit event counter mode is operating according to the setting.
- 8-bit PDO Mode
  8-bit PDO is output to the TC6 pin and COMMON pin outputs are inverted in TC6 interrupt processing. By monitoring signals output from the COMMON and C6 pins, the TC6 interrupt cycle and PDO output can be measured to check whether the 8-bit PDO mode is operating according to the setting.
- 8-bit PWM Mode
  8-bit PWM is output to the TC6 pin and COMMON pin outputs are inverted in TC6 interrupt processing. By monitoring signals output from the COMMON and TC6 pins, whether the TC6 interrupt cycle and PWM output are operating according to the setting can be checked.

The test number of TC6 test is 8. Table 5.2.28 shows the mode numbers and setting items of TC6 test.

Table 5.2.28 Modes and Setting Items of TC6 Test

Mode Name	Mode No	Setting Item
8bit Timer Mode	0	Operating mode, High-/Low-frequency selection, TTREG6, TC6 source clock
8bit Event Counter Mode	1	Operating mode, TTREG6
8bit PDO Mode	2	Operating mode, High-/Low-frequency selection, TTREG6, TC6 source clock, TTF
8bit PWM Mode	3	Operating mode, High-/Low-frequency selection, PWREG6, TC6 source clock, TTF

Table 5.2.29 to Table 5.2.32 show the register set values for each setting pattern.

Table 5.2.29 Register Set Values for TC6 8-bit Timer

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC6CR)	(TTREG6)	TC3 Interrupt Cycle
0	NORMAL(0xC0)	fc (0x00)	$fc/2^{11}$(0x08)	(0x04)	1.024ms
1				(0xC8)	51.2ms
2			$fc/2^{7}$(0x18)	(0x19)	400µs
3				(0x3F)	1.0008ms
4			$fc/2^{5}$(0x28)	(0x0E)	60µs
5				(0x32)	200µs
6			$fc/2^{3}$(0x38)	(0x01)	1µs(*)
7				(0x05)	5µs(*)
8				(0x32)	50µs
9				(0x64)	100µs
10				(0xC8)	200µs
11				(0xFF)	255µs
12		fs (0x10)	$fs/2^{3}$(0x08)	(0x01)	244µs
13				(0x29)	10.004ms
14	SLOW(0xE0)	fc (0x00)	$fs/2^{3}$(0x08)	(0x01)	244µs(*)
15				(0x29)	10.004ms

* In these settings, because the interupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the setting.

Table 5.2.30 Register Set Values for TC6 8-bit Event Counter

Setting No	Operating Mode (SYSCR2)	(TC6CR)	(TTREG6)
0	NORMAL(0xC0)	(0x78)	(0xFF)
1			(0x7F)
2			(0x3F)
3			(0x1F)
4			(0x0F)
5			(0x08)
6			(0x02)
7			(0x01)
8			(0xFF)
9			(0x7F)
10			(0x3F)
11			(0x1F)
12			(0x0F)
13	SLOW(0xE0)		(0x08)
14			(0x02)
15			(0x01)

Table 5.2.31 Register Set Values for TC6 8-bit PDO

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC6CR)			(TTREG6)	Inversion Interval
				Frequency	TFF		
0	NORMAL(0xC0)	fc (0x00)	(0x09)	$fc/2^{11}$	CLR	(0x04)	1.024ms
1			(0x89)		SET		
2			(0x09)		CLR	(0x28)	10.24ms
3						(0x64)	25.6ms
4						(0xC8)	51.2ms
5			(0x19)	$fc/2^{7}$		(0x3F)	1ms
6						(0xFA)	4ms
7			(0x29)	$fc/2^{5}$		(0x05)	20μs(*)
8						(0x32)	200μs
9			(0x39)	$fc/2^{3}$		(0x02)	2μs(*)
10						(0xC8)	200μs
11		fs (0x10)	(0x09)	$fs/2^{3}$		(0x29)	10ms
12						(0xCD)	50ms
13	SLOW(0xE0)	fc (0x00)	(0x09)			(0x29)	10ms
14			(0x89)		SET		
15			(0x09)		CLR	(0xCD)	50ms

* In these settings, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the setting.

Table 5.2.32 Register Set Values for TC6 8-bit PWM

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	(TC6CR)			(PWREG6)	Inversion Interval
				fc	TTF		
0	NORMAL(0xC0)	fc (0x00)	(0x0A)	$fc/2^{11}$	CLR	(0x40)	16.38ms
1			(0x8A)		SET		
2			(0x2A)	$fc/2^{5}$	CLR		256μs
3			(0xAA)		SET		
4			(0x5A)	$fc/2^{2}$	CLR		16μs(*)
5			(0xDA)		SET		
6			(0x4A)	fs	CLR		1.95ms
7			(0xCA)		SET		
8			(0x6A)	fc	CLR		8μs(*)
9			(0xEA)		SET		
10		fs (0x10)	(0x0A)	$fs/2^{3}$	CLR		15.616ms
11			(0x8A)		SET		
12	SLOW(0xE0)	fc (0x00)	(0x0A)	$fs/2^{3}$	CLR		
13			(0x8A)		SET		
14			(0x4A)	fs	CLR		1.95ms
15			(0xCA)		SET		

* In these settings, because the interrupt cycle is shorter thatn the interrupt processing time, interrupts are not generated according to the setting.

5.2.3.10 16-bit TC5 + 6 Test [Test number: 9]

The 16-bit TC5 + 6 test has the following three modes:

- 16-bit Timer Mode
  The 16-bit timer is activated and COMMON pin outputs are inverted in TC6 interrupt processing. By monitoring the COMMON pin, the TC6 interrupt cycle can be measured to check whether the 16-bit timer mode is operating according to the setting.
- 16-bit PWM Mode
  16-bit PWM is output to the TC6 pin and COMMON pin outputs are inverted in TC6 interrupt processing. By monitoring the COMMON and TC6 pins, the TC6 interrupt cycle and PWM output can be measured to check whether the 16-bit PWM mode is operating according to the setting.
- 16-bit PPG Mode
  16bit PPG is output to the TC6 pin and COMMON pin outputs are inverted in TC6 interrupt processing. By monitoring the COMMON and TC6 pins, the TC6 interrupt and PPG output can be measured to check whether the 16-bit PPG mode is operating according to the setting.

The test number of 16-bit TC5 + 6 test is 9. Table 5.2.33 shows the modes and setting items of 16-bit TC5 + 6 test.

Table 5.2.33 Modes and Setting Items of TC6 Test

Mode Name	Mode No	Setting Item
16bit Timer Mode	0	Operating mode, High-/Low-frequency selection, TTREG5, TTREG6, TC6 source clock
16bit PDO Mode	1	Operating mode, High-/Low-frequency selection, PWREG5, PWREG6, TC6 source clock, TTF
16bit PPG Mode	2	Operating mode, High-/Low-frequency selection, TTREG5, TTREG6, PWREG5, PWREG6, TC6 source clock, TTF

Table 5.2.34 to Table 5.2.36 show the register set values for each setting pattern.

Table 5.2.34 Register Set Values for TC5 + 6 16-bit Timer

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC5CR)	(TC6CR)	(TTREG56)	TC56 Interrupt Cycle
0	NORMAL(0xC0)	fc (0x00)	$fc/2^{11}$(0x08)	(0x0C)	(0x0001)	256μs
1					(0x0F42)	1s
2			$fc/2^{7}$(0x18)		(0x0001)	16μs
3					(0xF424)	1s
4			$fc/2^{5}$(0x28)		(0x0005)	20μs
5					(0xC350)	200ms
6			$fc/2^{3}$(0x38)		(0x0100)	1μs(*)
7					(0x0014)	20μs
8					(0x0064)	100μs
9					(0x03E8)	1ms
10					(0x2710)	10ms
11					(0xC350)	50ms
12		fs (0x10)	$fs/2^{3}$(0x08)		(0x0001)	244μs
13					(0x1002)	1s
14	SLOW(0xE0)	fc (0x00)			(0x0001)	244μs(*)
15					(0x1002)	1s

* In these settings, because the interrupt cycle is shorter than the interrupt processing time, interrupts are not generated according to the setting.

Table 5.2.35 Register Set Values for TC5 + 6 16-bit PWM

Setting Item	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC5CR)	TTF (TC6CR)	(TTREG56)	Inversion Interval
0	NORMAL(0xC0)	fc (0x00)	$fc/2^{11}$(0x0B)	CLR(0x0E)	(0x4000)	4.19s
1			$fc/2^{7}$(0x1B)			262.144ms
2			$fc/2^{5}$(0x2B)			65.536ms
3			$fc/2^{3}$(0x3B)			16.384ms
4				SET(0x8E)		
5				CLR(0x0E)	(0x2000)	8.191ms
6					(0x1000)	4.0955ms
7					(0x0800)	2.04775ms
8					(0x0400)	1.023875ms
9					(0x0200)	511.9375μs
10			fs(0x4B)		(0x4000)	499.712ms
11			fc/2(0x5B)			4.096ms
12			fc(0x6B)			2.048ms
13		fs (0x10)	$fs/2^{3}$(0x0B)			3.997696s
14	SLOW(0xE0)	fc (0x00)	$fs/2^{3}$(0x0B)			3.997696s
15			fs(0x4B)			499.712ms

Table 5.2.36 Register Set Values for TC5 + 6 16-bit PPG

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	Frequency Selection (TC5CR)	TFF (TC6CR)	(TTREG 56)	(PWREG 56)	Inversion Interval	Interrupt Cycle
0	NORMAL (0xC0)	fc (0x00)	$fc/2^{11}$(0x0B)	CLR(0x0F)	(0x0640)	(0x0190)	100ms	400ms
1				SET(0x8F)				
2			$fc/2^{7}$(0x1B)	CLR(0x0F)	(0x09C4)	(0x0271)	10ms	40ms
3				SET(0x8F)				
4			$fc/2^{5}$(0x2B)	CLR(0x0F)	(0x2710)	(0x09C4)	10ms	40ms
5				SET(0x8F)				
6			$fc/2^{3}$(0x3B)	CLR(0x0F)	(0x9c40)	(0x2710)	10ms	40ms
7				SET(0x8F)				
8				CLR(0x0F)		(0x1388)	5ms	40ms
9				SET(0x8F)	(0x4E20)	(0x2710)	10ms	20ms
10				CLR(0x0F)	(0x0014)	(0x000A)	10μs	20μs
11				SET(0x8F)	(0x0005)	(0x0001)	1μs	5μs
12		fs (0x10)	$fs/2^{3}$(0x0B)	CLR(0x0F)	(0x0668)	(0x019A)	100ms	400ms
13				SET(0x8F)				
14	SLOW (0xE0)	fc (0x00)		CLR(0x0F)				
15				SET(0x8F)				

* Because the inversion interval is short, inversion waveforms may not be ourput properly. Also, interrupts may not be generated according to the setting.

5.2.3.11 UART Test [Test number: 10]

The UART test has the following two modes:

- UART Tx (UART Transmit Test) Mode
  Data is transmitted from the TXD pin and COMMON pin outputs are inverted in UART Tx interrupt processing. By monitoring the COMMON pin as well as the UART transmit data output from the TXD pin, whether UART Tx is operating according to the setting can be checked.
- UART Rx (UART Receive Test) Mode
  Data is received from the RXD pin and COMMON pin outputs are inverted in UART Rx interrupt processing. By monitoring the COMMON pin as well as displaying on LCD the UART receive data input from the RXD pin, whether UART Rx is operating according to the setting can be checked.

The test number of UART test is 10. Table 5.2.37 shows the mode numbers and setting items of UART test.

Table 5.2.37 Modes and Setting Items of UART Test

Mode Name	Mode No	Setting Item
UART Tx Mode	0	Operating mode, Transmit stop bit length, Parity, Transfer clock, TTREG5, TC5 source clock, Transfer data
UART Rx Mode	1	Operating mode, Receive stop bit length, Parity, Transfer clock, TTREG5, TC5 source clock

(In the UART test, noise cancellation is set to “none”.)

The test completed state is entered after data transfer in the UART Tx mode and after data receive in the UART Rx mode. In the test competed state, transmitted or received data is displayed on LCD. This display is made divided into three times. When the display number is 1, the 1^{st} to 3^{rd} words of data are displayed. When the display number is 2, the 4^{th} to 6^{th} words are displayed When the display number is 3, the 7^{th} and 8^{th} words are displayed.

The 9^{th} and 8^{th} digits on LCD display the display number. The 7^{th} and 6^{th} digits display the 3^{rd} or 6^{th} word of transmit/receive data. The 4^{th} and 3^{rd} digits display the 2^{nd}, 5^{th}, or 8^{th} word . The 2^{nd} and 1^{st} digits display the 1^{st}, 4^{th}, or 7^{th} word.

The display number (1 to 3) is selected with “F4 Key” input.

If an error occurs during transfer, the cause of error is displayed on the 8^{th} to 6^{th} digits of Display Number 3. This display is made in the following manne:

Table 5.2.38 Error Display in UART Transfer

Display digit	Display	Cause
8^{th} digit	O	Overrun error
7^{th} digit	F	Flaming error
6^{th} digit	P	Parity error

If these errors occur, change the set value and transmit data again.

By pressing “INT0 Interrupt Key” in the study completed state, the state returns to the test item setting state.

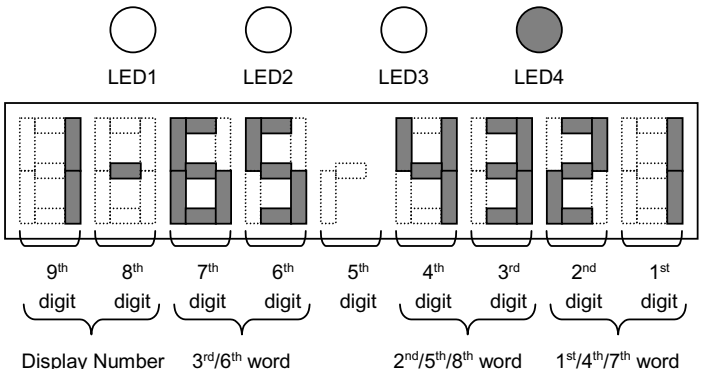


Figure 5.2.4 UART Test Completed

Note: In UART transmit, after data without parity and with 1-bit stop bit is output, if data is sent with parity and 2-bit stop bit, it has been observed that the TxD pin remains at "L" level and does not return to "H" level. Threfore, **after a test to transmit data without parity and with 1-bit stop bit, do not perform a test to transmit data with parity and 2-bit stop bit.** If tests are performed in this sequence, forciblly perform a reset with "Reset Key".

The same transmit data is used for the UART transmit test and for the SIO transmit and SIO receive tests that are described in the following chapter.

Table 5.2.39 shows the transmit data numbers and transmit data contents.

Table 5.2.39 Transmit Data for UART Tx, SIO Tx and SIO TxRx Tests

Transmit Data No (DataNo.)	Transmit Data Contents
0	0x10, 0x32, 0x54, 0x76, 0x98, 0xBA, 0xDC, 0xFE
1	0x21, 0x43, 0x65, 0x87, 0xA9, 0xCB, 0xED, 0x0F
2	0x32, 0x54, 0x76, 0x98, 0xBA, 0xDC, 0xFE, 0x10
3	0x43, 0x65, 0x87, 0xA9, 0xCB, 0xED, 0x0F, 0x21
4	0x54, 0x76, 0x98, 0xBA, 0xDC, 0xFE, 0x10, 0x32
5	0x65, 0x87, 0xA9, 0xCB, 0xED, 0x0F, 0x21, 0x43
6	0x76, 0x98, 0xBA, 0xDC, 0xFE, 0x10, 0x32, 0x54
7	0x87, 0xA9, 0xCB, 0xED, 0x0F, 0x21, 0x43, 0x65
8	0x98, 0xBA, 0xDC, 0xFE, 0x10, 0x32, 0x54, 0x76
9	0xA9, 0xCB, 0xED, 0x0F, 0x21, 0x43, 0x65, 0x87
10	0xBA, 0xDC, 0xFE, 0x10, 0x32, 0x54, 0x76, 0x98
11	0xCB, 0xED, 0x0F, 0x21, 0x43, 0x65, 0x87, 0xA9
12	0xDC, 0xFE, 0x10, 0x32, 0x54, 0x76, 0x98, 0xBA
13	0xED, 0x0F, 0x21, 0x43, 0x65, 0x87, 0xA9, 0xCB
14	0xFE, 0x10, 0x32, 0x54, 0x76, 0x98, 0xBA, 0xDC
15	0x0F, 0x21, 0x43, 0x65, 0x87, 0xA9, 0xCB, 0xED

Table 5.2.40 and Table 5.2.41 show the register set values for each setting pattern.

Table 5.2.40 Register Set Items for UART Tx

Setting No	High-/Low-Frequency Selection (TBTCR)	(UARTCR1)					DataNo	(TC5CR)	(TTREG5)
			Frequency	Baud Rate	Parity	StopBit			
0	fc (0x00)	(0x80)	fc/13	38400	None	1bit	0	—	—
1							1		
2							2		
3							3		
4		(0xA0)				2bit	4		
5		(0x88)			Odd	1bit	5		
6		(0x98)			Even		6		
7		(0xA8)			Odd	2bit	7		
8		(0xB8)			Even		8		
9		(0x81)	fc/26	19200	None	1bit	9		
10		(0x82)	fc/52	9600			10		
11		(0x83)	fc/104	4800			11		
12		(0x84)	fc/208	2400			12		
13		(0x85)	fc/416	1200			13		
14		(0x86)	TC5(250KHz)				14	(0x28)	(0x01)
15	fs (0x10)		TC5(4KHz)				15	(0x08)	(0x01)

Table 5.2.41 Register Set Items for UART Rx

Setting No	High-/Low-Frequency Selection (TBTCR)	(UARTCR1)				StopBit (UARTCR2)	(TC5CR)	(TTREG5)
			Frequency	Baud Rate	Parity			
0	fc (0x00)	(0x40)	fc/13	38400	None	1 bit (0x00)	—	—
1								
2								
3								
4						2bit (0x01)		
5		(0x48)			Odd	1bit (0x00)		
6		(0x58)			Even			
7		(0x48)			Odd	2bit (0x01)		
8		(0x58)			Even			
9		(0x41)	fc/26	19200	None	1bit (0x00)		
10		(0x42)	fc/52	9600				
11		(0x43)	fc/104	4800				
12		(0x44)	fc/208	2400				
13		(0x45)	fc/416	1200				
14		(0x46)	TC5(250KHz)				(0x28)	(0x01)
15	fs (0x10)		TC5(4KHz)				(0x08)	(0x01)

5.2.3.12 SIO Test [Test number: 11]

The SIO test has the following three modes:

- SIO Tx (SIO Transmit) Mode
  SIO data is transmitted from the TxD pin and COMMON pin outputs are inverted in SIO interrupt processing. By monitoring the COMMON pin as well as the SCK and SO pins, transmit data can be measured to check whether the SIO Tx mode is operating according to the setting.
- SIO Rx (SIO Receive) Mode
  SIO data is received from the RxD pin and COMMON pin outputs are inverted in SIO interrupt processing. By monitoring the COMMON pin to measure the interrupt cycle as well as receiving data sent in synchronization with the serial clock and displaying it on LCD, whether the SIO Rx mode is operating properly can be checked.
- SIO TxRx (SIO Transmit/Receive) Mode
  SIO data is transmitted from the TxD pin and data is received from the RxD pin at the same time. COMMON pin outputs are inverted in SIO interrupt processing. By monitoring the COMMON pin to measure the interrupt cycle as well as displaying on LCD the transmit data output from the SO pin in synchronization with the serial clock and the receive data input from the SI pin, whether the SIO TxRx mode is operating according to the setting can be checked.

The test number of SIO test is 11. Table 5.2.42 shows the mode numbers and setting items of SIO test.

Table 5.2.42 Modes and Setting Items of SIO Test

Mode Name	Mode No	Setting Item
SIO Tx Mode	0	Operating mode, High-/Low-frequency selection, Transmit mode, Serial clock, Transfer word number, Transmit data
SIO Rx Mode	1	Operating mode, High-/Low-frequency selection, Receive mode, Serial clock, Transfer word number
SIO TxRx Mode	2	Operating mode, High-/Low-frequency selection, Serial clock, Transfer word number, Transmit data, WAIT control

In the SIO test, 8-byte data is transferred. When transfer is made by 1 word, transfer is started again in SIO interrupt and SIO transfer is repeated until all 8-word data is transferred.

For data to be transmitted, see Table 5.2.39.

After 8-word data is transmitted/received, the SIO test enters the test completed state. In the test completed state, transmitted/received data is displayed on LCD. In the SIO Tx and SIO Rx modes, transmitted/received 8-word data is displayed divided into three times (display number:1 to 3). In the SIO TxRx mode, transmitted data is displayed when the display number is 1 to 3, and received data is displayed when the display number is 4 to 6. When the display number is 1 or 4, 1^{st} to 3^{rd} words are displayed. When the display number is 2 or 5, the 4^{th} to 6^{th} words are displayed. When the display number is 3 or 6, the 7^{th} and 8^{th} words are displayed.

The display number (1 to 3, 1 to 6 in the TxRx mode) is displayed on the 9^{th} and 8^{th} digits on LCD. It is selected with “K4 Key” input.

By pressing “INT0 Interrupt Key” in the test completed state, the state returns to the test item setting state.

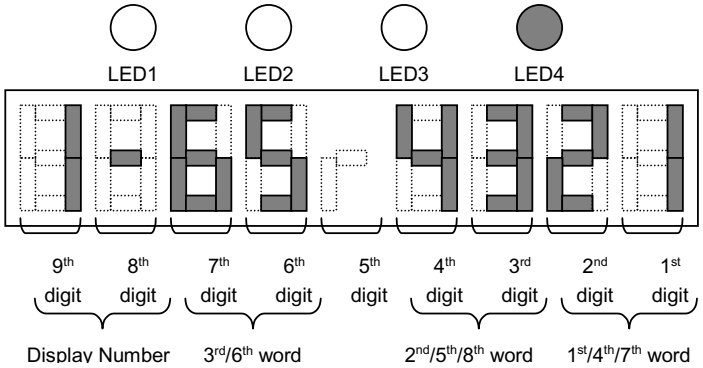


Figure 5.2.5 SIO Test Completed

Table 5.2.43 to Table 5.2.45 show the register set values for each setting pattern.

Table 5.2.43 Register Set Values for SIO Tx

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	(SIOCR1)			Transfer word number BUF (SIOCR2)	DataNo.
				Transfer bit (SIOM)	Transfer clock (SCK)		
0	NORMAL (0xC0)	fc (0x00)	(0x97)	4	External sck pin	1word(0x00)	0
1			(0x87)	8			1
2			(0x97)	4		8word(0x07)	2
3			(0x87)	8			3
4			(0x90)	4	$fc/2^{13}$	1word(0x00)	4
5			(0x80)	8		8word(0x07)	5
6			(0x92)	4	$fc/2^{7}$	1word(0x00)	6
7			(0x82)	8		8word(0x07)	7
8			(0x95)	4	$fc/2^{4}$ (*)	1word(0x00)	8
9			(0x85)	8		8word(0x07)	9
10		fs (0x10)	(0x90)	4	$fs/2^{5}$	1word(0x00)	10
11			(0x80)	8		8word(0x07)	11
12	SLOW(0xE0)	fc (0x00)	(0x90)	4		1word(0x00)	12
13			(0x80)	8			13
14			(0x90)	4		8word(0x07)	14
15			(0x80)	8			15

Table 5.2.44 Register Set Values for SIO Rx

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	(SIOCR1)			Transfer word number BUF(SIOCR2)
				Transfer bit (SIOM)	Transfer clock (SCK)	
0	NORMAL (0xC0)	fc (0x00)	(0xB7)	4	External sck pin	1word(0x00)
1			(0xAF)	8		
2			(0xB7)	4		8word(0x07)
3			(0xAF)	8		
4			(0xB0)	4	$fc/2^{13}$	1word(0x00)
5			(0xA8)	8		8word(0x07)
6			(0xB2)	4	$fc/2^{7}$	1word(0x00)
7			(0xAA)	8		8word(0x07)
8			(0xB5)	4	$fc/2^{4}$ (*)	1word(0x00)
9			(0xAD)	8		8word(0x07)
10		fs (0x10)	(0xB0)	4	$fs/2^{5}$	1word(0x00)
11			(0xA8)	8		8word(0x07)
12	SLOW(0xE0)	fc (0x00)	(0xB0)	4		1word(0x00)
13			(0xA8)	8		
14			(0xB0)	4		8word(0x07)
15			(0xA8)	8		

Table 5.2.45 Register Set Values for SIO TxRx

Setting No	Operating Mode (SYSCR2)	High-/Low-Frequency Selection (TBTCR)	(SIOCR1)		(SIOCR2)			Data No.
				Transfer clock (SCK)		Transfer Word No BUF	WAIT	
0	NORMAL (0xC0)	fc (0x00)	(0xA7)	External sck pin	(0x00)	1word	TD	0
1			(0xA7)		(0x18)		8TD	1
2			(0xA7)		(0x07)	8word	TD	2
3			(0xA7)		(0x1F)		8TD	3
4			(0xA0)	$fc/2^{13}$	(0x00)	1word	TD	4
5			(0xA0)		(0x18)		8TD	5
6			(0xA0)		(0x07)	8word	TD	6
7			(0xA0)		(0x1F)		8TD	7
8			(0xA2)	$fc/2^{7}$	(0x00)	1word	TD	8
9			(0xA2)		(0x07)	8word		9
10			(0xA5)	$fc/2^{4}$	(0x00)	1word		10
11			(0xA5)		(0x07)	8word		11
12		fs (0x10)	(0xA0)	$fs/2^{5}$	(0x00)	1word		12
13			(0xA0)		(0x18)	8word		13
14	SLOW(0xE0)	fc (0x00)	(0xA0)		(0x07)	1word		14
15			(0xA0)		(0x1F)	8word		15

* In SIO transfer, when $fc/2^{4}$ is selected as a serial clock, data may not be transferred properly depending on the connecting line of the SCK pin.

In SIO transmit/receive (SIO TxRx), a part of receive data may not be transferred properly.

5.2.3.13 ADC Test [Test number: 12]

The ADC test has the following two modes:

- Single Mode
  COMMON pin outputs are inverted in AD converter interrupt processing. By measuring each of analog inputs from the AIN0 pin three times and displaying results on LCD, whether the single mode is operating according to the setting can be checked.
- Repeat Mode
  COMMON pin outputs are inverted in AD converter interrupt processing. By monitoring the COMMON pin as well as measuring each of analog inputs from the AIN0 pin three times and displaying results on LCD, whether the repeat mode is operating according to the setting can be checked.

The test number of AD converter test is 12. Table 5.2.46 shows the mode numbers and setting items of AD converter test.

Table 5.2.46 Modes and Setting Items of AD converter Test

Mode Name	Mode No	Setting Item
Single Mode	0	Operating mode, Ladder resistor ON/OFF, AD conversion time
Repeat Mode	1	Operating mode, Ladder resistor ON/OFF, AD conversion time

After measurements are performed a fixed number of times, the AD converter test enters the test completed state. In the test completed state, 10-bit data after AD conversion is displayed on LCD. When the display number is 1, 2, and 3, the 1st, 2nd, and 3rd AD conversion data is displayed, respectively.

The display number (1 to 3) is selected with "F4 Key" input.

By pressing "INT0 Interrupt Key" in the test completed state, the state returns to the test item setting state.

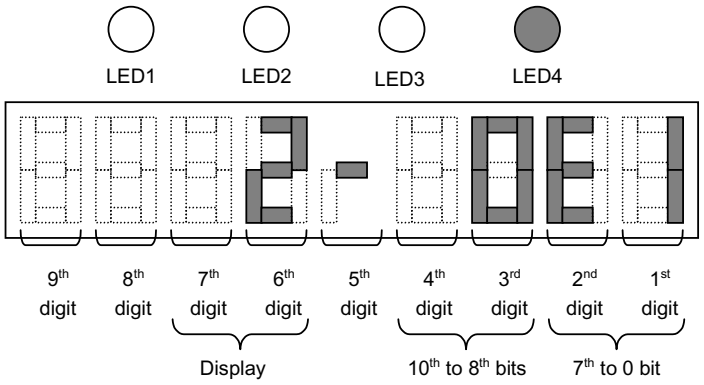


Figure 5.2.6 ADC Test Completed

Table 5.2.47 and Table 5.2.48 show the register set values for each setting pattern.

Table 5.2.47 Register Set Values for Single Mode

Setting No	(ADCCR1)	(ADCCR2)		
			ACK	IREFON
0	(0xA0)	(0x16)	19.5μs	0
1		(0x36)		1
2		(0x18)	39.0μs	0
3		(0x38)		1
4		(0x1A)	78.0μs	0
5		(0x3A)		1
6		(0x1A) (For continuous test)	78.0μs	0
7				
8				
9				
10				
11				
12				
13				
14				
15				

Table 5.2.48 Register Set Values for Repeat Mode

Setting No	(ADCCR1)	(ADCCR2)		
			ACK	IREFON
0	(0xE0)	(0x16)	19.5μs	0
1		(0x36)		1
2		(0x18)	39.0μs	0
3		(0x38)		1
4		(0x1A)	78.0μs	0
5		(0x3A)		1
6		(0x1A) (For continuous test)	78.0μs	0
7				
8				
9				
10				
11				
12				
13				
14				
15				

5.2.3.14 LCD Test [Test number: 13]

The LCD test checks the operation of LCD by lighting segments of LCD one by one.

When the LCD test is started, one segment in the 1st digit lights up. Each time "F4 Key" is pressed, the lighted segment changes. By this operation, LCD lights can be checked.

To end the LCD test, press "INT0 Interrupt Key".

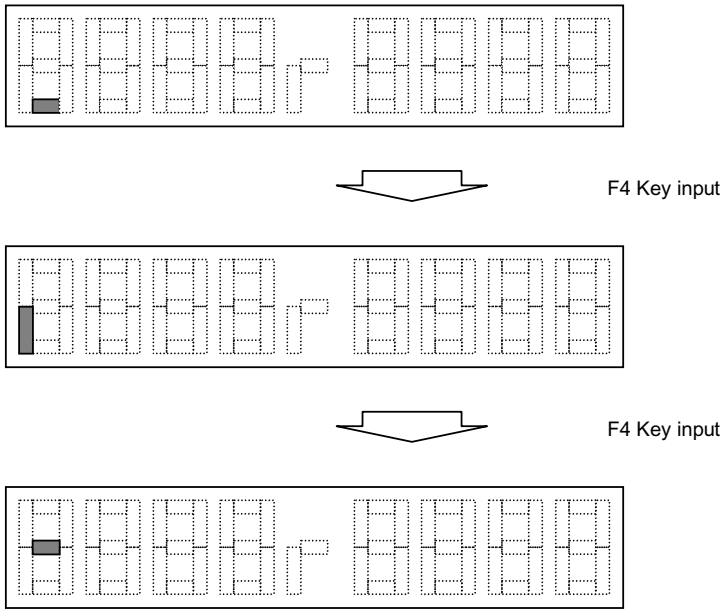


Figure 5.2.7 LCD Display Test [13-0-0]

5.2.3.15 Continuous Test [Test number: 14]

In the continuous test, tests can be performed one after another continuously. "INT0 Interrupt Key" ends each test and starts the next test.

The setting number that is set at the start is applied to all tests. In other words, when the setting number 0 is selected, all tests (TBT test, watchdog timer test, etc) are performed with the setting number 0.

For details of each test, see the test items for each test.

In the continuous test, the 9th digit on LCD displays "A", the 6th and 7th digits display the test number, the 4th digit displays the test mode, and the 1st and 2nd digits display the setting number.

Figure 5.2.8 shows an example of LCD display when a test of test number 3, mode 0, setting number 1 (TC1 timer test) is executed.

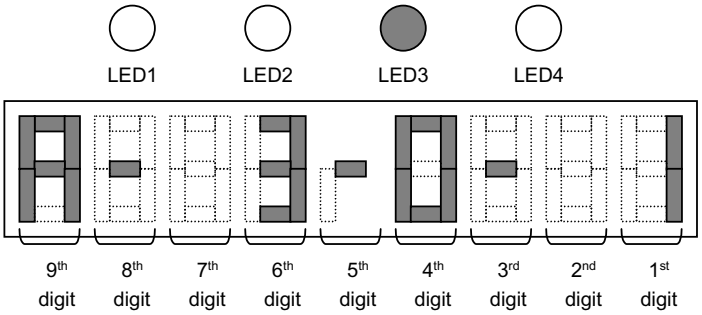


Figure 5.2.8

In the continuous test, the following tests are performed:

Table 5.2.49 Description of Continuous Test

Test No	Mode No	Description of Test	
0	0	TBT test	Time Base Timer
1	0	WDT test	Interrupt request
2	0	DVO test	DVO
3	0	TC1 test	18-bit timer
	1		18-bit event counter
	2		Pulse width measurement
	3		Frequency measurement
4	0	TC3 test	8-bit timer
	1		8-bit event counter
	2		8-bit PDO
	3		8-bit PWM
5	0	TC4 test	8-bit timer
	1		8-bit event counter
	2		8-bit PDO
	3		8-bit PWM
6	0	TC3 + 4 test	16-bit timer
	1		16-bit event counter
	2		16-bit PWM
	3		16-bit PPG
7	0	TC5 test	8-bit timer
8	0	TC6 test	8-bit timer
	1		8-bit event counter
	2		8-bit PDO
	3		8-bit PWM
9	0	TC5 + 6 test	16-bit timer
	1		16-bit PWM
	2		16-bit PPG
10	0	UART test	Tx
	1		Rx
11	0	SIO test	SIO Tx
	1		SIO Rx
	2		SIO TxRx
12	0	ADC test	Single mode
	1		Repeat mode

5.3 ROM/RAM Check Mode

In ROM/RAM Check mode, tests on internal ROM and RAM in the microcontroller are performed.

All LEDs are "OFF" in this mode.

When ROM/RAM Check mode is entered, the 9th to 6th digits on LCD display the check sum of internal ROM. The 4th to 1st digits display the most recent address where Read/Write are not performed properly. In internal RAM check, if there is no address where Read/Write are not performed properly, the 4th to 1st digits are all lit.

Key operation is not valid except for "Reset Key". After the check sum is displayed, press "Reset Key" to reset.

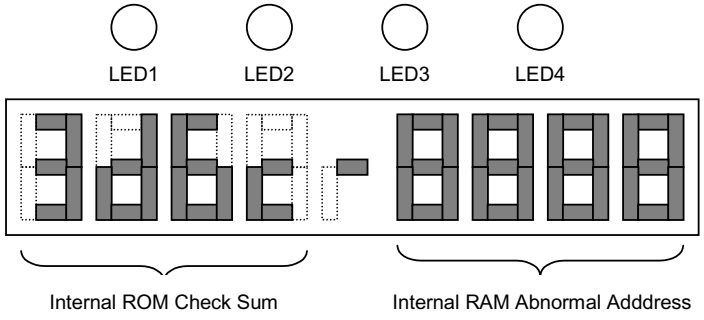


Figure 5.3.1 ROM/RAM Check Mode

6. Circuit Diagram

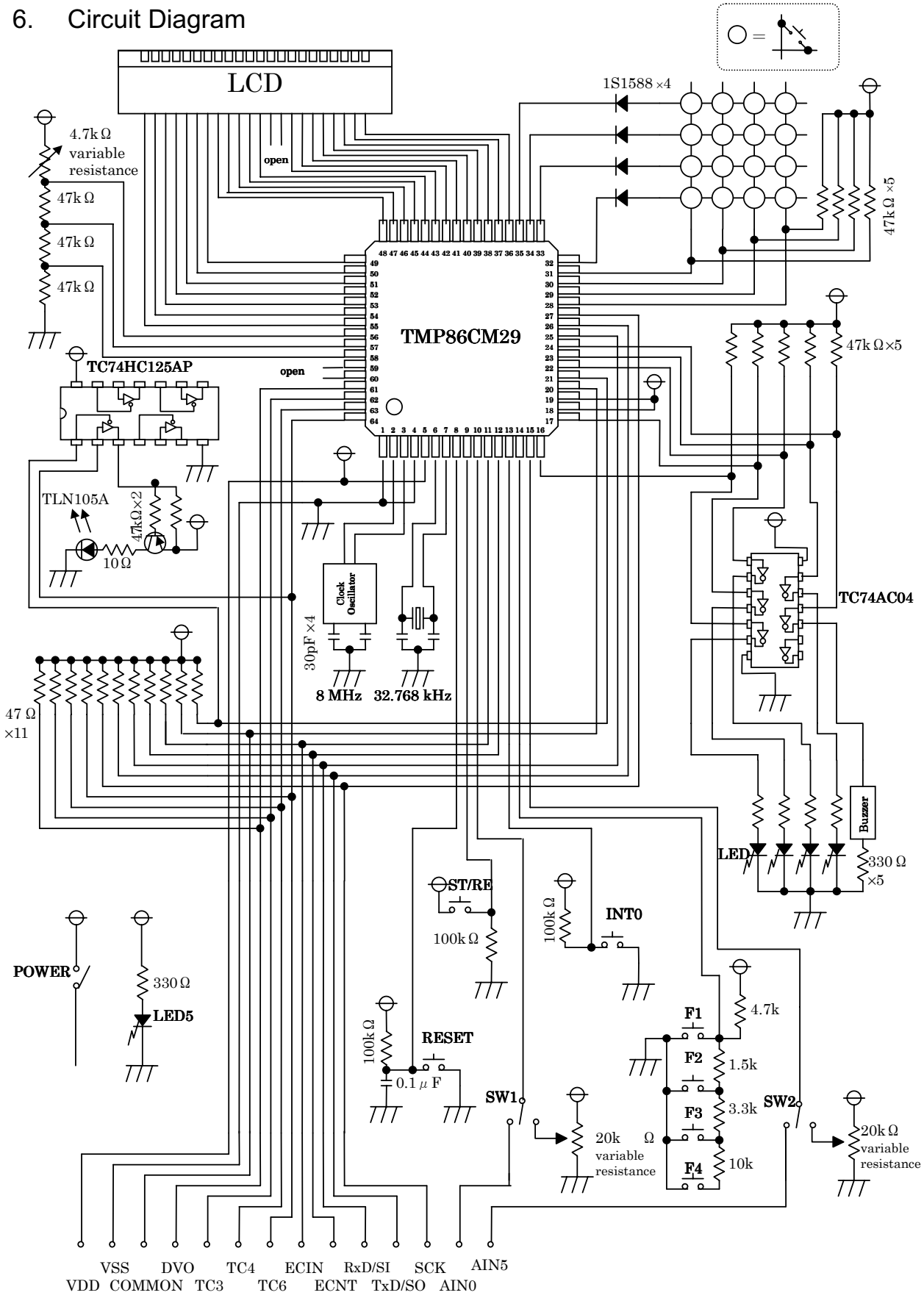


Figure 6.1 Circuit Diagram

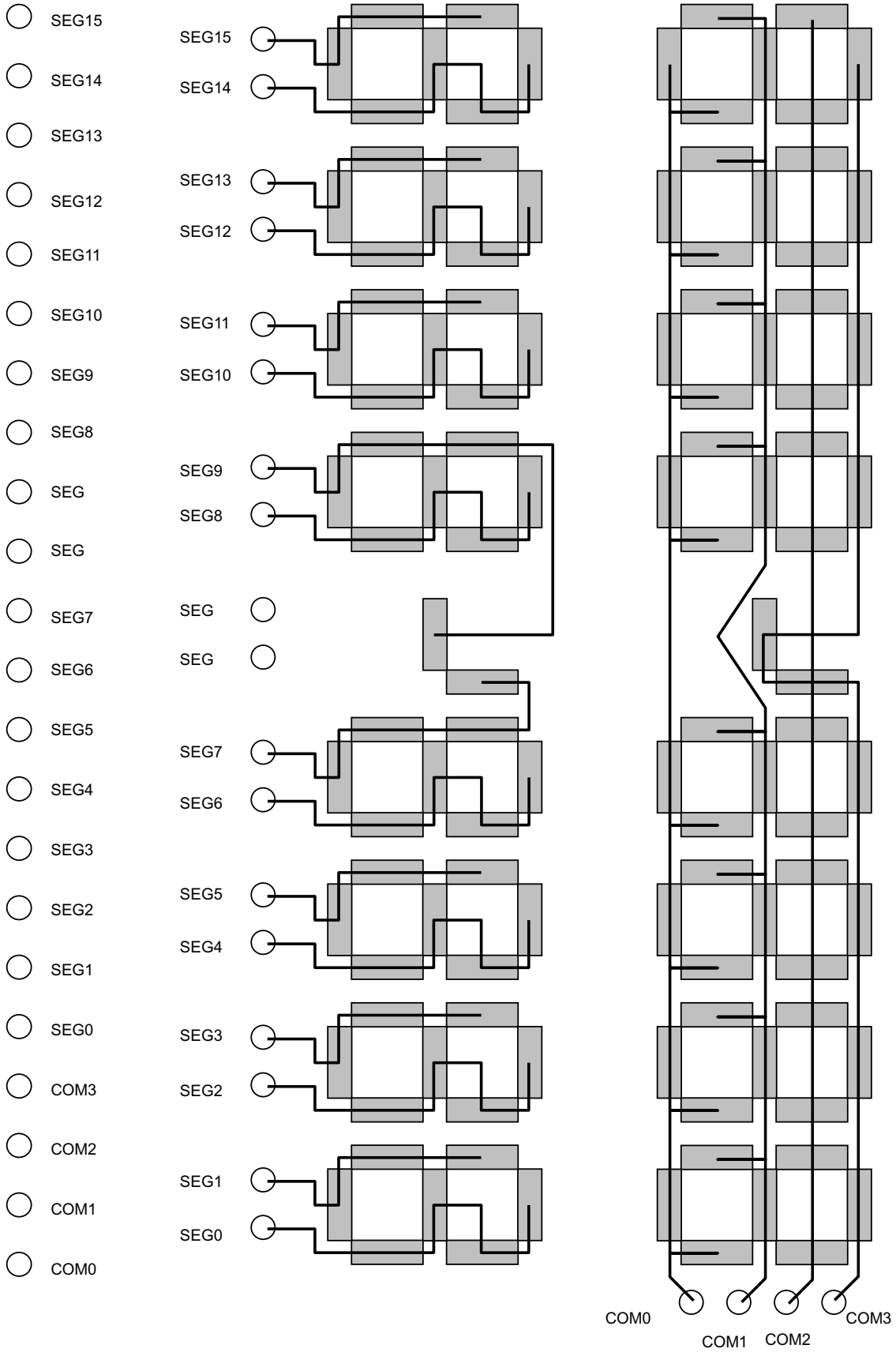


Figure 6.2 LCD Wiring

Postscript

This document describes the specifications of the demonstration set for the 8-bit microcontroller TMP86Cx29.

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