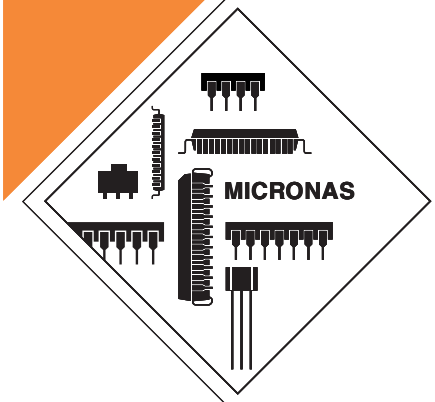

DRD 3515A
StarMan™ Channel Decoder for a WorldSpace™ TDM Downlink Carrier

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MICRONAS

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StarMan™ Channel Decoder for a WorldSpace™ TDM Downlink Carrier

1. Introduction

The WorldSpace System is a satellite based digital radio service for direct to home transmission of digital radio programs to WorldSpace radios. The coverage areas of this service are Africa, South America, and parts of Asia.

The DRD 3515A is the part of Micronas' StarMan chipset for demodulating and decoding the signals from the WorldSpace satellites. It performs channel demodulation, error correction, demultiplexing and the separation of one Broadcast Channel (BC). The DRD 3515A additionally provides an embedded stereo D/A converter and an amplifier for headphones or a small loudspeaker. Together with the audio decoder MAS 3506D, a micro controller and an L-band tuner, the DRD 3515A allows the design of compact and low cost WorldSpace receivers.

1.1. Features of the DRD 3515A

- Embedded 14.725 MHz crystal oscillator
- Two-battery cell (with DC/DC converter on the MAS 3506D) or three battery cell operation supported
- IF input with AGC and RSSI
- Digital I/Q splitting
- Fast synchronization strategy
- Crystal frequency offset compensation
- Embedded signal quality indication
- Demodulator status observable
- Stored TSCC information available in BC-mode
- Support of ES1 WorldSpace decrypting algorithm
- Full Broadcast Channel (BC) output available
- Optional serial output of one selected Service Component (SC)
- I^2S input interface for decoded MPEG audio signals
- Stereo D/A converter: S/N > 90 dB, THD < 0.01 %
- Two auxiliary analog stereo inputs
- Baseband audio source selector matrix
- Stereo line output, amplifier for stereo headphones or small mono speaker with click reduction
- Various low power and stand-by functions
- I^2C controller interface

1.2. System Overview

The Micronas StarMan chip set consists of the channel decoder DRD 3515A and the MPEG Layer 3 audio decoder MAS 3506D. All essential analog and digital building blocks for WorldSpace reception are provided on the Micronas chipset. Together with an L-band tuner and an appropriate controller this set builds a complete StarMan radio receiver.

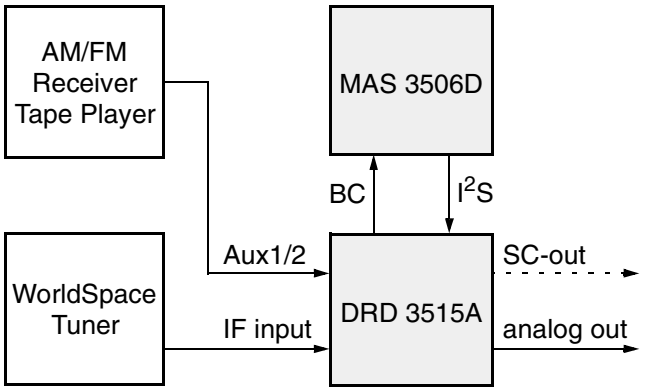

Fig. 1–1: Standard application of StarMan chipset

Since the DRD 3515A also contains an audio amplifier for headphone or small loudspeaker operation, only a minimum of external components are necessary. The additional inputs for analog signals (e.g. conventional AM/FM receiver, tape etc.) make the amplifier accessible to these audio sources and thus considerably simplify the design of complete radio receivers.

The analog audio output of the WorldSpace signal can be supplied to an external stereo amplifier for higher power output. Also a digital audio signal in standard I^2S format is provided for high end applications that may require an external D/A converter.

The complete WorldSpace Broadcast Channel (BC) is available as a serial output signal from the DRD 3515A and provides full access to all WorldSpace data by additional decoder modules. The additional Service Component (SC) output of the DRD 3515A may be useful in applications where a data and an audio channel are transmitted simultaneously. In this case the data component is directed to the SC output. The performance requirements for the data decoders are considerably lower for the Service Component because the demultiplexing of the BC-channel is already done inside the DRD 3515A. This function is independent from the audio Service Component extraction in the MAS 3506D.

Service Control Header data are available via I^2C controller interface from the MAS 3506D.

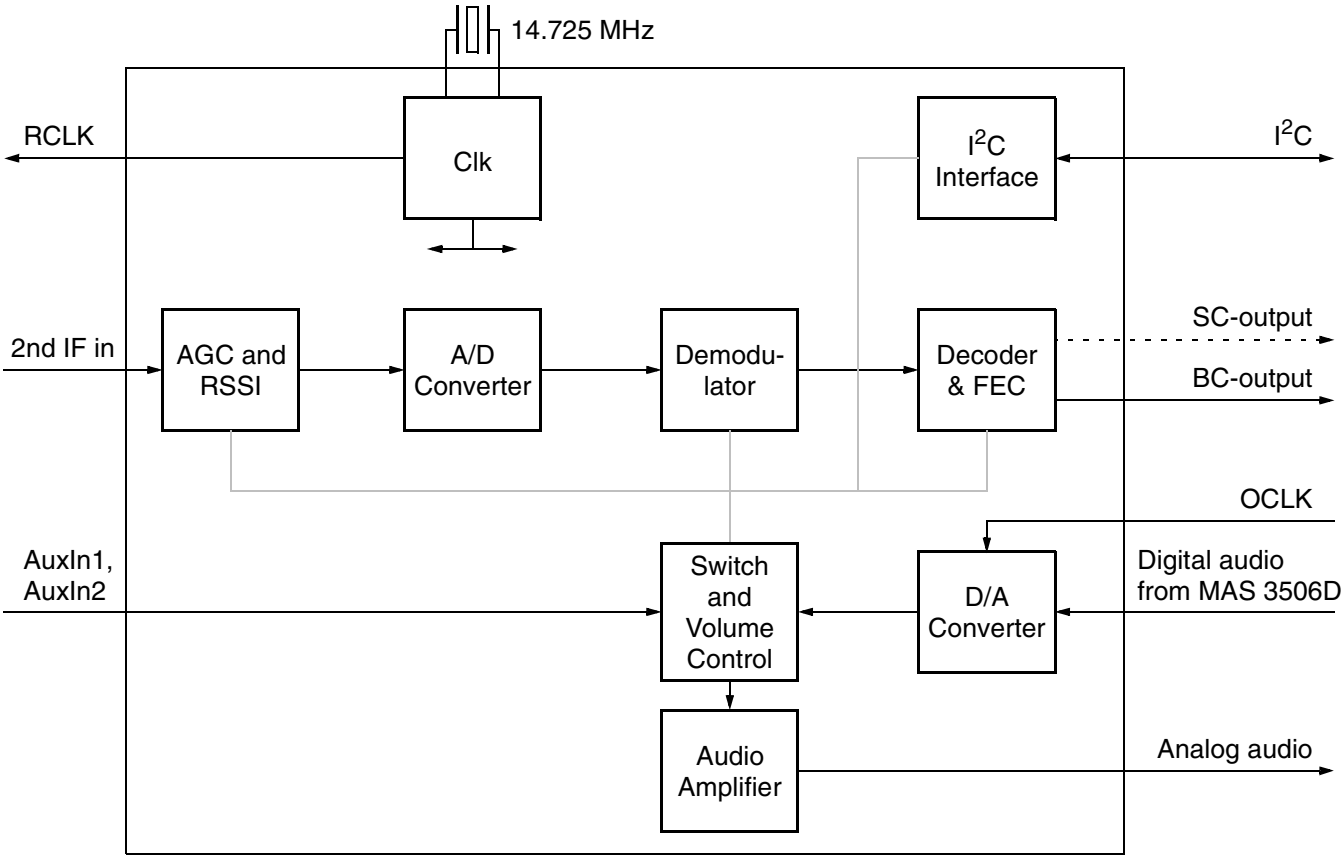

Fig. 1–2: Block diagram of the DRD 3515A

2. Functional Overview

2.1. The WorldSpace Signal

The WorldSpace satellite downlink carriers are QPSK-modulated. Every carrier transports a time division multiplex (TDM) signal with an overall gross bit rate of 3.68 Mbit/s. It consists of 96 Prime Rate Channels (PRC) with a gross (net) bit rate of 37.777 (16) kbit/s each and a frame header with the Master Frame Preamble (MFP, synchronization word) and the Time Slot Control Channel (TSCC, composition information).

One to eight of the Prime Rate Channels can be combined to yield one Broadcast Channels with a net bit rate of (1 ... 8) times 16 kbit/s (i.e. 16 ... 128 kbit/s).

The TDM data stream is assembled from all 96 Prime Rate Channels either at the main uplink station (transparent mode) or on the satellite by an on board baseband processor (processed mode). For the latter mode each radio station or service provider may separately uplink its own Broadcast Channel via FDMA (frequency division multiplex access).

Depending on the number of combined Prime Rate Channels each Broadcast Channel can be subdivided into one or more Service Components that may contain data services or compressed audio data.

2.2. General Signal Flow

The general signal flow within the DRD 3515A is depicted in Figure 2–1. The shaded regions demonstrate the membership of building blocks to different power supply areas. These areas will be selected or deselected depending on the various operating modes of the device.

The input signal of the DRD 3515A is one 3.68 Mb/s QPSK modulated WorldSpace TDM downlink carrier, which is down converted to an IF center frequency of 1.84 MHz. After a digitally controlled analog AGC, the A/D-conversion is performed.

Carrier and signal tracking, I/Q-splitting, and QPSK-demodulation are established digitally.

The information about the required Prime Rate Channels for the chosen Broadcast Channel is identified by the external controller and transmitted to the TDM demultiplexer. The required PRCs are then extracted from the TDM data stream by the demultiplexer. Error correction is done by a Viterbi and a Reed-Solomon decoder. The Service Components contained in this Broadcast Channel may carry compressed audio signals compliant with the MPEG 2 Layer 3 standard or data services.

The MAS 3506D selects the wanted audio Service Component and decompresses the Layer 3 encoded audio. The digital audio signal is transmitted back to the DRD 3515A via an I^2S serial interface for D/A conversion and amplification in the analog baseband block.

2.3. Power Supply Concept

All building blocks are implemented in low power CMOS technology. Two basic modes of operation are possible, a two battery operation using the DC/DC converter of the MAS 3506D, and a direct operation on three batteries or a stabilized power supply.

The DRD 3515A has 5 power supply regions.

2.3.1. Digital Power Supply

The two digital sections (I^2C interface and digital WorldSpace decoder blocks) are supplied via pin VDD. The interface part can be switched on via the pin PUP.

To activate the WorldSpace decoder parts the bit WSEN of the register GLB_CNFG must be set in addition to the PUP signal. This will also cause the WSEN output pin to go to a “high” level.

2.3.2. Analog Power Supply of the IF Section and the Oscillator

The IF input section and the quartz oscillator are powered via pin AVDD2. While the clock oscillator is switched on by the PUP signal only, the IF input section needs the WSEN bit of GLB_CNFG to be set in addition to PUP.

2.3.3. Performance of the Quartz Oscillator

If the tuner uses the quartz oscillator of the DRD 3515A as its master clock, it is highly recommended to use a well filtered supply voltage for the AVDD2 pin (e.g. a separate voltage stabilization) to avoid performance degradation of the oscillator due to power supply ripple.

2.3.4. Analog Power Supplies for the Audio Parts

The AVDD1 pin supplies the audio D/A converter, the analog switching and volume control parts. The AVDD0 pin supplies the audio amplifier. These parts can be enabled with the bit BAS_PUP in register GLB_CNFG.

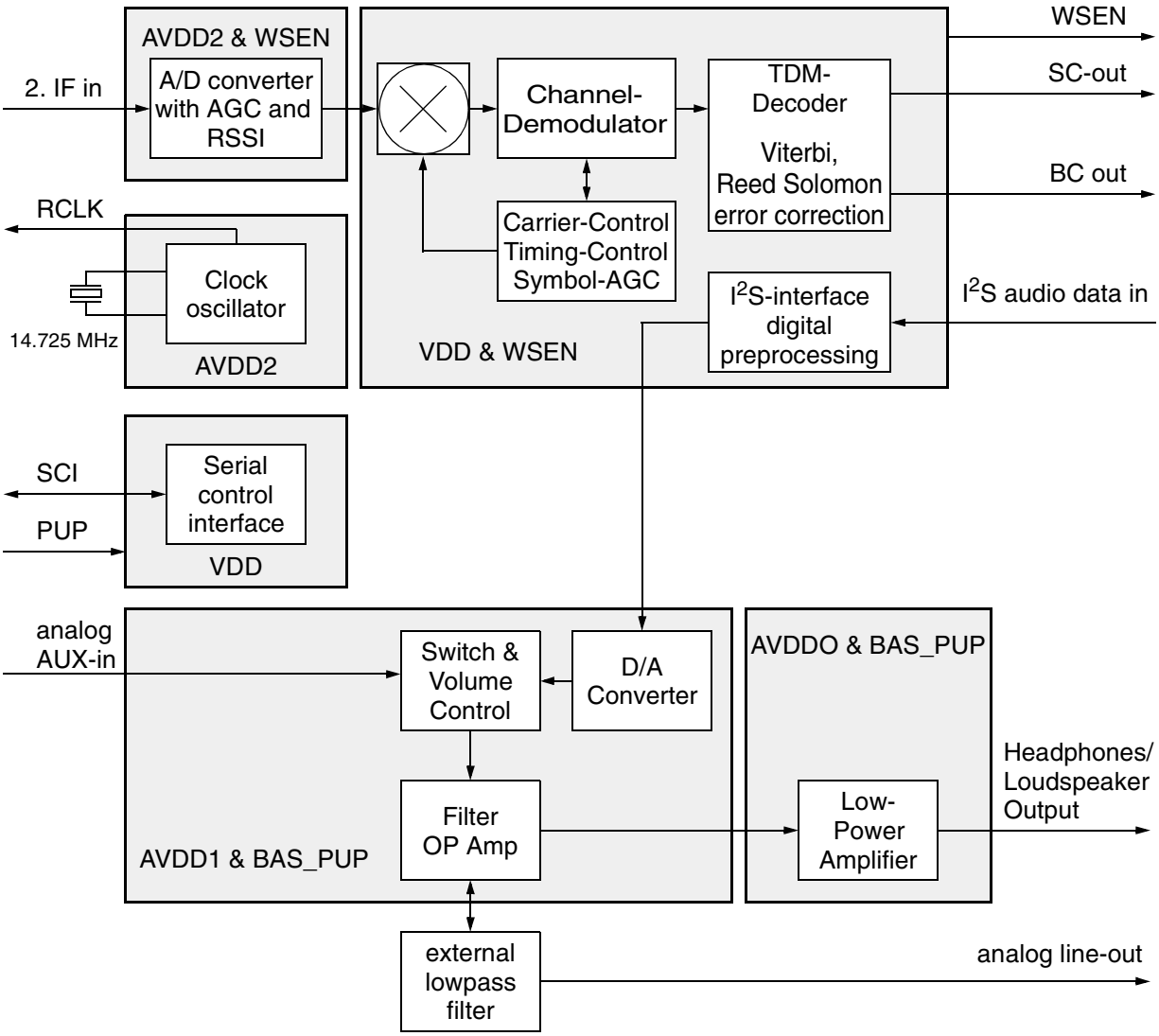

Fig. 2–1: DRD 3515A power supply sections and necessary enabling signals. The PUP signal is required for all sections.

2.4. IF Frontend

The 2nd IF input signal has a carrier frequency of 1.84 MHz and an amplitude between 15 mV and 500 mV. To use the full range of the A/D converter, a digitally controlled analog AGC and a DC offset compensation are used. The gain control leaves enough headroom for very noisy signals with high crestfactors. On the other hand the resolution of the A/D converter is high enough for the second AGC in the digital domain. The gain value of the analog AGC may be read by the micro controller to get the Received Signal Strength Indicator (RSSI, register DMD_AAG_AGC). The time constant of the control is designed to cope with different reception conditions and may be adjusted to situations like manual movement of the receiver or mobile operation.

The gain range of the analog AGC is 31 dB, this will cover all standard reception situations including hand-held, mobile and home operation. In the case of very strong retransmission in the immediate neighborhood an additional AGC regulator should be provided in the L-band tuner circuit. A single 20 dB attenuation step is sufficient for this task. The controller should watch for a continuous IF input overflow via the DMD_AAG_AGC register and could then activate this additional attenuation.

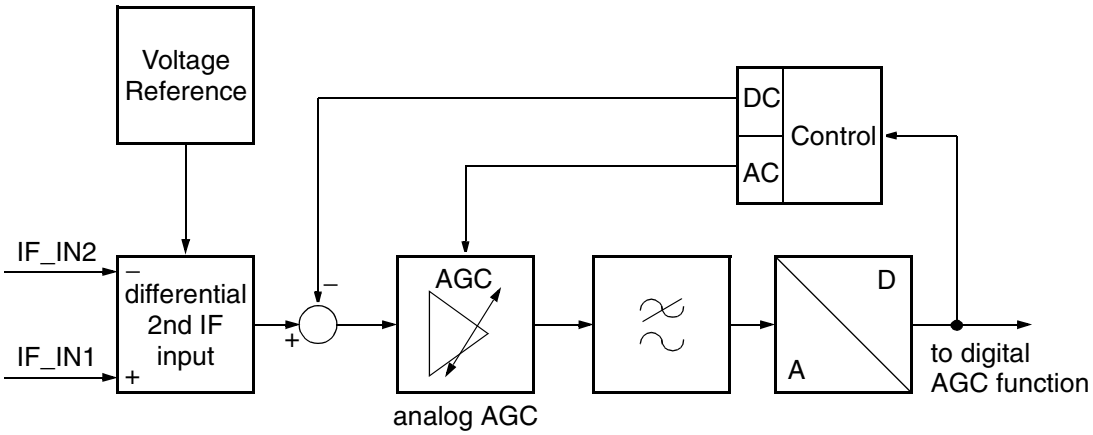

Fig. 2–2: Diagram of IF input section

2.5. QPSK Demodulator

The QPSK demodulator performs a digital I/Q splitting. A carrier frequency tracking loop and a symbol timing recovery loop are used for demodulation. The carrier tracking range covers carrier frequency offsets caused by crystal tolerances. Thus no carrier frequency feedback control to the tuner PLL is required. A second (pure digital) AGC controls the symbol amplitude for an optimal signal mapping for the subsequent error correction blocks. The phase uncertainty of QPSK modulation is compensated by evaluation of the Master Frame Preamble (MFP). The carrier recovery loop is optimized for operation with small C/N ratio. A fixed carrier frequency offset may be sent to the DRD 3515A after reset in order to compensate for a known frequency offset of the crystal. The quality of the QPSK demodulation may be obtained from the register DMD_AGC_RCVQU that displays the I/Q amplitude variance. This signal may be used to optimize the antenna pointing direction. All demodulation and synchronization parameters can be controlled via I^2C bus.

2.6. Frame Synchronization and Demultiplexing

2.6.1. Synchronization to MFP and PRCP

The Master Frame Preamble (MFP) is used to synchronize the decoder to the frame of the incoming bitstream. The MFP-detector block additionally eliminates the 90° phase-ambiguity of the QPSK-signal. The MFP-detector has been designed to cope even with bad reception conditions.

The Prime Rate Channel Preambles (PRCP) identify the beginning of each of the 96 Prime Rate Channels (PRC).

For both the Master Frame Preamble detection and Prime Rate Channel Preamble (PRCP) detection different threshold values can be defined for the unsynchronized and synchronized state.

In order to minimize false alarms in the unsynchronized state the threshold value should be high. In the synchronized state though the threshold value should be lower to minimize misses. In this state false alarms are omitted by a windowing technique that only activates the detection circuit when the next preamble is expected. This technique allows to meet the rigid requirements of the WorldSpace specification.

The MFP/PRCP circuits are “synchronized” upon successful detection of the respective preambles. They return to the “unsynchronized” hunting state upon several misses of the respective preambles
(see Table 4–13 on page 24).

In addition the MFP-detection returns to “unsynchronized” upon writing to register $1B (synched threshold values), the PRCP-detection returns to “unsynchronized” upon writing to one of the 8 TDM-timeslot selection registers.

2.6.2. TSCC Acquisition

After initial synchronization an acquisition of the Time Slot Control Channel (TSCC) should be performed. The TSCC data will be error corrected and made available to the external controller. The TSCC contains information about all Broadcast Channels on the carrier and the time slots of the corresponding Prime Rate Channels (PRC). The TSCC data can be read out by the controller via the FEC data read register (FEC_READ) immediately after they have been decoded. After one TSCC block is received, the DRD 3515A indicates the availability of the TSCC data at the SYNC output pin and in an FEC status register.

The TSCC acquisition is initiated after power-up and may be reinitiated via the FEC_WRITE register at any

time. During TSCC acquisition the normal Broadcast data reception is inhibited (see Section 2.7. on page 9).

2.6.3. TDM Demultiplexing: Selection of Broadcast Channel

Depending on the read TSCC information the controller writes the Prime Rate Channel numbers for the wanted Broadcast Channel in ascending order into the corresponding registers of the DRD 3515A. Also the unused time slots have to be given an unique ID number; however, these unused slots must be disabled. The DRD 3515A must now be switched into the BC mode via register FEC_WRITE. The demultiplexer takes the selected PRC time slots from the TDM data stream and passes their data to the subsequent forward error correction modules i.e. the Viterbi decoder and the Reed Solomon decoder.

The Service Control Header (SCH) is only available from the MAS 3506D.

2.7. Viterbi and Reed-Solomon Decoding

Forward error correction is done by an 1/2-rate Viterbi decoder followed by a Reed-Solomon decoder. These blocks are used either for Broadcast Channel data or for TSCC-data correction. Thus during acquisition of the TSCC normal Broadcast Channel reception is not possible. TSCC acquisition is usually only necessary after power-up. However, the TSCC information (194 bytes) is stored inside of the DRD 3515A and is available to the controller also in the Broadcast mode. This feature reduces the memory requirement for the system controller. The TSCC data will usually change only if the TDM data stream from the satellite is reconfigured.

The Viterbi decoder provides a signal quality information via the FEC_WRITE/READ functions. This information may be used in addition to the RSSI (register DMD_AAG_AGC) or the QPSK demodulation quality (register DMD_AGC_RCVQU) for antenna orientation.

Via a flag accessible through the FEC_WRITE/READ registers the Reed-Solomon decoder indicates whether the error correction was probably successful or failed due to a high input error rate.

2.8. Broadcast Channel Output and Selection of an Additional Service Component

The selected Broadcast Channel is sent via pins BCC and BCD to the MAS 3506D (input pins SIC and SID) for Service Component extraction and MPEG 2 Layer 3 audio decoding. The 2-wire BC-output may also be used by external devices to process Broadcast Channels containing data other than audio.

In addition one Service Component can be selected and activated via the FEC_WRITE command register. It is then sent to the 3 pin SC-output (SCC, SCD, SBCW). The additional word frame indication (SBCW) on the 3rd line simplifies the connection of optional data decoders. This SC output does not influence the selection of the audio Service Component in the MAS 3506D.

2.9. Analog Audio

The backend of the DRD 3515A consists of a digital part that performs the D/A conversion of the WorldSpace audio signal, and an analog part with a signal switch matrix for additional auxiliary analog audio inputs, filter op amps, a line output, and two low power amplifiers for directly driving stereo headphones or a small monoaural loudspeaker, respectively.

A digital input data signal from the MAS 3506D is passed to the D/A converter of the DRD 3515A in a 16 or 32-bit I^2S-format. For high quality audio it is recommended to use the 32-bit mode of the I^2S interface to make use of the full dynamic range provided by the Layer 3 audio transmission.

The D/A-converted signal passes a switch matrix, an analog volume control and a low power amplifier. In addition to the D/A converter, two external stereo signals AUX1 and AUX2 are connected to the switch matrix. The signal path is led over external pins FOUTL/R, FOPL/R and FINL/R to allow external filtering of the analog signals. The FINL/R pins are usable as line outputs (see Section 7.1. on page 48).

The low power amplifier output is provided at the OUT1 and OUT2 pins. If a loudspeaker is connected to these outputs the power amplifier for the right channel must be switched to inverse polarity. In order to optimize the available power the source of the two output amplifiers should be identical, i.e. a monoaural signal.

The stereo headphone requires external 47 Ω serial resistors in both channels.

A power-off mode for zero power consumption and a low power mode with a fast resume of normal operation is available to optimize battery operation. The 5 V option of the audio parts will result in higher output levels and a better S/N ratio.

The principle of the DRD 3515A baseband processing is shown in Figure 2–3 and Figure 2–4.

Audio Baseband Features

- High quality stereo D/A-converter
- 2 auxiliary analog stereo input pairs
- Source selector switch
- Mono switch for aux-input pairs
- Op amp connections accessible for customizable lowpass filtering of the analog audio signals
- Stereo analog volume control with 93 dB volume range and mute function
- Integrated low power stereo amplifier
- Stereo headphone or mono loudspeaker operation
- Single ended operation with 3V or 5V power supply
- Power-down mode with fast resume of normal operation
- Click-reduction for power mode switching

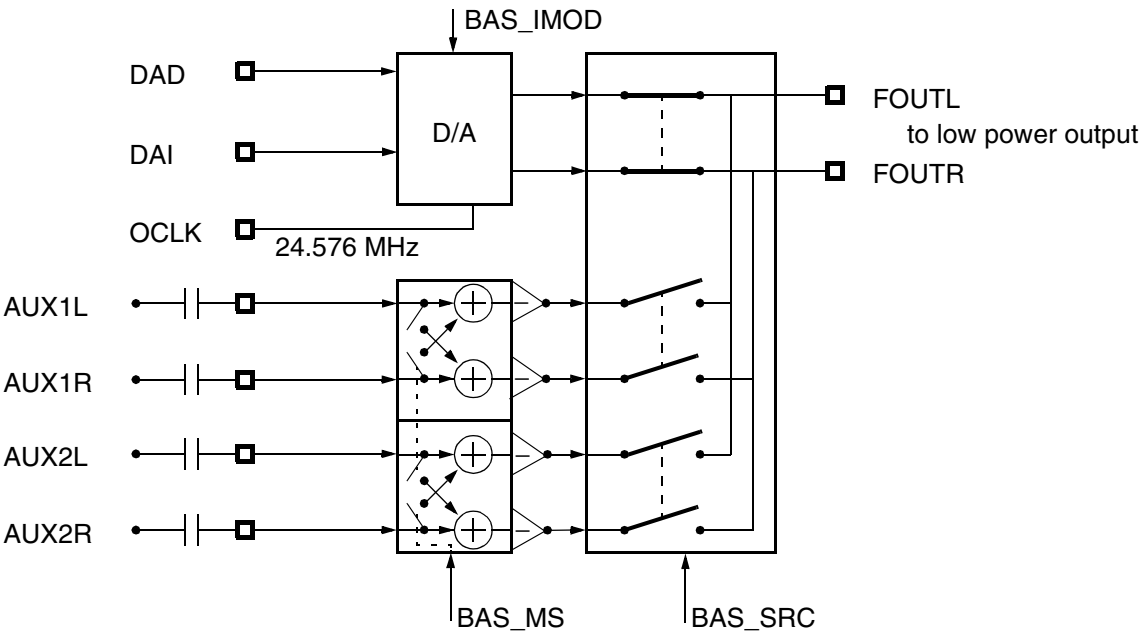

Fig. 2–3: Audio input signal switch matrix

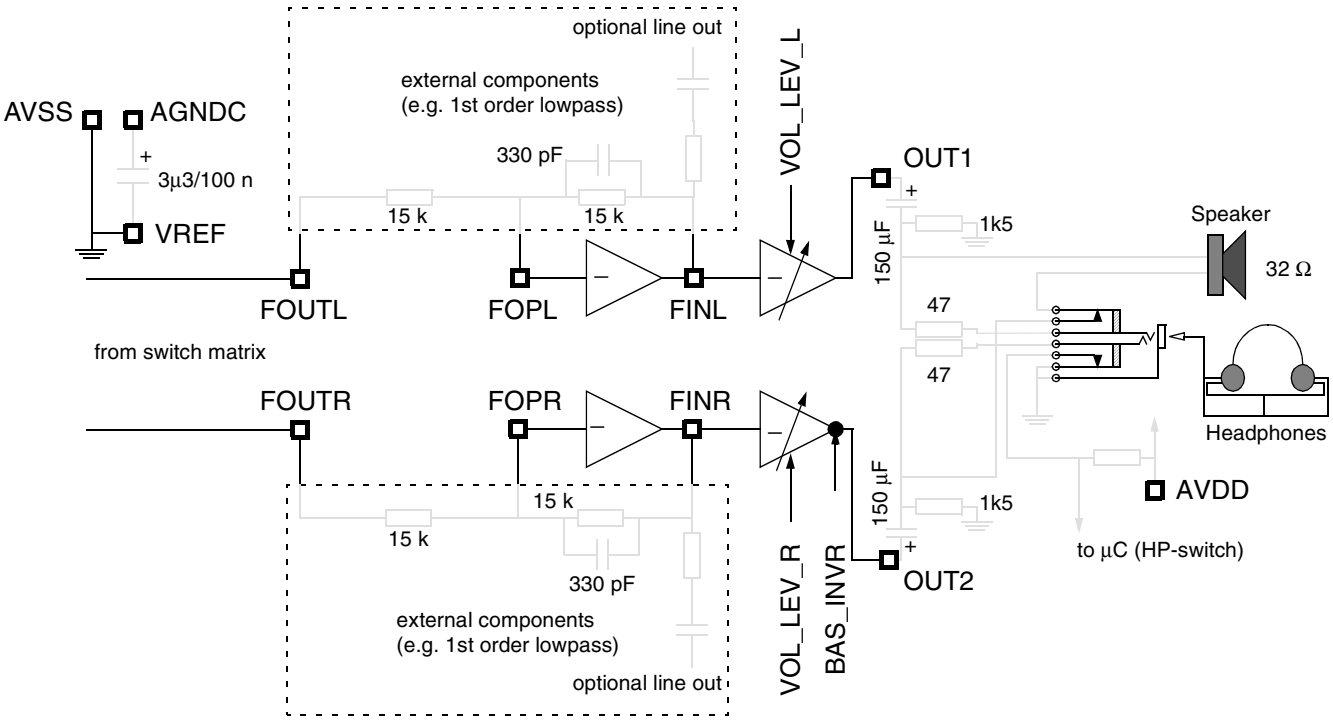

Fig. 2–4: Audio Baseband output amplifiers+

3. Modes of Operation

3.1. Interactions Between DRD 3515A and MAS 3506D

Both ICs, the DRD 3515A and the MAS 3506D are designed for joint operation. Both ICs interact very closely with respect to the system clock, the supply power concept and the corresponding operating modes. In Figure 3–1 a more detailed diagram shows how both chips are to be combined in a standard WorldSpace receiver.

3.2. Clock Concept

The complete chipset is driven by a single crystal at a frequency of 14.725 MHz. The DRD 3515A provides a crystal oscillator (1 in Fig. 3–1) and an appropriate clock buffer. The buffered clock output signal is provided at the RCLK pin. In order to reduce intermodulation with harmonics of the signal, it has a near-sinusoidal shape and a reduced voltage swing. This RCLK signal is also used to drive the digital parts of the tuner and the MAS 3506D. It can be directly connected to its input pin CLKI. In modes, where no MAS 3506D-operation is required, the RCLK signal may be switched off.

Since in the WorldSpace system the rate of the audio or user data channel is not locked to the Master Frame of the satellite (3), the MAS 3506D MPEG audio decoder has an own clock synthesizer which is driven by the DRD 3515A RCLK signal, but frequency-controlled by the data flow of the Broadcast Channel. The synthesizer locks its frequency to a multiple of the incoming BC data; its nominal frequency is 24.576 MHz. The synthesized 24.576 MHz is provided at the OCLK output of the MAS 3506D. This signal will be used as the master clock for the D/A converter in the DRD 3515A (signal 4 in Fig. 3–1).

Although the crystal frequency of 14.725 MHz is no exact submultiple of the L-band receiving frequencies, the selection of appropriate divisors in the PLL will result in a local oscillator frequency with sufficient accuracy (e.g. within 5 or 10 kHz of the target) that by far underbids the expected tolerances of the quartz crystal (50 ppm will result in a deviation of 75 kHz in the L-band).

3.3. Operation and Stand-By Modes

Different stand-by functions allow the operation of only those parts of the IC that are needed. The power concept (see Fig. 2–1 on page 7) of the MICRONAS StarMan chipset has been optimized for minimal power consumption with respect to the various operating modes of the chipset.

3.4. Power Up Sequence (2 Battery Operation)

In the DC/DC converter mode two external batteries with an expected voltage between 1.8 V and 3.0 V are connected to the DCSO pin of the MAS 3506D DC/DC converter via an inductance. The following sequence is executed after power up using the MAS 3506D DC/DC converter.

– The DC/DC converter and the power supervision start their operation upon a DCEN (DC enable) signal at the MAS 3506D.

– Wait for PUP (power up) output of MAS 3506D which indicates that sufficient output voltage is available.

– Activate PUP input signal at the DRD 3515A.

– The controller has to wait until the WRDY (WorldSpace ready) signal of the MAS 3506D is activated. This signal indicates that the MAS 3506D has received a valid clock at the RCLK input, i.e. the crystal oscillator of the DRD 3515A is ramped up.

– Select operating mode by an appropriate I^2C command (e.g. enable WorldSpace operation by setting the bit WSEN in the main configuration register of the DRD 3515A.)

– Enable the audio amplifier output (BAS_PUP = 1) after the specified charging time of the output decoupling capacitors.

3.5. Power Up Sequence (Operation Without DC/DC Converter)

Without the DC/DC converter a voltage between 3.0 V (absolute minimum 2.7 V) and 3.6 V is expected at the appropriate power supply input pins of both ICs. The DCSO input of the DC/DC converter must be connected to ground.

– The voltage supervision starts its operation upon a DCEN (DC enable) signal at the MAS 3506D.

– All other commands are as described in Section 3.4.

It is possible to directly connect the PUP output of the MAS 3506D to the PUP input of the DRD 3515A. However, if more sophisticated tasks are to be performed (e.g. battery voltage measurement with help of the power supervision circuit of the MAS 3506D), it is advised to route this line through the controller.

3.6. Power Down Sequence

– Mute the audio output.
– Switch audio input to DAC (BAS_SRC = 00).
– Switch audio block into “low power mode” (BAS_PUP = 0).
– Disable the PUP pin at the DRD 3515A.
– Disable the DCEN pin at the MAS 3506D.

3.6.1. Full WorldSpace Operation

All digital parts of the DRD 3515A are activated. After the power up sequence, the controller should set the WSEN bit. This will enable the WorldSpace decoder within the DRD 3515A and will validate the WSEN signal pin. This signal should be connected with the corresponding input of the MAS 3506D and with the “enable signals” of the tuner.

WSEN = 1, BAS_PUP = 1.

3.6.2. Audio Amplifier Operation

Only I^2C bus, audio source selector, volume control, audio amplifier and crystal oscillator are active.

All digital functions except the I^2C interface and the crystal oscillator can be powered down by setting WSEN to 0; thus the WorldSpace decoding functions of the DRD 3515A are put to stand-by and the WSEN output pin is forced to 0 which disables the audio decoding function of the MAS 3506D. This feature reduces the power consumption when only the audio amplifier and its co-functions (audio source selector, volume control) are needed to process external analog audio signals.

The audio baseband can additionally be switched into a “stand-by mode” (see Section on page 10).

WSEN = 0, BAS_PUP = 1.

3.6.3. WorldSpace Operation Only

The analog functions (switch, volume control, amplifier) can be powered down by clearing the control bit BAS_PUP. This yields operation of the WorldSpace decoder part up to the Broadcast Channel output.

WSEN = 1, BAS_PUP = 0.

Although the current in the analog parts is reduced considerably, there is some current needed to resume very quickly to normal mode without any clicks.

It is recommended to switch the input source of the analog part to the D/A only while BAS_PUP is 0! Otherwise there would exist an unavoidable path from the AUX-inputs to the outputs.

3.6.4. Off

By deactivating the PUP input signal the complete DRD 3515A is switched into zero power mode.

To avoid an unwanted DC path from the auxiliary audio inputs to the outputs it is recommended to switch the input source of the analog part to D/A (BAS_SRC = 0) before deactivating the PUP pin.

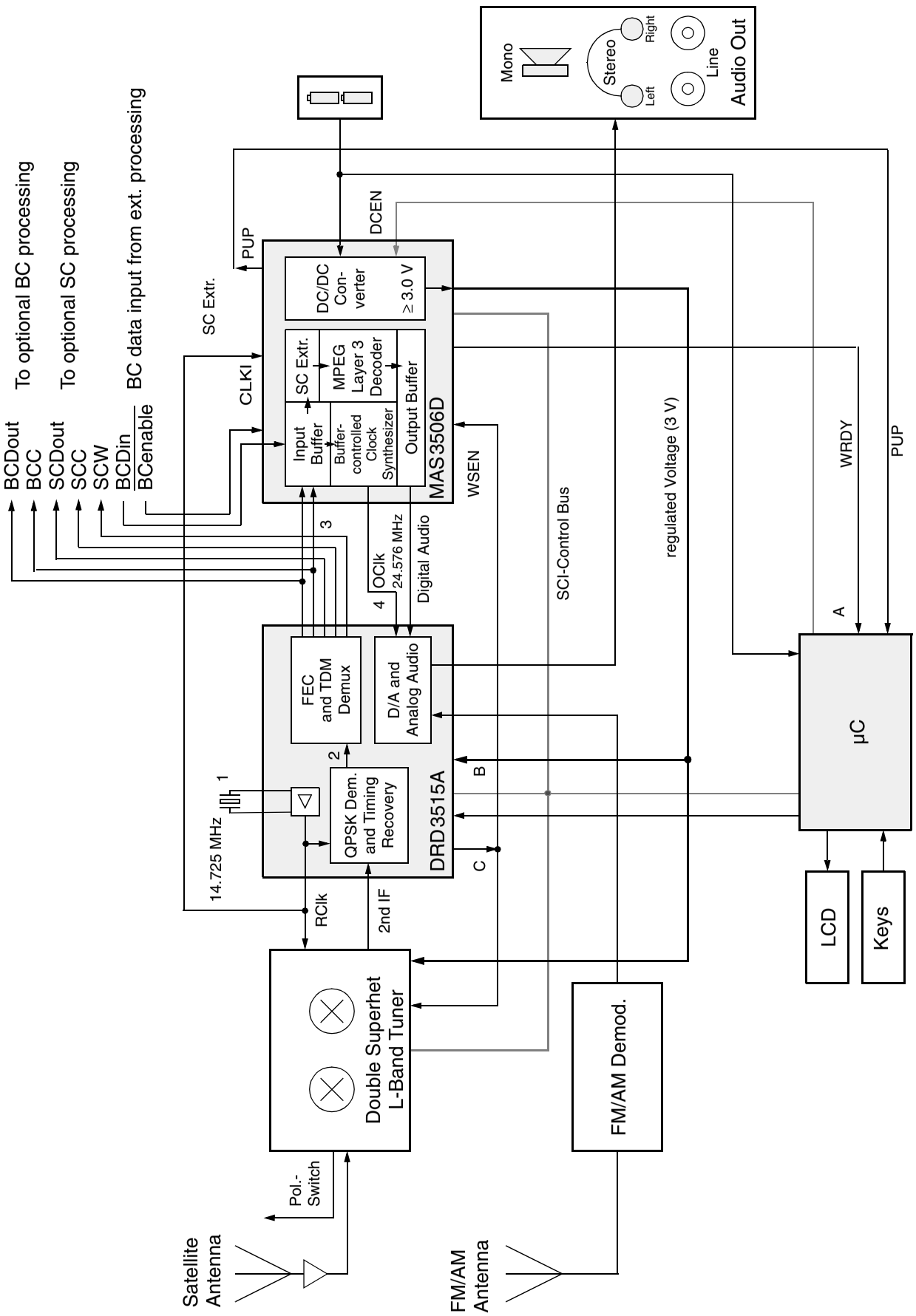

Fig. 3–1: Complete WorldSpace Receiver

4. Serial Control Interface

Communication between the DRD 3515A and the external controller is done via I²C serial control interface.

4.1. I²C-Bus Interface

The DRD 3515A is equipped with an I²C-bus slave interface. It then may use I²C clock synchronization to slow down the interface if required. The I²C-bus interface uses one level of subaddresses: one I²C-bus address is used to address the IC and a subaddress selects one of the internal registers. The I²C-bus chip address is given below.

dev_write = $38
dev_read = $39

Note: The I²C address is subject to change

Table 4–1: Bits of I²C-address

A6	A5	A4	A3	A2	A1	A0	W/R
0	0	1	1	1	0	0	0/1

The registers of the DRD 3515A have 8 or 16-bit data size; 16-bit registers are accessed by reading/writing two 8-bit data words.

Fig. 4–1 shows I²C-bus protocols for read and write operations of the interface; the read operation requires an extra start condition and repetition of the chip address with read command set.

4.2. Register Overview

Table 4–2 gives definitions of the DRD 3515A control and status registers. The number of bits indicated for each register in the table is the number of bits implemented in hardware. Write registers that can be read back are indicated in Table 4–2.

A hardware reset initializes all control registers to 0. The automatic chip initialization after power on reset or a positive edge at the PUP pin loads a selected set of registers with the default values given in Table 4–2.

The register modes given in Table 4–2 are

w write only register
r/w read/write data register
r read data from DRD 3515A

The mnemonics used in the Micronas DRD 3515A demo software are given in the last column.

Example: 16-bit I2C write access

S	dev_write	A	subaddress	A	high byte data	A	
					low byte data	A	P

Example: 8-bit I²C read access

S	dev_write	W	A	subaddress	A	S	dev_read	A	low byte data	N	P

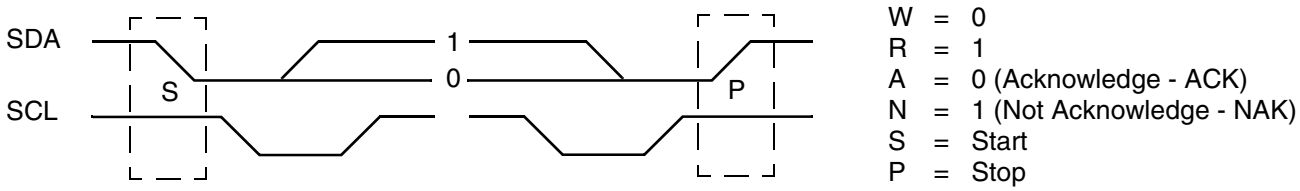

Fig. 4–1: I²C-Bus protocol

The following abbreviations have been used within register names and register bits.

GLB_	Global configuration
DMD_	IF input and QPSK demodulator
TDM_	Time division demultiplexer
FEC_	Viterbi and Reed Solomon forward error correction
BAS_	Analog audio baseband
AAG	Analog AGC
AGC	Automatic gain control
AMP	Amplifier
_BAS	Analog audio baseband
CLK	Clock
CNFG	Configuration
CNT	Count
COEF	Coefficient
_CR_	Carrier recovery
CYIN	Carry input
DIS	Disable
_EN_	Enable
EQU	Equal
_FB_	Feedback
LFSR	Pseudo-Random-Generator
MFP	Master Frame Preamble
_PR_	Phase recovery
PRC	Prime Rate Channel
PUP	Power up
SELF	Self test
_TH_	Threshold
_TR_	Timing recovery
_TS_	Time slot

Table 4–2: Register List

I^2C Sub-address (hex)	No of bits	R/W	Function	Default/ Target values (hex)	Name
GLOBAL CONFIGURATION GLB					
01	8	w	global configuration	0	GLB_CONFIG
			bit[7] WorldSpace mode enable	0	WSEN
			bit[6] select 5 V mode 0 = 3.3 V, 1 = 5 V	0	SEL5V
			bit[5] I^2S word length 0 = 16 bit, 1 = 32 bit	0	SI_IMOD
			bit[4] audio power 0 = low power, 1 = operation	0	BAS_PUP
			bit[3,2] input sel. 0 = D/A, 1 = AUX1, 2 = N/A, 3 = AUX2	0	BAS_SRC
			bit[1] mono/stereo for AUX inputs 0 = stereo, 1 = mono	0	BAS_MS
			bit[0] invert right power amplifier	0	BAS_INVR
IF INPUT SECTION DMD					
2E	8	w	analog AGC configuration	19	DMD_AAG_CNFG
			bit [7] reserved bit, keep ‘0‘	0	
			bit [6] reserved bit, keep ’0’	0	
			bit [5] reserved bit, keep ‘0‘	0	
			bit [4] input DC control loop enable	1	AAG_DC_EN
			bit [3] AGC control loop enable	1	AAG_AGC_EN
			bit [2:0] AGC time constant	1	AAG_PARA_KI
2F	8	r/w	bit [4:0] analog AGC amplification set/return (target)	16	DMD_AAG_AGC

Table 4–2: Register List

I²C Sub-address (hex)	No of bits	R/W	Function	Default/ Target values (hex)	Name
QPSK DEMODULATOR DMD					
20	8	r/w	carrier frequency offset (target)	0	DMD_CR_F
26	8	r	receiving quality (average I/Q amplitude variance) bit[7:4] receiving quality (target) bit[3:0] AGC-gain (target)	2 0 2	DMD_AGC_RCVQU RCVQU AGC_GAIN
28	8	r/w	timing recovery symbol time (target)	0	DMD_TR_TS
TDM_DEMULTIPLEXER TDM					
11	8	r/w	TDM time slot 1 bit [7] time slot 1 enable bit [6:0] time slot 1 channel ID (PRC number <1 ... 96>)	81 1 1	TDM_T_SLOT_1 TS_EN PRC
12	8	r/w	TDM time slot 2 bit [7] time slot 2 enable bit [6:0] time slot 2 channel ID (PRC number)	3 0 3	TDM_T_SLOT_2 TS_EN PRC
13	8	r/w	TDM time slot 3 bit [7] time slot 3 enable bit [6:0] time slot 3 channel ID (PRC number)	5 0 5	TDM_T_SLOT_3 TS_EN PRC
14	8	r/w	TDM time slot 4 bit [7] time slot 4 enable bit [6:0] time slot 4 channel ID (PRC number)	7 0 7	TDM_T_SLOT_4 TS_EN PRC
15	8	r/w	TDM time slot 5 bit [7] time slot 5 enable bit [6:0] time slot 5 channel ID (PRC number)	9 0 9	TDM_T_SLOT_5 TS_EN PRC
16	8	r/w	TDM time slot 6 bit [7] time slot 6 enable bit [6:0] time slot 6 channel ID (PRC number)	B 0 B	TDM_T_SLOT_6 TS_EN PRC
17	8	r/w	TDM time slot 7 bit [7] time slot 7 enable bit [6:0] time slot 7 channel ID (PRC number)	D 0 D	TDM_T_SLOT_7 TS_EN PRC
18	8	r/w	TDM time slot 8 bit [7] time slot 8 enable bit [6:0] time slot 8 channel ID (PRC number)	F 0 F	TDM_T_SLOT_8 TS_EN PRC
FORWARD ERROR CORRECTION FEC					
30	8	w	FEC command and data write register		FEC_WRITE
31	8	r	FEC data read register	0	FEC_READ

Table 4–2: Register List

I²C Sub-address (hex)	No of bits	R/W	Function	Default/ Target values (hex)	Name
ANALOG BASEBAND AUDIO BAS					
40	16	w	audio volume control bit [15] set to '0' bit [14] Disable RCLK bit [13:8] analog audio volume level left: 0 = mute; 1 = –75 dB; $2C_h$ = 0 dB, 38_h = +18 dB bit [7:6] set to '0' bit [5:0] analog audio volume level right 0 = mute; 1 = –75 dB; $2C_h$ = 0 dB, 38_h = +18 dB	0 0 0 0 0 0 0	BAS_AUDIO RCLK_OFF VOL_LEV_L VOL_LEV_R

4.3. Detailed Description of the Registers

4.3.1. Main Configuration Register GLB_CONFIG

The main configuration register GLB_CONFIG is used to enable/disable WorldSpace operation, different power modes and to control the analog audio back-end.

Table 4–3: GLB_CONFIG register ($01, write)

Bits	Signal	Comment
[7] Reset = 0	WSEN 0 1	WorldSpace enable disable WorldSpace enable WorldSpace
[6] Reset = 0	SEL5V 0 1	select 5 V mode for the audio blocks 3.3 Volt mode 5 Volt mode
[5] Reset = 0	SI_IMOD 0 1	I²S word length 16 bits 32 bits
[4] Reset = 0	BAS_PUP 0 1	power for audio low power stand by normal operation
[3,2] Reset = 0	BAS_SRC 0 1 2 3	audio input selector DAC AUX1 N/A Aux2
[1] Reset = 0	BAS_MS 0 1	mono/stereo for AUX stereo mono
[0] Reset = 0	BAS_INVR 0 1	invert right audio channel off on

– WSEN
If set, the WorldSpace mode of the DRD 3515A is enabled and the WSEN signal is activated at the output. Disabling this bit powers down all digital parts that are used exclusively for WorldSpace decoding.

– SEL5V
The SEL5V signal switches the internal bandgap reference voltage. In normal mode (SEL5V = 0) a power supply voltage of 3 V is expected for $VSUP_A$ (pins AVDD0/1) and the bandgap reference is switched to 1.5 V. If SEL5V = 1, a minimal power supply voltage of 4.5 V is expected for $VSUP_A$ (pins AVDD0/1) and the bandgap reference voltage is switched to 2.25 V. In the latter mode the signal level is increased by a factor of 1.5 (3.5 dB).

– SI_IMOD
The IMOD bit configures the I²S digital audio interface for different digital word lengths. In default mode, a word length of 16 bits/sample is expected. However, if additionally an external DAC is connected to the I²S output signal of the MAS 3506D, the full MPEG audio data resolution may be required. In this case the MAS 3506D will generate 32-bit samples. The special structure of the DRD 3515A digital input interface that uses only 2 input lines needs this additional information about the I²S word length.

– BAS_PUP
The BAS_PUP bit enables full operation of the analog baseband processing. If the BAS_PUP bit is cleared the analog baseband processing is switched into the low power stand by mode: The analog output is muted and the power consumption of the analog backend is reduced considerably. However, some parts are still working to provide a very fast resume of the full operation with minimum click.

– BAS_SRC
The BAS_SRC bits select the DAC or one of the

AUX1/AUX2 input lines as shown in Fig. 2–3.

– BAS_MS
In normal operating mode stereo signals are expected. However, monoaural output may be required e.g. to optimize the output power of a single loudspeaker. If AUX signals are selected, they can be converted to a monoaural signal by setting the BAS_MS bit. The BAS_MS bit setting also affects the line output signal at FINL/R (see Fig. 2–3 on page 10).
For the D/A converter signal the mono conversion must be performed in the digital domain, i.e. in the MPEG audio decoder.

– BAS_INVR
The power amplifier for the right channel will be switched to inverted polarity by setting this bit. The inversion is required if a single loudspeaker is connected to the OUT1 and OUT2 pins. In this case the output amplifiers work in bridge mode to allow maximum difference voltage swing (see Fig. 2–4 on page 11).

4.3.2. IF Input Configuration

Table 4–4: DMD_AAG_CNFG ($2E, write)

Bits	Signal	Comment
[4] Reset = 1	AAG_DC_EN 0 1	IF input DC control loop enable (see Fig. 2–2) disable AGC DC loop enable AGC DC loop
[3] Reset = 1	AAG_AGC_EN 0 1	IF input AGC enable disable AGC function enable AGC function
[2..0] Reset = 1	AAG_PARA_KI 0 1 2 3 4 5 6 7	AGC time constant 4.48 ms/dB 2.24 ms/dB 1.12 ms/dB 1.25 ms/dB 0.58 ms/dB 0.28 ms/dB 0.07 ms/dB 0.04 ms/dB

– AAG_DC_EN
The AAG_DC_EN bit enables or disables the automatic DC compensation (see Figure 2–2).

– AAG_AGC_EN
The AAG_AGC_EN bit enables or disables the automatic gain control.

– AAG_PARA_KI
By setting AAG_PARA_KI time constant register, the reaction of the AGC with respect to level changes of the IF-input signal can be modified. This is a useful option for adjusting the behavior to different reception environments.

4.3.3. IF Input: Analog Automatic Gain Control

Table 4–5: DMD_AAG_AGC register ($2F, read/write)

Bits	Signal	Comment
[4..0] Reset = 0	DMD_AAG _AGC 0 1 ... 30 31	read/write 0 dB gain 1 dB gain 30 dB gain 31 dB gain

– DMD_AAG_AGC
If the AAG_AGC_EN bit is enabled, reading DMD_AAG_AGC returns a value that is inversely proportional to the signal strength of the IF input signal. If the AAG_AGC_EN bit is cleared, reading DMD_AAG_AGC returns the default value or the value that has been written previously. Writing to the DMD_AAG_AGC register is only of duration if the AAG_AGC_EN bit is set to 0.

4.3.4. QPSK Demodulator Carrier Frequency Offset

Table 4–6: DMD_CR_F register ($20, read/write)

Bits	Signal	Comment
[7..0] Reset = 0	DMD_CR_F –128 –127 .. 0 .. 126 127	read/write IF frequency deviation –115 kHz –114 kHz 0 kHz 113 kHz 114 kHz

– The DMD_CR_F sets/returns the actual input carrier frequency relative to the nominal IF-center frequency of 1.840 MHz. After synchronization to a WorldSpace channel, this register reflects a value that depends on the actual frequency deviation due to the accuracy and stability of the 14.725 MHz crystal and that of the tuner reference. This value can be stored into a non-volatile controller memory and rewritten to the DMD_CR_F register after power-up or re synchronization. This measure will considerably speed up carrier and timing synchronization for noisy channels. Reading the DMD_CR_F register in the power-down cycle and rewriting it with the same value in the power-up cycle will help the digital carrier frequency recovery to find the satellite signal.

4.3.4.1. QPSK Demodulator Receiving Quality Indicator

Table 4–7: DMD_AGC_RCVQU register ($26, read)

Bits	Signal	Comment
[7:4]	RCVQU	receiving quality (C/N)
	0 1 2 3 4 5 6 7 8 9 10 ... 15	40 dB 20 dB 17 dB 14 dB 12 dB 11 dB 9 dB 7 dB 6 dB 4 dB below threshold
[3:0]	AGC_GAIN	gain of digital AGC
	0 1 2 .. 15	not allowed Gain = 1/4 Gain = 2/4 Gain = 15/4

– The 4 MSBs of the register return the receiving quality indicated by the average I/Q amplitude variance as detected by the QPSK demodulator. The values of Table 4–19 on page 27 depend on the amplitude target of the digital AGC (AGC_GAIN).

The values read out by the receiving quality evaluation are only meaningful, if the digital AGC is not in saturation.

– The 4 LSBs of the register return the actual gain of the QPSK demodulator´s digital AGC and phase recovery control.

4.3.5. QPSK Demodulator Timing Recovery Symbol Time.

Table 4–8: DMD_TR_TS register ($28, read/write)

Bits	Signal	Comment
[7:0] Reset = 0	DMD_TR_TS	$f_{symb\text{-}crystal}$ - $f_{symb\text{-}recv}$
-105_d ... -1 0 1 ... 105		–184 Hz ... –1.75 Hz 0 Hz 1.75 Hz 184 Hz

– The DMD_TR_TS sets/returns the internal symbol timing standard offset that locks on the symbol timing of the incoming data stream which is nominally 1.84 MHz. After synchronization to a WorldSpace channel, this register reflects a value that depends on the actual frequency deviation due to the accuracy and stability of the 14.725 MHz crystal. This value can be stored into a non-volatile controller memory and rewritten to the DMD_TR_TS register after power-up or re synchronization. This measure will considerably speed up timing synchronization especially for noisy channels. Values should not exceed the range given above.

– TDM Time Slot Registers.

Table 4–9: TDM_T_SLOT_n ($12 ... $18, write)

Bits	Signal	Comment
[7] Reset = 0 (Reset = 1 for register 11)	TS_EN	enable time slot n
[6:0] Different reset values	PRC	Prime Rate Channel ID number <1 ... 96>

– A requested Broadcast Channel may consist of 1 or more (up to 8) Prime Rate Channels. The according PRC ID numbers are documented in the TSCC information.

– The PRC numbers for the requested Broadcast Channel must be deposited in the lowest TDM_T_SLOT registers in ascending order. These time slots must be enabled by setting bit TS_EN.

– If the BC consists of less than 8 PRCs the controller must also deposit Prime Rate Channel numbers to **all** unused TDM_T_SLOT registers as well. These PRC numbers must be unique (one number must only occur once) and different from those used to build the requested BC. Unused TDM_T_SLOT registers must be disabled (i.e. TS_EN = 0).

– Writing to one of the TDM_T_SLOT registers will set the PRC preamble detection algorithm to the “unsynched” state (see Table 4–13 on page 24). During normal reception these registers must not be written.

4.3.6. Analog Audio Gain

Table 4–10: BAS_AUDIO ($40, write)

Bits	Signal	Comment
[14]	RCLK_OFF 0 1	disable RCLK RCLK available RCLK disabled
[13:8] Reset = 0	VOL_LEV_L 0 1 2 ... 7 8 9 ... 44 45 ... 55 56	Analog volume left Mute –75.0 dB –72.0 dB ... –57.0 dB –54.0 dB –52.5 dB ... 0.0 dB +1.5 dB ... +16.5 dB +18.0 dB
[5:0] Reset = 0	VOL_LEV_R 0 1 2 ... 7 8 9 ... 44 45 ... 55 56	Analog volume right Mute –75.0 dB –72.0 dB ... –57.0 dB –54.0 dB –52.5 dB ... 0.0 dB +1.5 dB ... +16.5 dB +18.0 dB

– RCLK_OFF is used to disable the RCLK output signal.

– VOL_LEV_L/R bits are used to control the volumes of the audio amplifiers. For loudspeaker operation the amplification of both channels must be equal.

– For best loudspeaker performance it is recommended (but not mandatory) to use a mono audio source by either selecting the proper audio matrix mixing coefficients in the MAS 3506D or by setting the BAS_MS bit in the GLB_CONFIG register for AUX input sources. Note that the line outputs will also be affected by these settings.

4.4. Registers for Advanced Features

The following registers are only needed for advanced features such as adjusting the demodulation parameters to special situations (e.g. car radio) or different than the recommended hardware configuration (e.g. 2nd IF spectrum not mirrored). The use of these registers is not needed for normal WorldSpace operation and thus they should normally be left at their default values.

Table 4–11: Register list for advanced features

I²C Sub-address (hex)	No of bits	R/W	Function	Default/ Target values (hex)	Name
IF INPUT SECTION DMD					
2D	8	r/w	DC value of digitized input signal (target)	0	DMD_AAG_DC
QPSK DEMODULATOR DMD					
21	8	r/w	carrier recovery amplitude validation threshold	41	DMD_CR_A_TH
22	8	r/w	phase validation threshold	52	DMD_CR_P_TH
			bit [7:6] Viterbi gain	1	PR_VGAIN
			bit [5:0] phase threshold	12	CR_P_TH
23	8	r/w	frequency validation threshold	0C	DMD_CR_F_TH
			bit [7] TWTA compensation bit 0 (LSB)	0	TWTA_COMP_0
			bit [6] spectrum of IF input signal not mirrored	0	PR_CONJ
			bit [5:0] frequency threshold	0C	CR_F_TH
24	8	r/w	carrier and phase recovery control	AC	DMD_CR_PARA
			bit [7] select downsampling in MTA filter between 8 and 4	1	CR_PARA_4
			bit [6] TWTA compensation bit 1	0	TWTA_COMP_1
			bit [5:3] frequency control loop	5	CR_PARA_F
			bit [2:0] I-part of phase recovery control loop	4	CR_PARA_P_KI
25	8	r/w	amplitude target of digital AGC	4B	DMD_AGC_A_TGT
27	8	r/w	digital AGC and phase recovery control	2C	DMD_AGC_PARA
			bit [7] TWTA compensation bit 2 (MSB)	0	TWTA_COMP_2
			bit [6] select downsampling in MTA filter between 64 and 32	0	AGC_PARA_32
			bit [5:3] I-part of digital AGC control loop	5	AGC_PARA_A
			bit [2:0] P-part of phase recovery control loop	3	CR_PARA_P_KP
29	8	w	timing recovery control	19	DMD_TR_PARA
			bit [6] select downsampling in MTA filter between 16 and 8	0	TR_PARA_8
			bit [5:3] P-part of timing recovery control loop	3	TR_PARA_TS_KP
			bit [2:0] I-part of timing recovery control loop	1	TR_PARA_TS_KI
TDM_DEMULTIPLEXER TDM					
19	16	w	TDM synchronization unsynched threshold values	4C27	TDM_TH_USYNC
			bit [15] set to ‘0‘	0	
			bit [14:8] Master Frame Preamble (MFP) threshold (in unsynchronized state)	4C	MFP_TH_USYNC
			bit [7] set to ‘0‘	0	
			bit [6] set to ‘0‘	0	
			bit [5:0] Prime Rate Channel (PRC) preamble threshold (in unsynchronized state)	27	PRC_TH_USYNC

Table 4–11: Register list for advanced features

I²C Sub-address (hex)	No of bits	R/W	Function	Default/ Target values (hex)	Name
1B	16	w	TDM synchronization synched threshold values	4021	TDM_TH_SYNC
			bit [14:8] Master Frame Preamble (MFP) threshold in synchronized state	40	MFP_TH_SYNC
			bit [5:0] Prime Rate Channel (PRC) preamble threshold in synchronized state	21	PRC_TH_SYNC

4.5. FEC Registers

The FEC Data Read and Write registers have a different functionality in the register space of the DRD 3515A. The FEC registers give access to all function of the internal FEC-processor that performs the error correcting tasks (i.e. Viterbi decoding and Reed-Solomon decoding). Some additional tasks like ES1 decryption and Time Slot Control Channel (TSCC) decoding are also done by this processor. It is controlled by using a special command syntax. These I²C commands allow the micro controller to access internal states, RAM contents and hidden internal hardware control registers. The following commands are supported by the DRD 3515A.

Table 4–12: Basic FEC controller commands

Code	Command	Comment
$4x	idle mode	select idle mode
$6x	TSCC mode	switch into TSCC mode
$7x	BC-mode	switch into BC-mode
$8x	Mem-Read	read from internal memory
$Cx	Mem-Write	write to internal memory

The FEC data register control interface is also used for low bit rate data transmission, i.e. the transfer of TSCC data. The synchronization between controller and DRD 3515A will be initiated by the signal on the SYNC pin or by monitoring the status (at the cost of a higher work load for the controller).

The DRD 3515A embedded processor scans the FEC register periodically and checks for pending or new commands. However, due to some time critical firmware parts a certain latency time for the response has to be expected.

4.5.1. Conventions for the Command Description

The description of the various commands use the following formalism:

– A data value is split into 4-bit nibbles which are numbered beginning with 0 for the least significant nibble.

– Data values in nibbles are always shown in hexadecimal notation indicated by a preceding “$”.

– A hexadecimal 16-bit number d is written e.g. as d = $7C63, its four nibbles are:
d3 = $7, d2 = $C, d1 = $6, d0 = $3

– **Abbreviations** used in the following descriptions

a address
d data value
n byte count value
o offset value
x don’t care

S Start (please see Figure 4–1)
A Acknowledge
N Not acknowledge
P Stop

dev_write $38
dev_read $39

FEC_WRITE $30 (these addresses are listed
FEC_READ $31 in Table 4–2 on page 16)

4.5.2. Detailed DRD 3515A Command Syntax

4.5.2.1. Idle Mode

S	dev_write	A	FEC_WRITE	A	**4,0**	A	P

Switch DRD 3515A into idle mode. In idle mode neither BC decoding nor TSCC decoding is performed and the DRD 3515A will generate no output at the Broadcast Channel or Service Component output pins.

4.5.2.2. TSCC Mode

S	dev_write	A	FEC_WRITE	A	**6,0**	A	P

Switch DRD 3515A into TSCC mode. In TSCC mode no BC decoding is performed and the DRD 3515A will generate no output at the Broadcast Channel or Service Component output pins. The TSCC-data of the Broadcast Channel are extracted and stored for readout by the controller (Section 4.5.4.6. on page 27). After having decoded the TSCC-data successfully the DRD 3515A will indicate this via the SYNC signal and switch into idle mode.

The TSCC mode is the default mode of the DRD 3515A after power-on reset.

4.5.2.3. BC Mode

S	dev_write	A	FEC_WRITE	A	**7,0**	A	P

Switch DRD 3515A into BC mode. In BC mode Broadcast Channel decoding is performed and the DRD 3515A will generate output at the Broadcast Channel output pins and - if an SC is selected - also at the Service Component output pins. Before switching into BC-mode the TDM_T_SLOT registers should be written accordingly. In BC mode the SYNC signal indicates that a new SCH has been detected. This signal may be used for calculation of decryption keys.

4.5.2.4. MEM Read

This command is e.g. required for reading the TSCC data.

S	dev_write	A	FEC_WRITE	A	**8**,a2	A	a1,a0	A	
							n1,n0	A	P

S	dev_write	A	FEC_READ	A	S	dev_read	A
						d1,d0	A

...repeat for n-1 data values...

n1,n0	N	P

Read data starting at address **a** = (a2,a1,a0) from the internal memory of the DRD 3515A FEC-processor.

For the exact procedure to read the TSCC-data please refer to Section 4.5.4.6. on page 27.

4.5.2.5. MEM Write

S	dev_write	A	FEC_WRITE	A	**C**,a2	A	a1,a0
						A	n1,n0
						A	d1,d0

...repeat for n-1 data values...

A	d1,d0	A	P

Write data starting at address **a** = (a2,a1,a0) to the internal memory of the DRD 3515A FEC-processor.

4.5.2.6. Default Read

S	dev_write	A	FEC_READ	A	S	dev_read	d1,d0	N	P

The Default Read command immediately returns the content of the main status register of the DRD 3515A in the variable **d** = (d1,d0). The Default Read is the fastest way to get information from the DRD 3515A and may be used for polling of the FEC-processor status.

Table 4–13: Main Status Register

Bits	Name	Comment	Valid
7	TSCC	TSCC data available	Cleared when entering TSCC mode
6	SyncA	MFP detected, MFP detection circuit is now in “synched” state^	
5	RecOK	All Prime Rate Channels for selected BC have been detected, PRCP detection circuit is now in “synched” state	BC Frame (432 ms)
4	RSE	Reed-Solomon error (at least one RS word with more than 16 errors in one BC Frame)	BC Frame (432 ms)
3	SCHE	SCH not properly detected	PRC Frame (432 ms)

Table 4–13: Main Status Register

Bits	Name	Comment	Valid
2	SYNC	SYNC pin status, reflects the level of the SYNC pin (active high). In TSCC mode it indicates that new TSCC data are available. In BC mode it indicates that new encryption information is available.	TSCC: Static BC: Pulse of 25 ms (8 PRCs in BC) up to 200 ms (1PRC in BC)
1,0	Indx	Modulo index counter is incremented every BC Frame (432 ms)	

4.5.3. Memory Table

The memory areas displayed in the following table can be read and written via I^2C commands.

Important note! Writing into undocumented memory cells is possible but it is highly recommended not to do so. It may damage the function of the FEC-processor and may even lead to a complete system crash of the decoder operation which can only be restored by a reset.

Table 4–14: FEC-Memory Table

Address	Size (Bytes)	R/W	Function	Validity	Name
$00f	1	W	Extended mute function	BC	Mute
$014	1	W	Test settings for bit error rate measurement	BC	BERTest
$015	1	R	Minimal Distance of Viterbi decoder	BC	VMinDist
$01a	1	W	Selects Service Component for the SC output of the DRD 3515A	BC	SC
$13e..$1ff	194	R	TSCC data of selected TDM	always	TSCCInfo
$200	1	W	User's Decryption Hierarchy	BC	SCRank
$202, $203	2	R	Reed-Solomon error accumulator	MSB of $203=1	RSError

Table 4–15: Validity Region for FEC memory cells

Name	Validity
always	The contents of this memory cells can always be read out and will return valid numbers.
BC	Always valid in BC mode. Information that is transmitted in the SCH will be updated every 432 ms indicated by the signal on the SYNC pin. **Note:** In TSCC mode, the writable configuration cells (e.g. EM, PIW0,...) will be reset to their default values or cleared and have to be restored after entering the BC-mode.
BC(1)	Signal valid 400 ms after rising edge of SYNC impulse.
BC(2)	Must be written within 400 ms after rising edge of SYNC impulse.
SYNC	Only readable when SYNC signal is active.

4.5.4. Standard Memory Cells

4.5.4.1. Mute

A special extended mute algorithm has been designed that substitutes the data of the BC-output with a dummy output stream if the Reed-Solomon decoder cannot correct the data block. This dummy output causes the MPEG audio decoder to mute. The Service Component output of the DRD 3515A is not affected.

The extended mute function shall be enabled in situations when no corrupted audio output is tolerated. For maximum intelligibility of the audio signal (e.g. for noisy channels) the extended mute function may be switched off.

This extended mute function can be disabled by setting the MSB of location $00f.

Table 4–16: Extended mute function ($00f)

Bits	Signal	Comment
[7]	Ex_Mute_Off	default 0
	0 1	extended mute enabled extended mute disabled

4.5.4.2. Test Mode for BER Measurements

For bit error rate measurements the Reed-Solomon decoder and its related functions can be switched off. These functions are especially useful with the BER measurement download software for the MAS 3506D.

Table 4–17: BERTest ($014)

Bits	Signal	Comment
[6]	RSoff	Test Mode 1
[5]	FECoff	Test mode 2
[4]	SCtoBC	Test mode 3

In test mode 1 the Reed-Solomon decoder is switched off. BC descrambling and decryption remain active. Normal BC mode is recovered by clearing this bit.

In test mode 2 all functions of the FEC processor are switched off, i.e. Reed-Solomon, descrambling and decryption are inactive. In this mode the output of the Viterbi decoder is directly sent to the BC output pins. In the Main Status Register (default read) updates are only performed on bit 6 (SyncA) and bit 5 (RecOK). Normal BC mode is recovered by clearing the bit and then issuing a “BC mode” command as described in Section 4.5.2.3. on page 24.

In test mode 3 the selected Service Component is not only sent to the SC output but also to the BC output. Normal BC mode is recovered by clearing this bit.

Test modes 1 and 3 may be combined while test mode 2 must not be selected together with any other test mode.

4.5.4.3. VMinDist

The Viterbi Minimal Distance is a highly reliable information about the received signal quality near the signal threshold level. The VMinDist cells are only valid in BC-mode. The Viterbi Minimal Distance is evaluated during the decoding process of the Viterbi decoder.

Table 4–18: VMinDist ($015)

Bits	Signal	Comment
[7..0]	VMinDist	Viterbi Minimal Distance (MSBs)

The distances of each incoming symbol bit to the nearest decision symbol bit are added.

The numerical value of the Viterbi Minimal Distance depends on the target value of the QPSK-symbol AGC (DMD_AGC_A_TGT register $25) and the VGAIN setting in the QPSK demodulator. With the chosen default values for the target value, a PR_VGAIN (in DMD_CR_P_TH register $22) of 2 and noise free input signals, the optimal value of 56 will be displayed in memory cell $15.

If noise is added to the signal, the TDM_I and TDM_Q signals will deviate from the two bit decision values and thus increase the VMinDist value.

The expected range for the Viterbi Mindistance in register $15 is:

- optimal theoretical value: 56
- good signal quality: 59
- bad signal quality: 70
- highest possible value: 112

4.5.4.4. Reed-Solomon Error Counter

A 10 bit counter accumulates all errors that occurred in the Reed-Solomon words of one BC frame. More than 16 errors in a single Reed-Solomon word (worst case) will increment the counter by 17. The counter value is only valid in the BC mode of the FEC processor and only as long as the MSB of location $203 is equal to one.

Table 4–19: MSBs of accumulated Reed-Solomon errors ($203)

Bits	Signal	Comment
[7]	RSErrorValid	Set bit indicates a correctly decoded SCH preamble which means that the RSError is valid
[1..0]	RSError	2 MSBs of 10 bit Reed-Solomon error accumulator

Table 4–20: LSBs of accumulated Reed-Solomon errors ($202)

Bits	Signal	Comment
[7..0]	RSError	8 LSBs of 10 bit Reed-Solomon error accumulator

4.5.4.5. Service Component Output of the DRD 3515A

The SC-memory cell has to be written to select one Service Component for the SCC, SCD, SCW output lines of the DRD 3515A. This choice does not influence the selection of the Layer 3 audio Service Component in the MAS 3506D.

If a selected SC does not exist, there will be no output.

Table 4–21: SC-output ($01a)

Bits	Signal	Comment
[3..0]	SC	SC-output
	0(default)	no SC
	1	SC 1
	2	SC 2
	3	SC 3
	4	SC 4
	5	SC 5
	6	SC 6
	7	SC 7
	8	SC 8
	9..15	no SC

4.5.4.6. TSCC Information

TSCC information is available after the TSCC aquisition has been performed in TSCC-mode. After switching into BC-mode the TSCC information is still available for being read out by the controller. Thus, in cases where the TDM downlink is not changed but only a new Broadcast Channel is selected by the user, the previously stored TSCC information can be reused.

The TSCC information is stored in the memory cells $13e .. $1ff and contains 194 bytes. The alignment is shown in the following table.

Table 4–22: TSCC-fields

Memory Cell	Variable
$13e	TDM Identifier[15..8]
$13f	TDM Identifier[7..0]
$140	TSCW1[15..8]
$141	TSCW1[7..0]
...	...
$1fe	TSCW96[15..8]
$1ff	TSCW96[7..0]

The read-out is performed with the MEM Read command explained in Section 4.5.2.4. on page 24.
Reading should start at address **a** = $13e; for the complete TSCC-information 194 bytes (96 TSCC-word plus TDM identifier) should be transmitted:

Address code: a2 = $1, a1 = $3, a0 = $e
Byte count: n1 = $c, n0 = $2

Telegrams for this example:
<$38> <$30> <$81> <$3e> <$c2>
<$38> <$31> <$39> (now read 194 bytes)

4.5.5. Encryption Related Memory Cells

A special agreement is necessary to disclose information about the encrytion related memory cells. Please contact Micronas for details.

5. Interface Specifications

5.1. Broadcast Channel (BC) Interface

The Broadcast Channel is a container signal in the WorldSpace system that is combined of up to 8 Service Components that are all generated by one broadcaster. These services may contain different types of data like audio data (MPEG Layer 3 encoded), picture data, Internet pages etc. For these services the Broadcast Channel output may serve as a distribution link to external data decoders.

The Broadcast Channel output signal consists of 2 wires: A clock (BCC) and a data line (BCD). The data transmitted via the Broadcast Channel are 8 bits wide. The most significant bit is transmitted first.

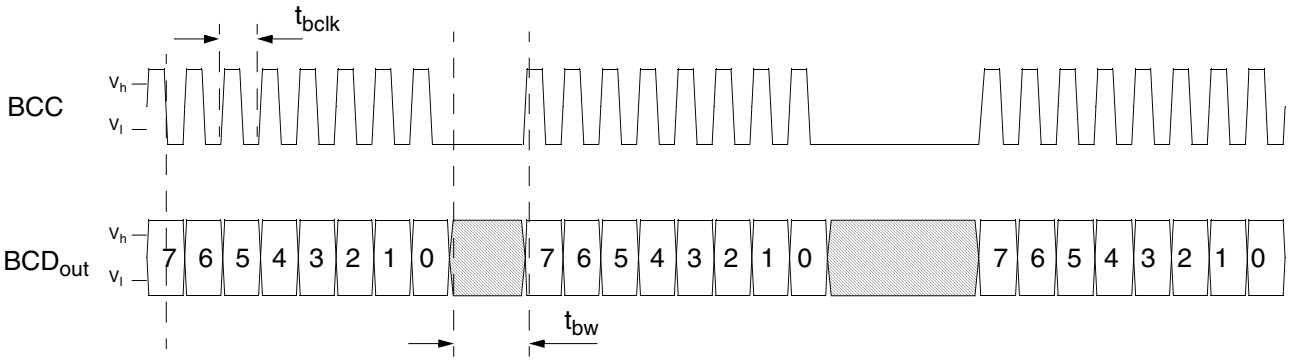

Fig. 5–1: Format of the Broadcast Channel (BC) interface

As shown in Fig. 5–1 the Broadcast Channel output always combines packages of 8 bits length. The data bits are valid at the negative slope of the clock line. The clock signal BCC is gated in correspondence with the BCD signal. Gating of the clock allows the use of bitstream decoder modules that reconstruct the word boundaries by detecting the clock pauses.

5.2. Service Component Interface

The Service Component (SC) data output interface is used to select one of the Service Components of a Broadcast Channel explicitly. This may simplify the application of an external low performance Service Component decoder. The selection of a Service Component at this output of the DRD 3515A does not influence the selection of an audio Service Component in the MAS 3506D.

The interface has basically the same format as the BC interface. However, the SC has an additional frame identification signal (SBCW).

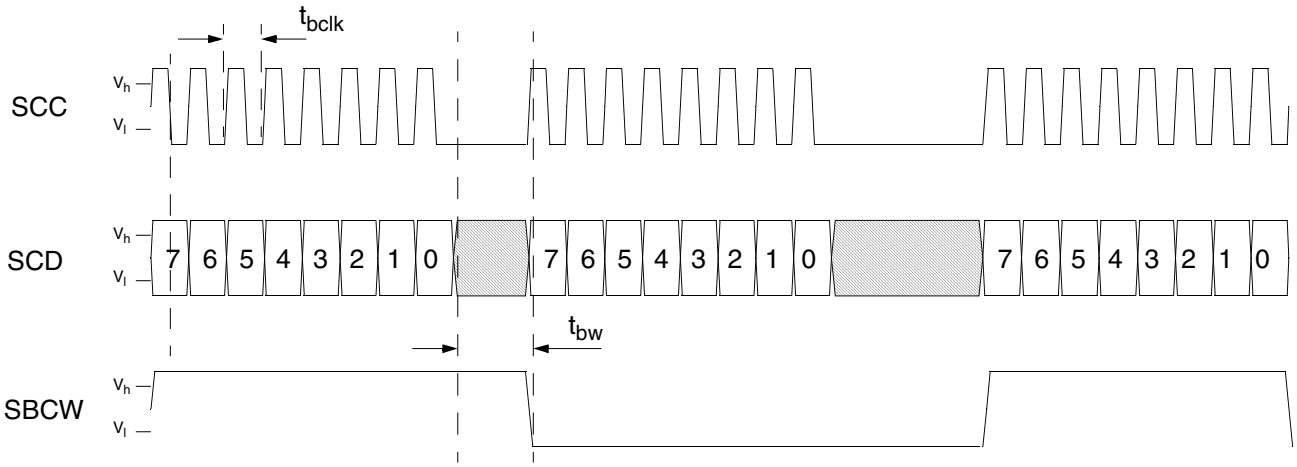

Fig. 5–2: Format of the Service Component interface

5.3. Serial Audio Data Interface

The serial audio data interface works with a subset of the usual I^2S lines, the DAD (digital audio data) and the DAI (digital audio frame identification) line. A special clock signal is not used for this interface. The clock information is derived from the OCLK signal which is running at a nominal frequency of 24.576 MHz.

An additional information about the oversampling factor of this clock has to be sent to the DRD 3515A serial interface by the control bit SI_IMOD in the GLB_CONFIG register of the DRD 3515A audio baseband block that defines the number of bits per sample.

The interface format is defined in the following figures:

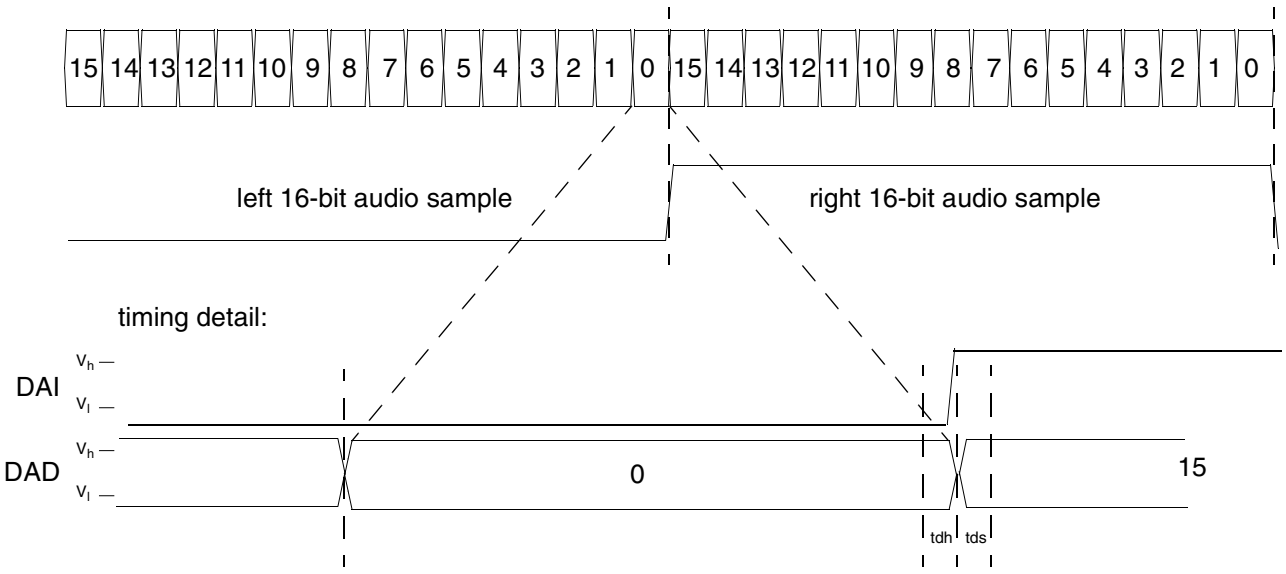

Fig. 5–3: Digital audio interface (serial audio data stream in 16 bit format)

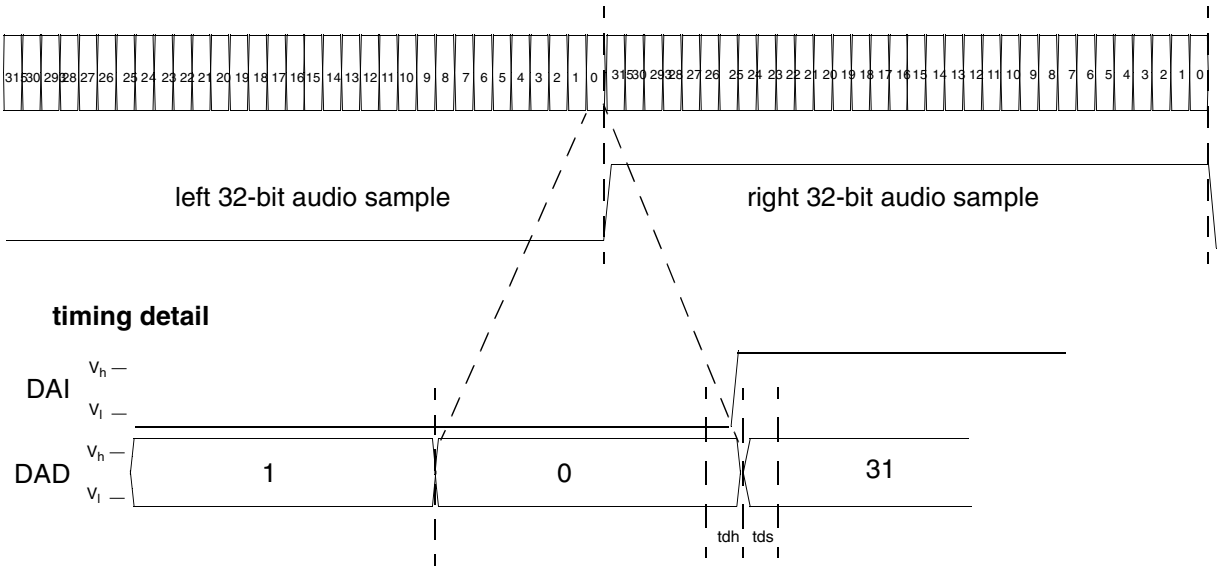

Fig. 5–4: Digital audio interface (32 bit serial data format)

Table 5–1: Data transmission rates of the serial audio interface in the 16 bit mode

fs (kHz)	SOI (kHz)	SOC (kHz)	OCLK (MHz)
8	8	8*16*2 = 256	24.576
12	12	12*16*2 = 384	24.576
16	16	16*16*2 = 512	24.576
24	24	24*16*2 = 768	24.576
32	32	32*16*2 = 1024	24.576
48	48	48*16*2 = 1536	24.576

Table 5–2: Data transmission rates of the serial audio interface in the 32 bit mode

fs (kHz)	SOI (kHz)	SOC (kHz)	OCLK (MHz)
8	8	8*32*2 = 512	24.576
12	12	12*32*2 = 768	24.576
16	16	16*32*2 =1024	24.576
24	24	24*32*2 = 1536	24.576
32	32	32*32*2 = 2048	24.576
48	48	48*32*2 = 3072	24.576

6. Specifications

6.1. Outline Dimensions

Housing: 44 pin PLCC, alternatively 44 pin QFP.

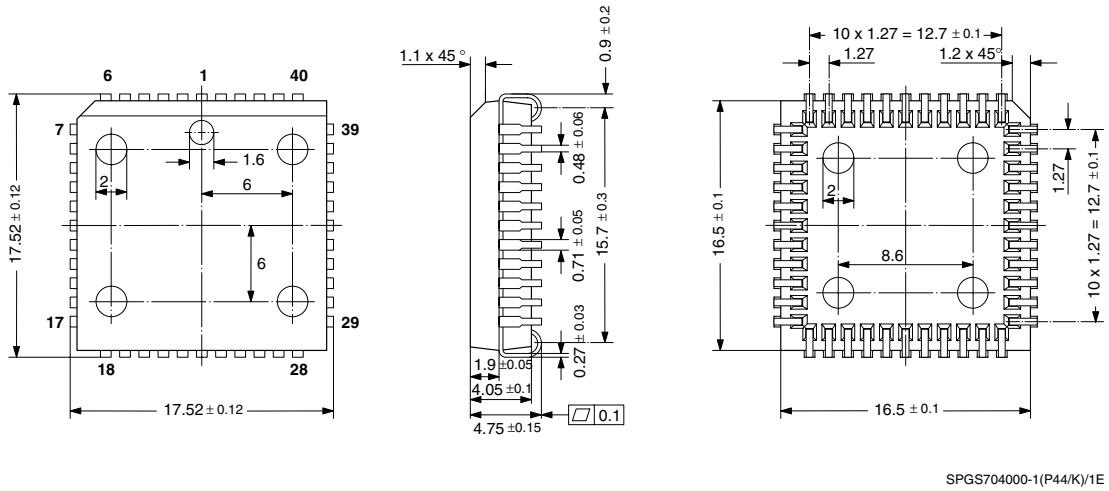

Fig. 6–1: 44-Pin Plastic Leaded Chip Carrier Package **(PLCC44)**
Weight approximately 2.5 g
Dimensions in mm

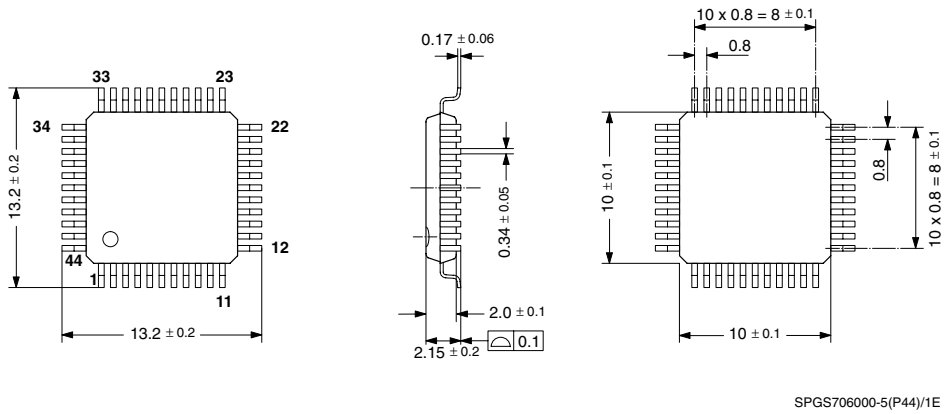

Fig. 6–2: 44-Pin Plastic Metric Quad Flat Pack **(PMQFP44)**
Weight approximately 0.4 g
Dimensions in mm

Caution: Start pin and orientation of pin numbering is different for PLCC and QFP-housings!

6.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
LV = if not used, leave vacant
VSS = if not used, connect to VSS

X = obligatory; connect as described in circuit diagram
VDD = connect to VDD

Pin No.		Pin Name	Type	Connection (If not used)	Short Description
PMQFP 44-pin	PLCC 44-pin				
1	6	AGNDC	IN/OUT	X	Analog reference ground
2	5	AVSS1	SUPPLY	X	VSS 1 for audio stages
3	4	AVSS0	SUPPLY	X	VSS 0 for audio output amplifiers
4	3	OUT1	OUT	LV	Audio Output: Headphone left or Speaker +
5	2	OUT2	OUT	LV	Audio Output: Headphone right or Speaker -
6	1	AVDD0	SUPPLY	X	VDD 0 for audio output amplifiers
7	44	AVDD1	SUPPLY	X	VDD 1 for audio stages
8	43	XTI	IN	X	quartz oscillator pin 1
9	42	XTO	OUT	X	quartz oscillator pin 2
10	41	AVDD2	SUPPLY	X	VDD for IF input
11	40	AVSS2	SUPPLY	X	VSS for IF input
12	39	RCLK	OUT	LV	output reference frequency
13	38	SGND	IN	X	Signal GND for IF input
14	37	IFIN	IN	X	differential IF input
15	36	IFINQ	IN	X	differential IF input inverted
16	35	VREFI	IN/OUT	X	Reference for IF input
17	34	VSS	SUPPLY	X	digital VSS
18	33	VDD	SUPPLY	X.	digital VDD
19	32	TEQ	IN	X	Test Enable, active low
20	31	PORQ	IN	VDD	Power On Reset, active low
21	30	SYNC	OUT	LV	TSCC mode: TSCC data ready BC mode: Decryption data from new SCH available
22	29	SDA	IN/OUT	X	SCI-data
23	28	SCL	IN/OUT	X	SCI-clock
24	27	SCC	OUT	LV	Service Component Clock
25	26	SCD	OUT	LV	Service Component Data
26	25	SBCW	OUT	X	Service Component Wordstrobe

Pin No. PMQFP 44-pin	Pin No. PLCC 44-pin	Pin Name	Type	Connection (If not used)	Short Description
27	24	WSEN	OUT	LV	WorldSpace enable output
28	23	PUP	IN	X	power up
29	22	OCLK	IN	X	24.576 MHz input oversampling clock
30	21	BCC	OUT	LV	Broadcast Channel clock
31	20	BCD	OUT	LV	Broadcast Channel data
32	19	DAI	IN	VSS	Digital Audio Frame Identification
33	18	DAD	IN	VSS	Digital Audio Data
34	17	AUX2L	IN	LV	AUX2 left input for external analog signals (e.g.tape)
35	16	AUX2R	IN	LV	AUX2 right input for external analog signals (e.g. tape)
36	15	AUX1L	IN	LV	AUX1 left input for external analog signals (e.g. FM)
37	14	AUX1R	IN	LV	AUX1 right input for external analog signals (e.g. FM)
38	13	FOUTL	OUT	X	Output to left external filter
39	12	FOPL	IN/OUT	X	Filter op-amp inverting input, left
40	11	FINL	IN/OUT	X	Input for FOUTL or filter op-amp output (line out)
41	10	FOUTR	OUT	X	Output to right filter op-amp
42	9	FOPR	IN/OUT	X	Right Filter op-amp inverting input
43	8	FINR	IN/OUT	X	Input for FOUTR or Filter opamp output (line out)
44	7	VREF	IN	X	Analog reference voltage

Caution: Start pin and orientation of pin numbering is different for PLCC and QFP-housings!

6.3. Pin Descriptions

6.3.1. Power Supply Pins

The DRD 3515A combines various analog and digital functions which may be used in different modes. For optimized performance major parts have their own power supply pins. All VSS-ground pins have to be connected.

VDD	**SUPPLY**
VSS	**SUPPLY**

The VDD and VSS power supply pair is connected internally with all digital parts of the DRD 3515A.

AVDD0	**SUPPLY**
AVSS0	**SUPPLY**

AVDD0 and AVSS0 are separate power supply pins that are exclusively used for the on-chip headphone/ loudspeaker amplifiers. AVDD0 and AVDD1 have to be connected together.

AVDD1	**SUPPLY**
AVSS1	**SUPPLY**

The AVDD1 and AVSS1 pins are supplying the analog audio processing parts except the headphone/loud-speaker amplifiers. AVDD0 and AVDD1 have to be connected together.

AVDD2	**SUPPLY**
AVSS2	**SUPPLY**

AVDD2 and AVSS2 are separate power supply pins for the analog IF input parts and the quartz oscillator of the DRD 3515A. The circuit board must be layouted in a way that digital noise and power supply ripple on lines connected to these pins are minimized.

6.3.1.1. IF-Related Pins

IFIN	**IN**
IFINQ	**IN**

The IFIN and IFINQ-pins are differential IF-input pins for a WorldSpace 2nd IF signal on 1.84 MHz.
For single ended IF-sources, the IFIN-pin should be used as the AC reference and IFINQ represents the single-ended input. In this case IFIN has to be connected to SGND via a capacitor.

SGND	**IN**

The SGND-pin serves as analog reference pin for the internal nodes. The circuit board layout needs extra care to ensure that no IF/RF-current is induced to any lines that lead to this pin. This pin has to be connected to AVSS2.

VREFI	**IN/OUT**

The VREFI-pin is used to block the internal reference voltage of the A/D converter against the signal ground SGND. VREFI and SGND must be connected via a 22 µF and 10 nF capacitor.

6.3.1.2. Analog Audio Pins

AGNDC	**IN/OUT**

DC-Reference for analog audio signals. This pin is used as reference for the internal op amps. This pin has to be blocked against VREF with a 3.3 µF parallel to a 10 nF capacitor.

Note: The pin has a typical DC-level of 1.5/2.25 V depending on the setting of SEL5V. It can be used as reference input for external op amps, when no current load is applied.

VREF	**IN**

Reference ground for the internal bandgap and biasing circuits. This pin should be connected to a clean ground potential (AVSS1). Any external distortions on this pin will affect the analog audio performance of the DRD 3515A.

AUX1L	**IN**
AUX1R	**IN**
AUX2L	**IN**
AUX2R	**IN**

The AUX-pins provide two analog stereo inputs. Auxiliary input signals e.g. the output of a conventional receiver circuit or the output of a tape recorder can be connected with these inputs. The input signals have to be connected by capacitive coupling. The signal return line is the analog reference pin VREF.

FOUTL	**OUT**
FOPL	**IN**
FINL	**IN/OUT**
FOUTR	**OUT**
FOPR	**IN**
FINR	**IN/OUT**

Filter op amps are provided in the analog baseband signal paths. These inverting op amps are freely accessible for external use by these pins.

The FOUTL/R-pins are connected with the buffered output of the internal switch matrix. The FOPL/R-pins are directly connected with the inputs of the inverting filter op amps, the FINL/R-pins are connected with the outputs of the op amps.

OUT1 **OUT**
OUT2 **OUT**

The OUT1/2-pins are connected to the internal output amplifiers. They can be used for either stereo headphones or a mono loudspeaker. The signal of the right channel amplifier can be inverted for mono loudspeaker operation. The return line of the headphone amplifier is AVSS0.

Caution: Any short circuit at these pins may result in destruction of the internal circuits due to excessive power dissipation.

6.3.1.3. Oscillator and Clock Pins

XTI **IN**
XTO **IN/OUT**

The XTI-pin is connected to the input of the internal crystal oscillator, the XTO-pin to its output. Both pins should be directly connected to the crystal and two ground connected capacitors (see application hint).

RCLK **OUT**

The RCLK-pin provides a buffered output of the crystal oscillator. The output signal has a sinusoidal shape and a reduced amplitude for a minimized electromagnetic noise emission. For operation modes that do not require the RCLK signal, this line can be switched off.

Caution: Any short circuit at these pins may result in destruction of the internal circuits due to excessive power dissipation.

6.3.1.4. Digital Interface Section

BCC **OUT**
BCD **OUT**

The output of the BCC-pin is the clock signal of the WorldSpace Broadcast Channel. This output clock signal is internally gated. With each positive slope of the BC-clock BC-data signal changes its value. The BCD output contains the digital data of the Broadcast Channel. The data are transmitted byte-wise with the most significant bit first. The BCC and BCD-pins are to be connected with the corresponding pins at the MAS 3506D.

SCC **OUT**
SCD **OUT**
SBCW **OUT**

The SCC/SCD are the output of the clock and the data signals of a selected Service Component. The data format is identical with the Broadcast Channel output (BCC, BCD). The SBCW-pin indicates the byte alignment of the SCD-data. The SBCW output changes with the most significant bit of each transmitted byte.

OCLK **IN**
DAI **IN**
DAD **IN**

These 3 pins are inputs for the decoded digital audio data and should be connected with the corresponding pins of the MAS 3506D. The OCLK expects a 24.576 MHz oversampling clock that is synchronized to the digital audio data DAD. The frame indication signal is named DAI. The digital audio data are transmitted in an I^2S compatible 16/32 bit format. However, the sample bit clock is not used by the DRD 3515A. It is rather internally derived from the OCLK-signal.

SYNC **OUT**

In TSCC-mode it indicates that the TSCC-data are ready for being read out by the controller. The signal is cleared when reentering the TSCC-mode.

In BC-mode the SYNC-signal indicates that a new SCH has been decoded and new decryption information is available. The signal is a single pulse per Broadcast Channel Frame (432 ms) of 25 ms minimum (8 PRCs in selected BC) and 200 ms maximum (1 PRC in selected BC).

PUP **IN**

Power up pin. Activating the PUP-pin enables the crystal oscillator and the SCI-interface of the DRD 3515A. For operation with the DC/DC-converter the PUP-pin has to be connected to the corresponding pin of the MAS 3506D that indicates that the output of the DC/DC-converter has reached its operating voltage.

WSEN **OUT**

The WSEN output of the DRD 3515A indicates that the WorldSpace mode is active. This pin should be connected with the corresponding MAS 3506D-pin to start the Layer 3 decoding. It can also be used to activate the WorldSpace tuner.

SCL **IN/OUT**
SDA **IN/OUT**

SCL (serial clock) and SCA (serial data) provide the connection to the serial control interface.

6.3.1.5. Other Pins

TEQ **IN**

This pin must always be connected to VDD.

PORQ **IN**

This pin may be used to reset the chip. Pulling this pin to ground potential has the same effect as the internal power on reset. If not used, this pin must be connected to VDD.

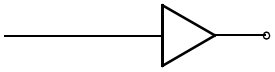

Fig. 6–3: Output Pin: RCLK

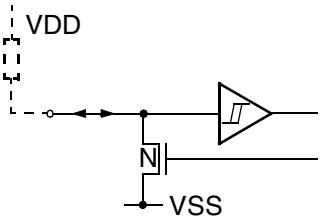

Fig. 6–4: Input/Output Pins SDA, SCL

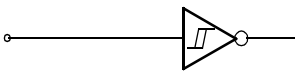

Fig. 6–5: Input Pins DAI, DAD, PORQ

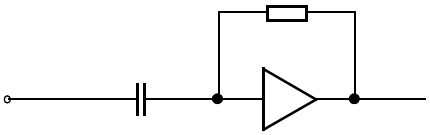

Fig. 6–6: Input Pin OCLK

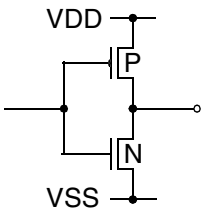

Fig. 6–7: Output Pins
SCC, SCD, WSEN, BCC, BCD, SYNC, SBCW

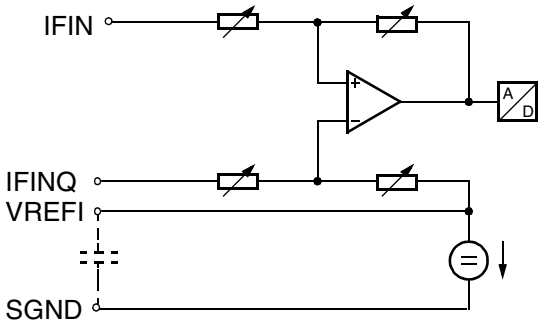

Fig. 6–8: Input Pins VREFI, IFINQ, IFIN, SGND

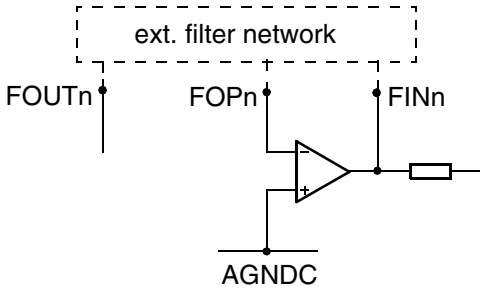

Fig. 6–9: Pins FINR, FOPR, FINL, FOPL

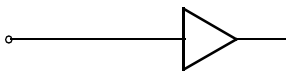

Fig. 6–10: Input Pins TEQ, PUP

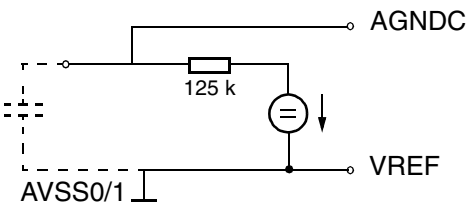

Fig. 6–11: Pins AGNDC, VREF

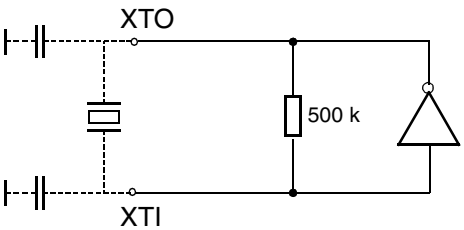

Fig. 6–12: Output/Input Pins XTI, XTO

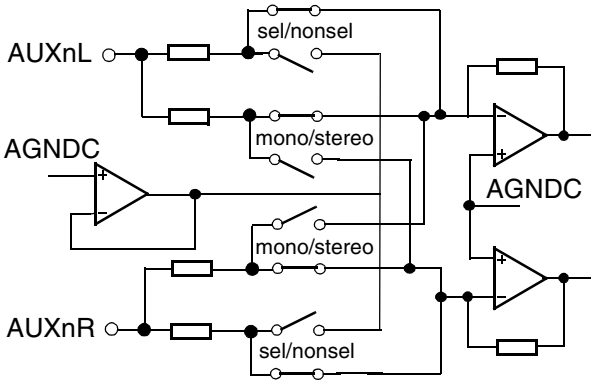

Fig. 6–13: Input Pins AUX1R, AUX1L, AUX2R, AUX2L

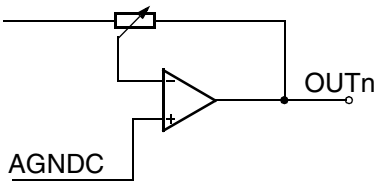

Fig. 6–14: Output Pins OUT1, OUT2

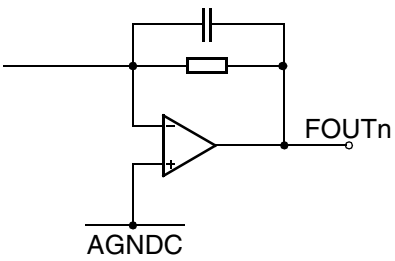

Fig. 6–15: Output Pins FOUTL, FOUTR

6.4. Electrical Characteristics

6.4.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature		–20	85	°C
T_S	Storage Temperature		–40	125	°C
P_{max}	Power dissipation QFP			620	mW
	Power dissipation PLCC			720	
$VSUP_A$	Analog supply voltage [1]	AVDD0/1	–0.3	6	V
$VSUP_D$	Digital supply voltage		–0.3	6	V
	Input voltage, all digital inputs		–0.3	$VSUP_D$ + 0.3	V
	Input current, all digital inputs		–20	+20	mA
	Input voltage, all analog inputs		–0.3	$VSUP_A$ + 0.3	V
	Input current, all analog inputs		–5	+5	mA
	Output current, audio output [2]	OUT1/2		0.2	A
	Output current, all digital outputs			250	mA

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

[1] Both have to be connected together!

[2] These pins are NOT short circuit proof !

6.4.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Temperature Ranges and Analog Supply Voltages						
T_A	Ambient temperature range		0		80	°C
$VSUP_A$	Analog audio supply voltage at T_A	AVDD0/1	3.0	3.3 or 5.0[1)]	5.5	V
$VSUP_{IF}$	IF input and oscillator supply voltage at T_A	AVDD2	3.0		3.6	V
Digital Supply Voltage						
$VSUP_D$	Digital supply voltage at T_A	VDD	2.7	3.3	3.6[2)]	V
Relative Supply Voltages						
$VSUP_A$	Analog audio supply voltage in relation to the digital supply voltage	AVDD0/1	$VSUP_D$ −0.25 V		5.5 V	
$VSUP_{IF}$	IF input supply voltage in relation to the digital supply voltage	AVDD2	2.7 V		$VSUP_D$ +0.25 V	
Digital Input Pins						
I_{IL27}	Input Low Voltage at V_{DD} = 2.7 V ... 3.6 V	$\overline{POR}$ SCL, SDA			0.5	V
I_{IH36}	Input High Voltage at V_{DD} = 2.7 V ... 3.6 V		1.8			V
I_{IH33}	Input High Voltage at V_{DD} = 2.7 V ... 3.3 V		1.7			V
I_{IH30}	Input High Voltage at V_{DD} = 2.7 V ... 3.0 V		1.6			V
I_{ILD}	Input Low Voltage	PUP, DAI, $\overline{DAD}$, $\overline{TE}$,			0.5	V
I_{IHD}	Input High Voltage		$VSUP_D$ −0.5 V			

[1)] The supply voltage for the audio parts depends on the setting of bit SEL5V in register GLB_CNFG
[2)] Higher operating voltages are possible on request.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Analog Reference						
C_{AGNDC1}	Analog reference capacitor	AGNDC		3.3		µF
C_{AGNDC2}	Analog reference capacitor	AGNDC		10		nF
C_{VREFI1}	IF input reference capacitor	VREFI		22		µF
C_{VREFI2}	IF input reference capacitor	VREFI		10		nF
Analog Audio Inputs						
V_{AI}	Analog Input Voltage AC, SEL5V = 0	AUXnL/R[3]		0.35	0.7	V_{rms}
V_{AI}	Analog Input Voltage AC, SEL5V = 1	AUXnL/R[3]		0.525	1.05	V_{rms}
Analog Filter Input and Output						
Z_{AFLO}	Load at analog filter output[4]	FOUTL/R	7.5		6	kΩ pF
Z_{AFLI}	Load at analog filter input[5]	FINL/R	5		7.5	kΩ pF
Analog Audio Output						
R_{DEC}	Decoupling Resistor[6]	FINL/R	612	680		Ω
C_{DEC}	Decoupling capacitor	OUTn	100	150	200	µF
Z_{LO}	Load at Audio Line Output[7]	FINL/R	10		1	kΩ nF
Z_{AOL_HP}	Analog Output Load HP (47 Ω Series Resistor required, see Section 7.3. on page 49)	OUTn		32 400		Ω pF
Z_{AOL_SP}	Analog Output Load SP (bridged)	OUTn		32 50		Ω pF

[3] n = 1 or 2.
[4] Please refer to Section 7.2. “Recommended Low Pass Filters for Analog Outputs” on page 48.
[5] Please refer to Section 7.2. “Recommended Low Pass Filters for Analog Outputs” on page 48.
[6] Please refer to Section 7.1. “Line Output Details” on page 48.
[7] Please refer to Section 7.1. “Line Output Details” on page 48.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Quartz Characteristics						
T_{AC}	Ambient temperature range		–20		80	°C
F_P	Load resonance frequency at C_l = 20pF	XTn		14.725		MHz
$\Delta F/F_s$	Accuracy of adjustment	XTn	–20		20	ppm
$\Delta F/F_s$	Frequency variation versus temperature	XTn	–20		20	ppm
R_{EQ}	Equivalent Series Resistance	XTn		12	30	Ω
C_0	Shunt (parallel) capacitance	XTn		3	5	pF
C_1	Motional capacitance	XTn		14		fF
Load at Reference Frequency output						
Cload	Capacitance	RCLK	5	14	21	pF
Rload	Resistance	RCLK	1	2		kΩ

6.4.3. Extended Operating Range

Within the extended operating range, the IC operates as mentioned in the functional description. The functionality has been tested on samples, whereby the characteristics may lie outside the specified limits.

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient temperature range		–20		85	°C
$VSUP_A$	Analog Audio supply voltage	AVDD0/1	2.7		5.5	V
$VSUP_{IF}$	IF input supply voltage	AVDD2	2.7		3.6	V

6.4.4. Characteristics

At T_A = 0 to 80 °C, $VSUP_D$ = 3.0 to 4.8 V, $VSUP_A$ = 3.0..5.5 V, $VSUP_{IF}$ = 3.0 to 3.3 V; typical values at T_J = 27 °C, $VSUP_D$ = $VSUP_A$ = $VSUP_{IF}$ = 3.15 V, quartz frequency = 14.725 MHz, duty cycle = 50%, positive current flows into the IC, digital audio input word width = 32 bits

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Supply							
I_{VDD}	Current consumption	VDD		13		mA	BC with 16 or 32 kb/s
I_{VDD}	Current consumption	VDD		15		mA	BC with 48 or 64 kb/s
I_{VDD}	Current consumption	VDD		19		mA	BC with 96 or 128 kb/s
Backend Clock Input							
	Clock Input Voltage	OCLK	0		$VSUP_A$	V	
	Clock Amplitude		0.5			V	peak to peak, sine wave
Digital Output Pins							
	Output High Voltage	BCC, BCD, SCC SCD, SBCW, SYNC, WSEN	$VSUP_D$ –0.3			V	no load at output
	Output Low Voltage				0.3	V	
Data Outputs							
t_{bclk}	Clock period	BCC, SCC	-	3.2	-	µs	
t_{bw}	Clock low time		0	-	5	ms	
I^2C Bus							
I^2CC	Clock frequency	SCL			400	kHz	
R_{on}	Output impedance	SCL, SDA			60	Ω	I_{load} = 5 mA, $VSUP_D$ = 2.7 V
Analog Supply							
I_{AVDD}	Current Consumption Analog Audio, SEL5V = 0	AVDD 0/1	5.3 0.35	7.7 0.55	10 0.76	mA mA	BAS_PUP = 1, Mute BAS_PUP = 0, Mute
	SEL5V = 1		8.2 0.4	11.8 0.73	15.3 1.1	mA mA	BAS_PUP = 1, Mute BAS_PUP = 0, Mute
$PSRR_{AA}$	Power Supply Rejection Ratio for Analog Audio Output	AVDD 0/1, OUTn	60	63		dB	1kHz sine at 100 mV_{rms} Analog Gain = 6 dB
			20	40		dB	≤ 100 kHz sine at 100 mV_{rms}
$PSRR_{LO}$	Power Supply Rejection Ratio for Line Output	AVDD 0/1, FINL/R	65	67		dB	1kHz sine at 100 mV_{rms}
				58		dB	≤ 100 kHz sine at 100 mV_{rms}

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
I_{IF}	Current Consumption IF supply	AVDD2	5.7	7.8	10	mA	Crystal oscillator on, output disabled (DIS_RCLK = 1)
			7.0	9.6	12.5	mA	Crystal oscillator on, output enabled (DIS_RCLK = 0), load 14 pF
Reference Frequency Generation							
I_{DD}	Supply current	AVDD2		3.2		mA	21 pF, 1 kΩ, 3.15 V WSEN = 0
V_{XTn}	DC voltage at oscillator pins	XTn		0.5 * $VSUP_{IF}$		V	
C_{XTI}	Input capacitance at oscillator pin	XTI		3		pF	
C_{XTO}	Input capacitance at oscillator pin	XTO		7		pF	
Vxtalout	Voltage swing at oscillator pins (peak-peak)	XTn	0.6		1.0	pp, VDD_{IF}	
t_{SUP}	Oscillator start up time				50	ms	VDD slew rate
S	Transconductance	XTn	3.3			mA/V	(not tested)
N_{CP}	Phase noise	RCLK			–100	dBc	f_{mod} = 100 Hz (not tested)
$PSRR_{XTAL}$	FM power supply rejection ratio of quartz oscillator	RCLK		0.66		ppm/V	
Aacl	Gain between quartz oscillator and output	XTO, RCLK		0.47			no load at output
I_{DD}	Supply current	AVDD2		3.2		mA	21 pF, 1 kΩ, 3.15 V WSEN = 0
R_{out},HF	Output resistance	RCLK		120	160	Ω	
VclkoutAC	Voltage swing at reference frequency output	RCLK	250	412	500	mV_{rms}	$VSUP_{IF} \leq 3.3$ V
					560	mV_{rms}	$VSUP_{IF} \leq 3.6$ V
VclkoutDC	DC voltage at reference frequency output	RCLK	0.475	0.513	0.55	VDD_{IF}	
THD_{XTO}	Total harmonic distortion	RCLK		–37	–27	dB	
$PSRR_{XTO}$	Power Supply Rejection Ratio T	AVDD2, RCLK		0		dB	f < 20 kHz

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
IF Input							
V_{Reftop}	Reference voltage top	VREFI	2.5	2.65	2.8	V	10 µF || 10 nF, ≥ 10 MΩ probe
$V_{IF\ low}$	Differential input voltage for –6 dB_{FS}	IFIN, IFINQ		15		mV_{rms}	maximum gain[1)]
$V_{IF\ high}$	Input voltage for –6 dB_{FS}			530		mV_{rms}	minimum gain[1)]
Z_{IFQ}	Input impedance R, minimum gain R, maximum gain C	IFINQ	 1.5 20 3	 2.1 28 5	 2.8 38 7	 kΩ kΩ pF	pin to GND
Z_{IF}	Input impedance R C	IFIN	 40 3	 49.2 5	 60 7	 kΩ pF	pin to GND
V_{IFB}	Input bias voltage			0.975		V	DC compensation disabled
AGC Amplifier							
ΔAGC	Gain per step		0.9	1	1.1	dB	
ΔAGC	Number of steps			32			
QPSK Demodulation							
SNR_Q	Input S/N			3.0		dB	BER ≤ 10^{-4}
F_D	Maximum input frequency offset				80	kHz	
Analog Audio							
V_{AGNDC}	Analog Reference Voltage	AGNDC	1.46	1.5	1.54	V	SEL5V = 0 R_L >> 10 MΩ, referred to VREF
			2.20	2.25	2.31	V	SEL5V = 1 R_L >> 10 MΩ, referred to VREF
R_{AGNDC}	Output resistance of Analog Reference Voltage	AGNDC	94 92	130	165 172	kΩ kΩ	T_J = 27 ^OC, T_A = 0 to 80 ^OC i = ± 5µA, referred to VREF , SEL5V = 0
R_{IAUX}	Input resistance at Input Pins	AUXnL/R	10.4 10.2	14.2	18.1 18.9	kΩ kΩ	T_J = 27 ^OC T_A = 0 to 80 ^OC Input selected, BAS_PUP = 1 i = ± 10 µA, referred to VREF
			21 20.6	28.8	36.6 38.3	kΩ kΩ	T_J = 27 ^OC T_A = 0 to 80 ^OC Input not selected i = ± 10µA, referred to VREF
R_{OOUT}	Output resistance at Output pins	OUTn	460	650	890	Ω	T_J = 27 ^OC BAS_PUP = 0 i = ± 200 µA, referred to VREF

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
R_{OFILT}	Output resistance of Filter pins	FINL		15		kΩ	BAS_PUP =0,Mute i = ± 10µA, referred to VREF
		FINR		11,25		kΩ	
V_{OffI}	Offset voltage at Input pins	AUXnL/R	–15		15	mV	BAS_PUP = 1, referred to AGNDC
V_{OffO}	Offset voltage at Output pins	OUTn	–10		10	mV	BAS_PUP = 1, Mute referred to AGNDC
V_{OffFI}	Offset voltage at Filter Output pins	FOUTL/R	–15		15	mV	BAS_PUP = 1, referred to AGNDC
V_{OffFO}	Offset voltage at Filter Input pins	FINL/R	–20		20	mV	BAS_PUP = 1, referred to AGNDC
dV_{DCPD}	Difference of DC voltage at Output pins after Backend Low Power Sequence	OUTn	–10		10	mV	Analog Gain = Mute, BAS_PUP switched from 0 to 1
$R_{D/A}$	D/A passband ripple	OUTn, FOUTL/R		–0.1		dB	0 ... 0.47 fs; fs = 8, 12, 16, 24, 32, 48 kHz (no external filters used)
$A_{D/A}$	D/A stopband attenuation			40		dB	0.55 ... 7.45 fs (no external filters used)
BW_{AUX}	Bandwidth for auxiliary inputs	AUXn, FINL/R		760		kHz	
THD_{ALO}	Total Harmonic Distortion from auxiliary inputs to line outputs	AUXn, FINL/R			0.01	%	BW = 20 Hz ... 22 kHz, unweighted, R_L > 5 kΩ Input 1 kHz at 0.5 V_{rms} $R_{dec} \geq 612\ \Omega$
THD_{DLO}	Total Harmonic Distortion (D/A converter to line output)	FINL/R			0.01	%	BW = 20 Hz ... 0.5 fs, unweighted, R_L > 5 kΩ Input 1 kHz at –3 dBFS $R_{dec} \geq 612\ \Omega$
THD_{HP}	Total Harmonic Distortion (Headphone)	OUTn			0.02	%	BW = 20 Hz ... 0.5 fs, unweighted, $R_L \geq 32\ \Omega$ (47 Ω series resistor required), Analog Gain = 0 dB, Input 1 kHz at –3 dBFS
THD_{SP}	Total Harmonic Distortion (Speaker)	OUTn			0.05	%	BW = 20 Hz ... 0.5 fs, unweighted, $R_L \geq 32\ \Omega$ (speaker bridged), Analog Gain = 0 dB, Input 1 kHz at –3 dBFS
SNR_{AUX}	Signal to noise ratio from analog input to line output	AUXn, FINL/R	93	98		dB	SEL5V = 0, input –20 dB below 0.7 V_{rms} $R_L \geq 5$ kΩ, $R_{dec} \geq 612\ \Omega$ BW = 20 Hz ... 22 kHz
	Signal to noise ratio from analog input to headphone output	AUXn, OUTn	88	96		dB	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
SNR_1	Signal to Noise Ratio	OUTn	89	94		dB FS	$R_L \geq 32\ \Omega$ (external 47 Ω series resistor required) BW = 20 Hz ... 0.5 fs unweighted, Analog Gain = 0 dB, Input = –20 dBFS 32-bit I^2S
		FINL/R	90	92		dB FS	$R_L \geq 5\ k\Omega$, $R_{dec} \geq 612\ \Omega$ BW etc. as above 16 bit I^2S, SEL5V = 0
			90	95		dB FS	32 bit I^2S, SEL5V = 0
				96		dB FS	16 bit I^2S, SEL5V = 1
				98		dB FS	32 bit I^2S, SEL5V = 1
SNR_2	Signal to Noise Ratio	OUTn	59	64		dB FS	$R_L \geq 32\ \Omega$ (external 47 Ω series resistor required) BW = 20 Hz ... 0.5 fs unweighted Analog Gain = -40.5 dB, Input = -3 dBFS 32 bit I^2S
Lev_{Mute}	Mute Level	OUTn		–110		dBV_{rms}	BW = 20 Hz ... 22 kHz unweighted, no digital input signal, Analog Gain = Mute
V_{AO}	Analog Output Voltage AC	OUTn, FOUTL/R, FINL/R	0.65	0.7	0.75	V_{rms}	SEL5V = 0, $R_L > 5\ k\Omega$, Analog Gain = 0 dB Input = 0 dBFS digital
			1.0	1.05	1.1	V_{rms}	SEL5V = 1
G_{AUX}	Gain from auxiliary inputs to line outputs	AUXn, FINL/R	–0.5	0	0.5	dB	f = 1 kHz, sine wave, $R_L > 5\ k\Omega$ 0.5 V_{rms} to AUXn
P_{HP}	Output Power (Headphone)	OUTn		5		mW	SEL5V = 0, $R_L = 32\ \Omega$, Analog Gain = +2 dB, distortion < 1 %, external 47 Ω series resistor required
				12		mW	SEL5V = 1
P_{SP}	Output Power (Speaker)	OUTn		60		mW	$R_L = 32\ \Omega$, Analog Gain = +2 dB, distortion < 10 %, SEL5V = 0
				140		mW	SEL5V = 1
G_{AO}	Analog Output Gain Setting Range	OUTn	–75		18	dB	
dG_{AO}	Analog Output Gain Step Size	OUTn		1.5		dB	+18 ... –54 dB
				3			–54 ... –75 dB
E_{GA1}	Analog Output Gain Error	OUTn	–2		2	dB	–46.5 dB ≥ Analog Gain ≥ –54 dB
E_{GA2}	Analog Output Gain Error	OUTn	–1		1	dB	–40.5 dB ≥ Analog Gain ≥ –45 dB

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
E_{GA3}	Analog Output Gain Error	OUTn	–0.5		0.5	dB	18 dB ≥ Analog Gain ≥ –39 dB
E_{dGA}	Analog Output Gain Step Size Error	OUTn	–0.5		0.5	dB	18 dB ≥ Analog Gain ≥ –48 dB
G_{AI}	Analog Input Gain (Auxiliary analog inputs to line outputs)	AUXn, FINL/R	–0.5	0	0.5	dB	0.5 V_{rms}, 1 kHz
$XTALK_{LO}$	Crosstalk Left/Right Channel (Line Output)	AUXn, FOUTL/R, FINL/R	–80	–90		dB	f = 1 kHz, sine wave, R_L > 7.5 kΩ Analog Gain = 0 dB, Input = –3 dBFS or 0.5 V_{rms} to AUXn
$XTALK_{HP}$	Crosstalk Left/Right Channel (Headphone)	OUTn	–75	–80		dB	f = 1 kHz, sine wave, OUTn: R_L ≥ 32 Ω (47 Ω series resistor required) Analog Gain = 0 dB, Input = –3 dBFS or 0.5 V_{rms} to AUXn
$XTALK_2$	Crosstalk between Input Signal Pairs	AUXn	–80	–85		dB	f = 1 kHz, sine wave, FINL/R: R_L > 7.5 kΩ OUTn: R_L ≥ 32 Ω (47 Ω series resistor required) Analog Gain = 0 dB, Input = –3 dBFS and 0.5 V_{rms} to AUXn
dV_{DCPD}	Output click at headphone after activating BAS_PUP	OUT_n		2.3		mV	C_{VREFI} = 3.3 µF t_{BAS_PUP} = 2 s after Reset
dV_{DCM}	max. click output voltage after POR	OUT_n		10.2		mV	

[1] The peak-peak value of this sinusoidal voltage uses 0.5 FS of the ADC (–6dB_{FS}). This is also the reference value of the AGC to leave some headroom.

7. Application Notes

7.1. Line Output Details

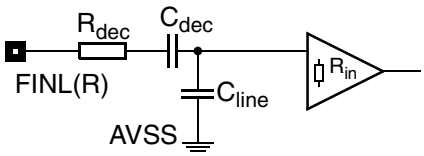

Fig. 7–1: Use of FINL/R as Line Outputs

Table 7–1: Load at FINL/R when used as Line Output for external amplifier

	Comment	Nominal Values
R_{dec}	Resistor used for decoupling C_{line} from FINL(R) to achieve stability	680 Ω
C_{line}	Capacitive load according to e.g. cable, amplifier	≤ 1 nF
C_{dec}	DC decoupling capacitor	1 µF
R_{in}	Input resistance of amplifier	≥ 10 kΩ

7.2. Recommended Low Pass Filters for Analog Outputs

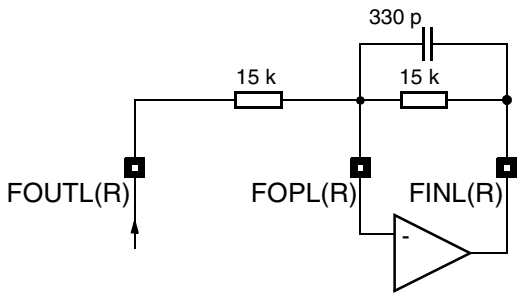

Fig. 7–2: 1st order low pass filter

Table 7–2: Attenuation of 1st order low pass filter

Frequency	Gain
24 kHz	–1.9 dB
30 kHz	–2.7 dB
300 kHz	–23 dB

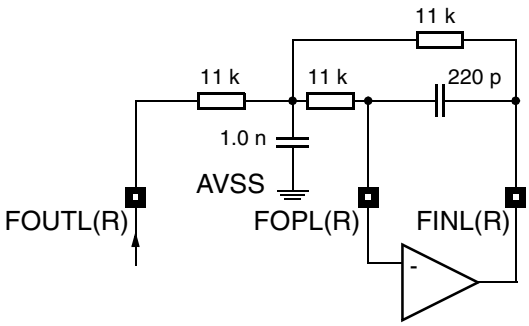

Fig. 7–3: 2nd order low pass filter

Table 7–3: Attenuation of 2nd order low pass filter

Frequency	Gain
24 kHz	–1.5 dB
30 kHz	–3.0 dB
300 kHz	–43 dB

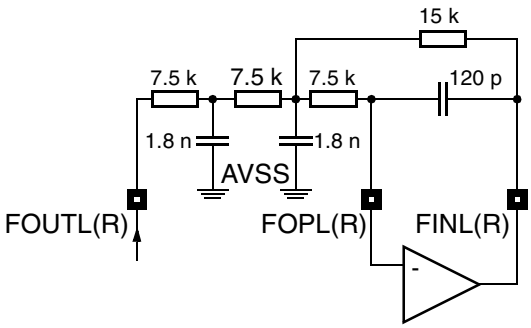

Fig. 7–4: 3rd order low pass filter

Table 7–4: Attenuation of 3rd order low pass filter

Frequency	Gain
18 kHz	0.17 dB
24 kHz	–0.23 dB
30 kHz	–3.00 dB
300 kHz	–63 dB

7.3. Equivalent Output Circuitry in 3 Different Analog Modes

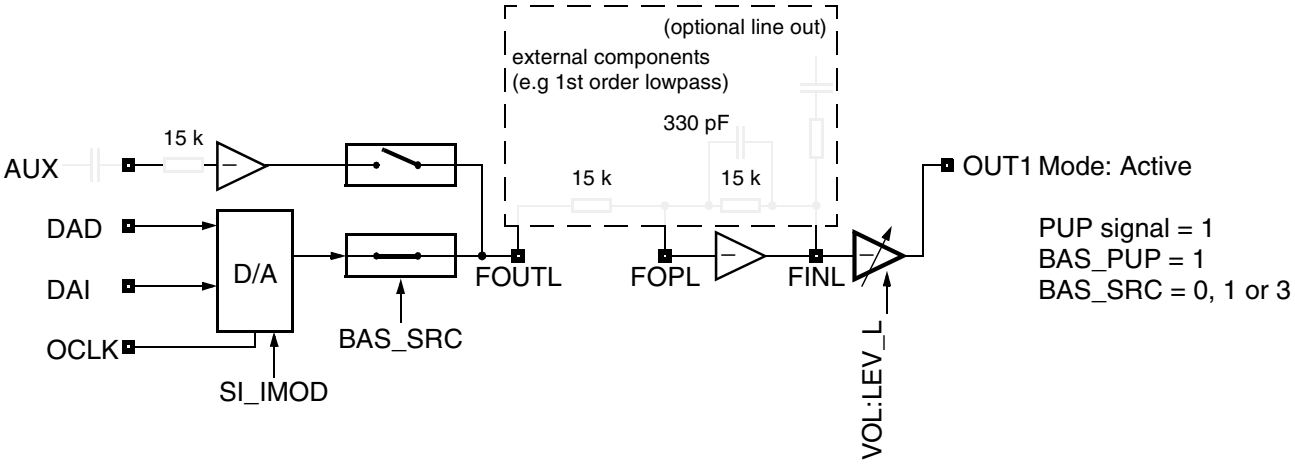

Fig. 7–5: Audio output circuits in active mode

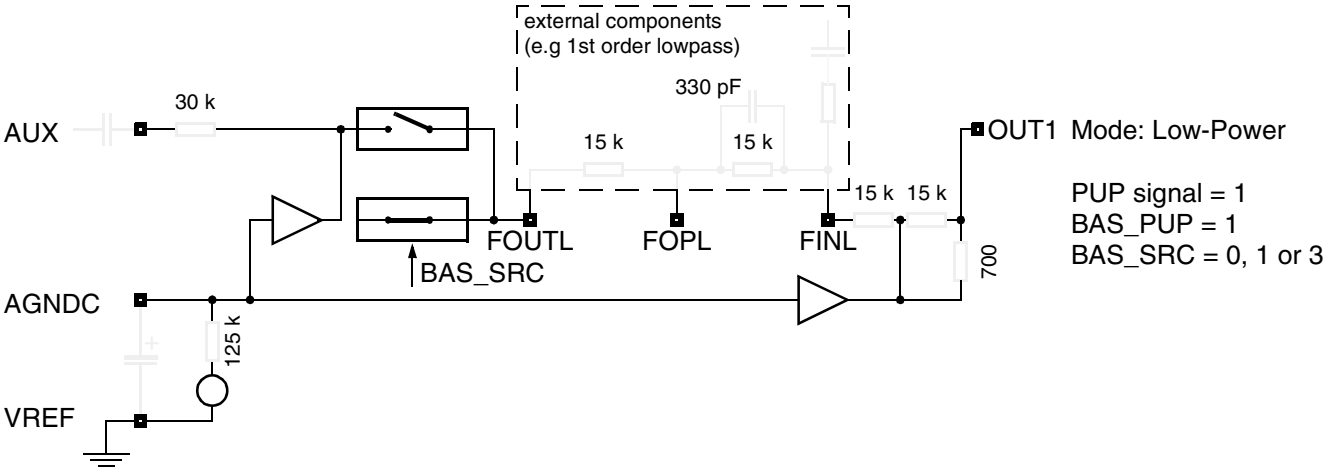

Fig. 7–6: Audio output circuits in stand-by mode

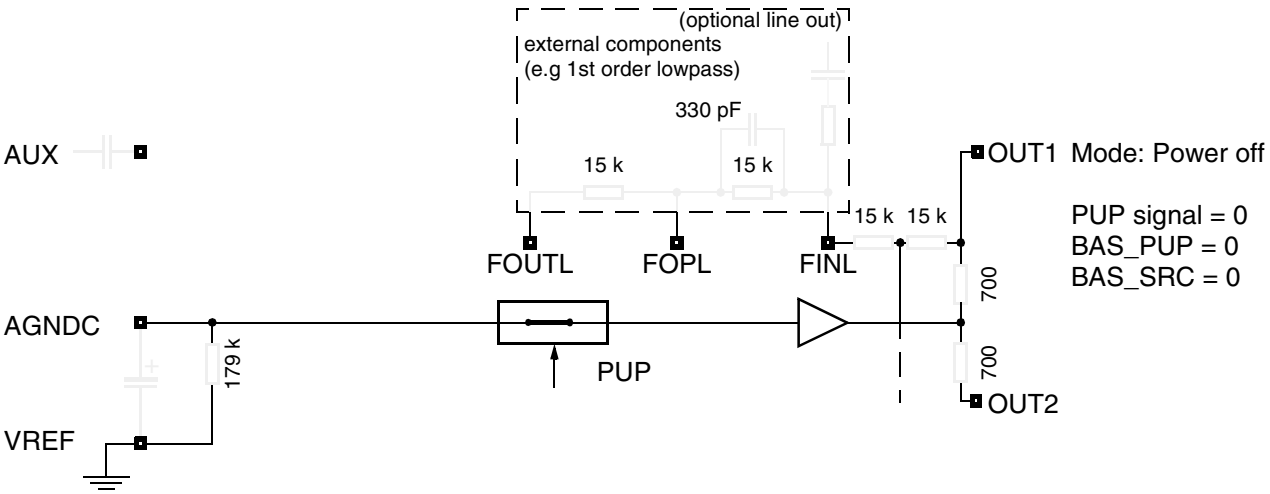

Fig. 7–7: Audio output circuits with IC set to low-power

8. Data Sheet History

1. Final data sheet: “DRD 3515A StarMan™ Channel Decoder for a WorldSpace™ TDM Downlink Carrier, Sept. 20, 2001, 6251-430-1DS. First release of the final data sheet.

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