Standard Products

CT1611 Microprocessor Interface DMA Controller with Buffer Memory, MIL-STD-1750A Compatible

www.aeroflex.com

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FEATURES

- Full Bus Control and RTU Operation
- Low Software Overhead
- Complete BI-Directional Message Buffer
- Memory-Mapped DMA Message Transfers
- Simple Programmable Polling Operation in Bus Controller Mode
- Pin Programmable for both 8 and 16 Bit Microprocessors
- Monolithic construction using linear ASICs
- Processed and screened to MIL-STD-883 specs
- Aeroflex is a Class H & K MIL-PRF-38534 Manufacturer
- MIL-PRF-38534 Compliant Devices Available

GENERAL

The CT1611 provides a complete Bus Controller and Remote Terminal interface between the MIL-STD-1553B chip set (CT1561, CT1602, CT1610, etc.) and most microprocessor-based systems (F9450A, 68000, 8086, VME bus, Multibus, etc.). The unit is constructed totally with CMOS technology and includes a custom CMOS chip, two HC CMOS FIFO's and HCT CMOS buffers. Thus the interface has extremly low power requirements.

The CT1611 interface permits the use of all 15 mode codes and all types of data transfers as specified in MIL-STD-1553B in both Bus Controller and Remote Terminal operating modes. A Remote Terminal is capable of switching to a Bus Controller when requested via the Dynamic Bus Control mode code.

DATA TRANSFERS

Data transfers in both Bus Controller and Remote Terminal operation are performed via a DMA burst. This powerful feature insures that the host microprocessor system will never be held up more than 16.5 usec when transferring 32 data words into or out of the interface. It also insures that only good and complete messages will be transferred to the host's memory. Operation of the DMA is as follows: When data is received from the 1553 cable via the chip set, it is loaded into an internal FIFO at the 20 µsec/word 1553 rate. Once the complete message has been received and has passed all validity tests, the CT1611 issues the signal $\overline{\text{DMA REQ}}$ to the subsystem. (This signal corresponds to a HOLD request in many systems.) The host microprocessor then acknowledges and grants this request by issuing the signal $\overline{\text{DMA ACK}}$. The CT1611 then becomes the bus master of the subsystem and transfers all the data on a memory-mapped basis. When the transfer is complete, the CT1611 removes its $\overline{\text{DMA REQ}}$ and returns control of the microprocessor bus to the microprocessor. When data is to be transmitted on the 1553 cable, a similar DMA takes place. Data is preloaded into the FIFO via a single DMA burst and then transmitted.

As a failsafe, an internal timeout is provided to insure that the CT1611 can never control the microprocessor bus longer than 80 µsec. In addition, a hard-wired Master Reset input signal is provided that will place all output signals in a tri-state condition. Therefore, in the unlikely condition of a failure in the CT1611, the host microprocessor system can never be brought down or placed in a non-recoverable state.

A built-in test function has been included to exercise the DMA operation and verify the message data path. This function is initiated by an I/O command from the subsystem.

I/O CONTROL

The CT1611 can be addressed, written to, read from, and programmed much like any peripheral device located on a microprocessor bus. The address lines and a device select input signal allow the subsystem to read or write to the CT1611 as if it were memory. In view of the fact that microprocessors are becoming very fast, two types of handshake signals were incorporated into the CT1611, either of which may be used to permit asynchronous read and write operations. Handshaking directly with the 9450A, 8085, 8086 and the 6802 is the active high Ready signal. Handshaking directly with the 68000 or VME and Multibus busses is the active low Acknowledge signal.

INTERFACING

To accomodate both 8 and 16 bit microprocessor data busses, the CT1611 data path is pin programmable for either operation. When operating in 8 bit mode, data is DMA'd in 8 bit bytes and therefore requires twice the time to be transferred.

Bus control signals are pin programmable for either individual read and write strobes or a common read/write signal and data strobe. Individual read and write strobes are used with the Intel 8085, 8086 and Multibus. A common read/write signal and data strobe are used with the 9450A, 6802, 68000 and VME bus. Two separate pins are provided for input and output data strobes. These signals may be connected or kept separate to insure that 1553 data can never be written into a protected area of memory.

RTU OPERATION

The CT1611 is powered-up and reset as a Remote Terminal. In addition, in Bus Controller mode, it can be changed into a Remote Terminal via an I/O command.

In Remote Terminal mode, the CT1611 uses dedicated registers for the received command word, the sync data word, and the vector word. The command word register contains a second tier so that receive command words are double buffered. This feature maximizes the allowable I/O access time.

Four interrupts are provided to alert the subsystem that a valid message has been received or transmitted or that a mode command has

been serviced. Use of the interrupts is optional. The interrupt signals are the same for bus control operation although different in meaning. Interrupts for received or transmitted data messages are generated after the DMA transfers have been completed.

The Busy, Service Request, and Subsystem Error bits for the status word are contained in a dedicated register accessible via I/O. The Busy bit is set high at power-up as well as via a subsystem reset.

BC OPERATION

The CT1611 is programmable into Bus Controller operation via I/O from the subsystem. Under Bus Controller mode, there are two command word registers, a received mode data register, two returned status word registers, an error latch and a transaction word register.

The first command register is used for all 1553 bus transfers. The second command register is for the second command word used in RT to RT transfers or for the associated mode data required for certain mode codes.

The CT1611 provides full validity checking for all 1553 transfers and alerts the subsystem, via interrupts, as to whether the transfer was valid or not. The two status word registers are preset high at the initiation of a transfer and may be read at completion. The second status word is provided for RT to RT transfers. The error latch may be used to determine the nature of a failure should a transfer be unsuccessful.

The transaction word register is used to define the type of transfer to be performed, to which bus the transfer is to be made, and to define which bits (when set) in the returned status word constitute an invalid transfer.

A polling operation has also been included that enables the CT1611 to automatically load the command words and transaction words from main memory via DMA. This function allows a preprogrammed polling sequence of the remote terminals to be implemented with a minimum of subsystem intervention.

Absolute Maximum Ratings

Parameter	Range	Units
Operating Free-air Temperature	-55°C to +125	°C
Storage Case Temperature	-55°C to +155	°C
Supply Voltage (V_{DD})	-0.3 to +7	Volts
Input and Output Voltage at any Pad	-0.3 to V_{DD} +0.3	Volts

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage V_{DD}	4.5	5.0	5.5	V
Operating Temperature	-55	-	+125	°C

Electrical Characteristics

(V_{DD} = +5.0V ±10%, T_A = -55°C to +125°C, unless otherwise specified)

Parameter	Conditions	Min	Max	Unit
V_{IH} High Level Input Voltage		2.0	-	V
V_{IL} Low Level Input Voltage		-	0.8	V
I_{IN} Input Current		-10	+10	µA
I_{IL} Low Level Input Current	Note 4A	-25	-400	µA
I_{IH} High Level Input Current	Note 4B	-25	-400	µA
V_{OH} High Level Output Voltage	Note 1	2.4	-	V
V_{OL} Low Level Output Voltage	Note 2	-	0.4	V
I_{DD1} Quiescent Supply Current	Note 3	5	30	mA
I_{DD2} Dynamic Supply Current	Note 5	-	200	mA

Note 1. I_{OH} = -2mA for I/O BUS, ADDRESS, R/$\overline{W}$ & STROBE signal pads
(FP and DIP Pins 12->27 / 28->33 / 5,7)

I_{OH} = -1mA for OUTPUT ONLY signal pads
(FP Pins 1->3,6,9,10,39->42,55->58,65,67->69,79,81->83)
(DIP Pins 1->3,6,9,10,39->42,57->60,67,69->71,81,83->85)

Note 2. I_{OL} = 4mA for I/O BUS, ADDRESS, R/$\overline{W}$ & STROBE signal pads
(FP and DIP Pins 12->27 / 28->38 / 5,7)

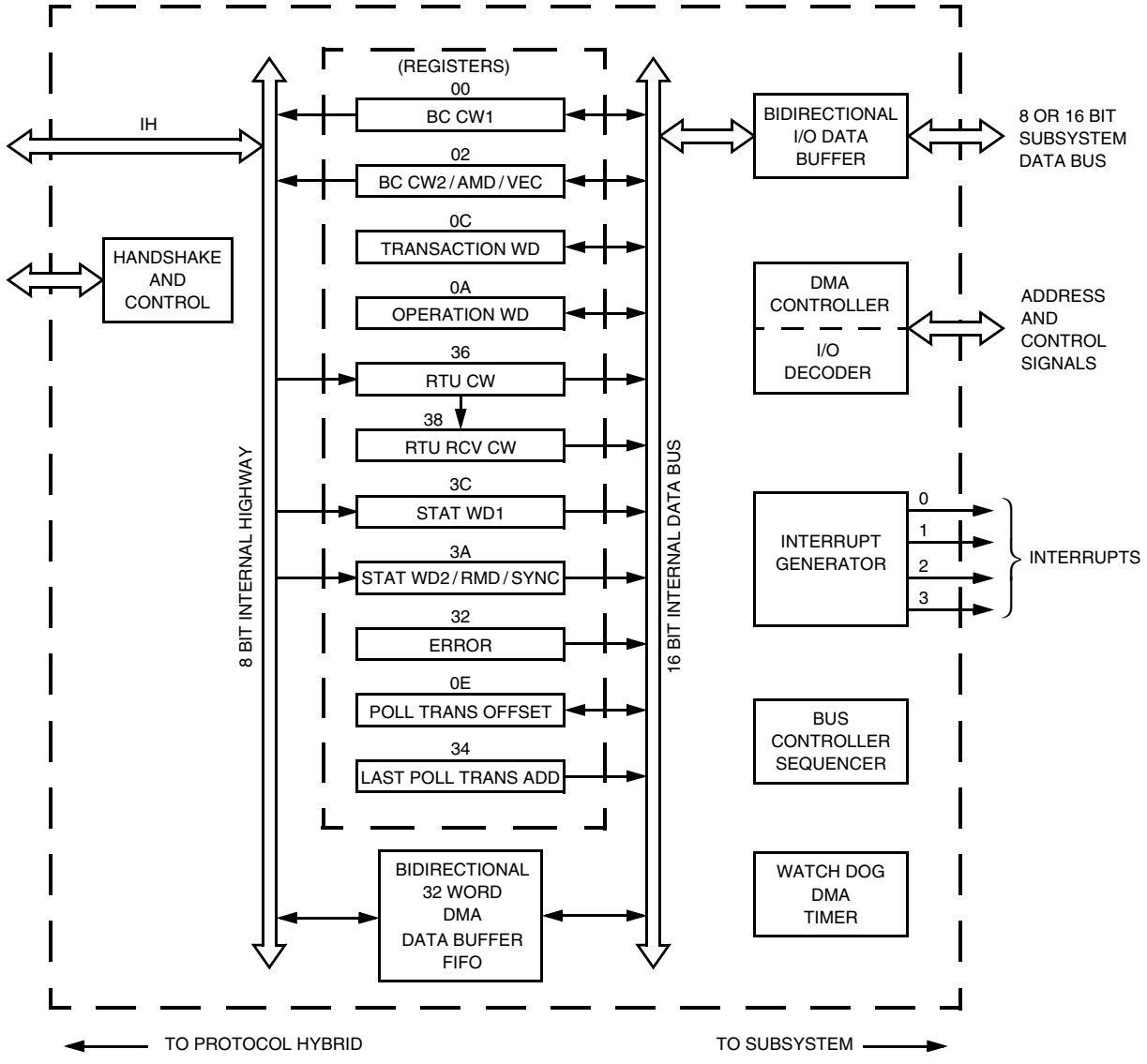
IOL = 2mA for OUTPUT ONLY signal pads
(FP Pins 1->3,6,9,10,39->42,55->58,65,67->69,79,81->83)
(DIP Pins 1->3,6,9,10,39->42,57->60,67,69->71,81,83->85)

Note 3. Bidirectional I/O at V_{DD}
(FP Pins 12->27 / 28->38 / 45->52 / 5)
(DIP Pins 12->27 / 28->38 / 47->54 / 5)

I/O Address Lines (FP and DIP Pins 34->38) at V_{DD}, remaining OUTPUTS = N/C, remaining INPUTS at V_{DD}, MRB at V_{IL} < 0.4V.

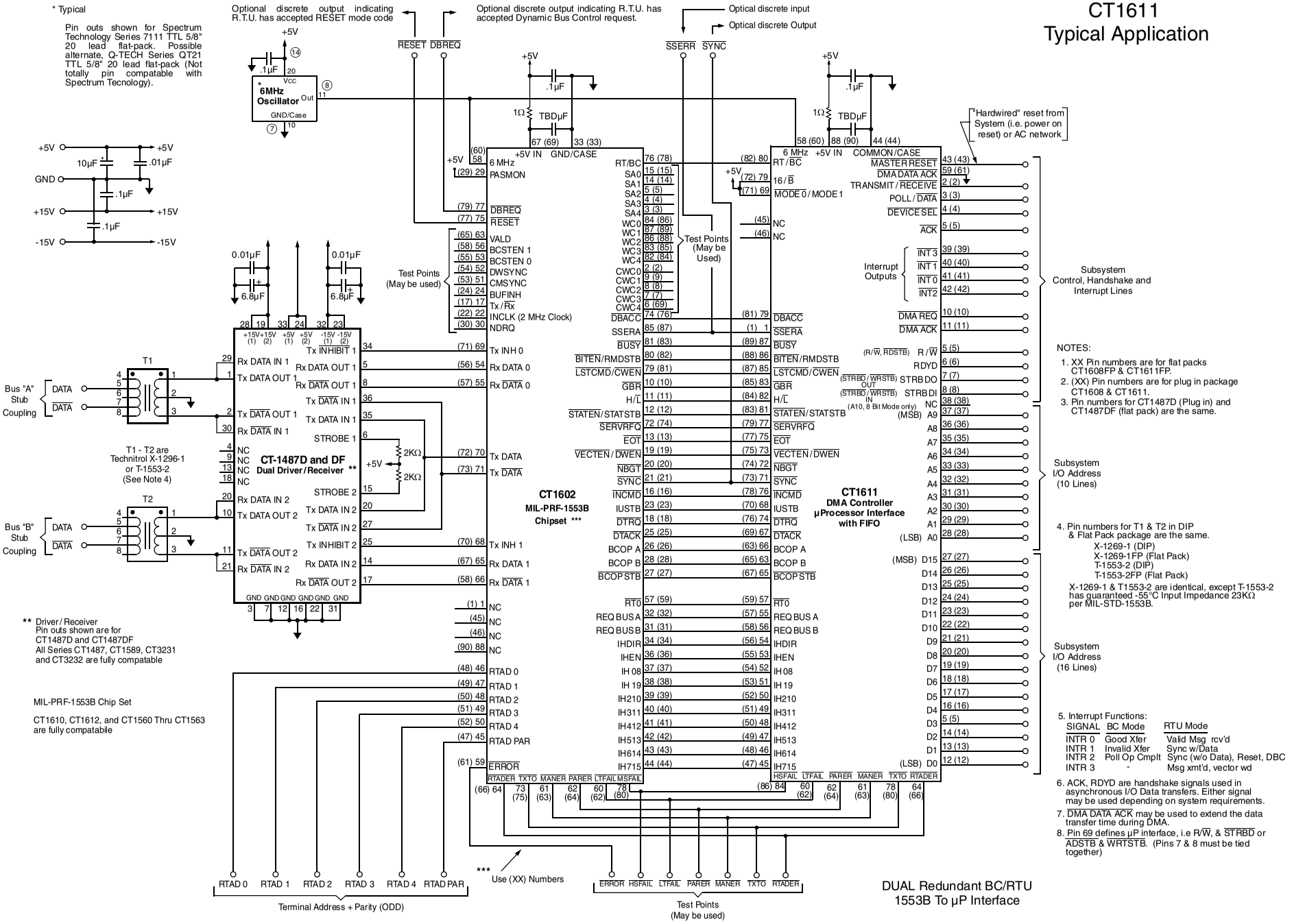
Note 4. For INPUTS
(FP Pins 59,62,63,64,66,77,86)
(DIP Pins 61,64,65,66,68,79,88)
@V_{DD} = 5.5V
A. @V_{IL} = 0.4V
B. @V_{IH} = 2.4V

Note 5. During typical 32 Word DMA (Output Loading = 0)



CT1611 FUNCTIONAL BLOCK DIAGRAM

CT1611
Typical Application

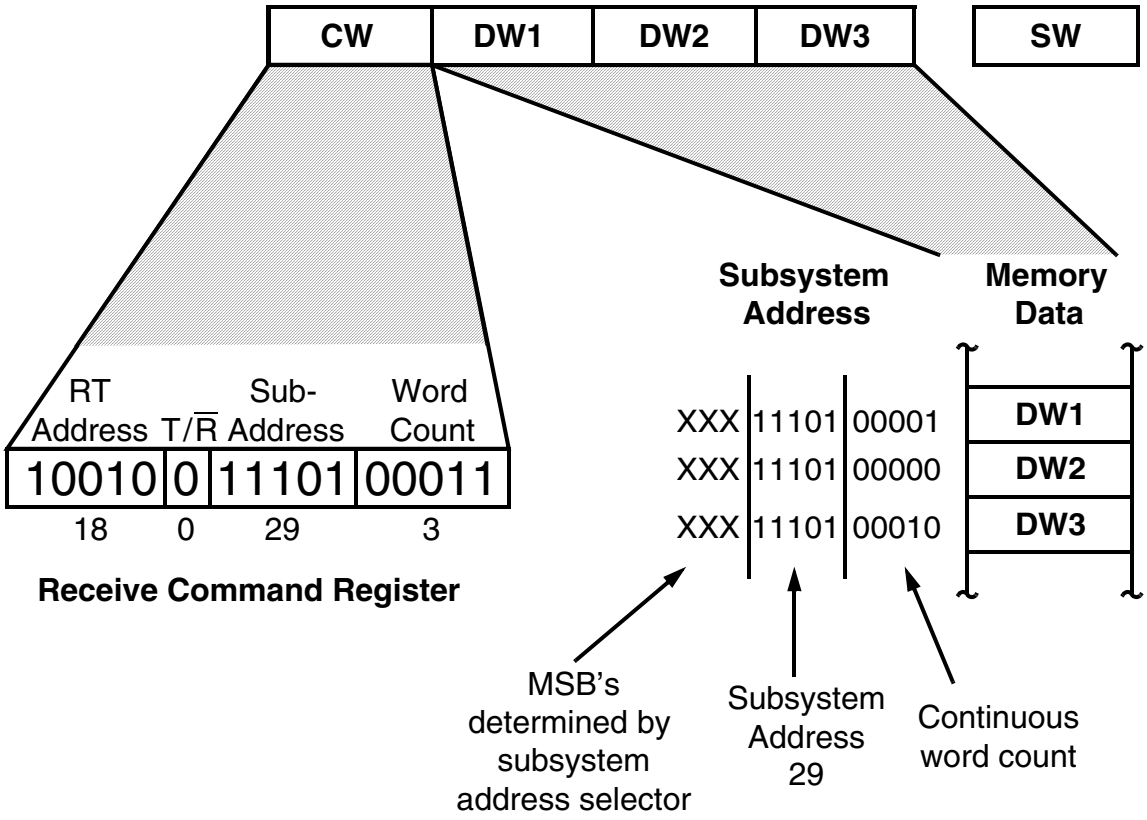


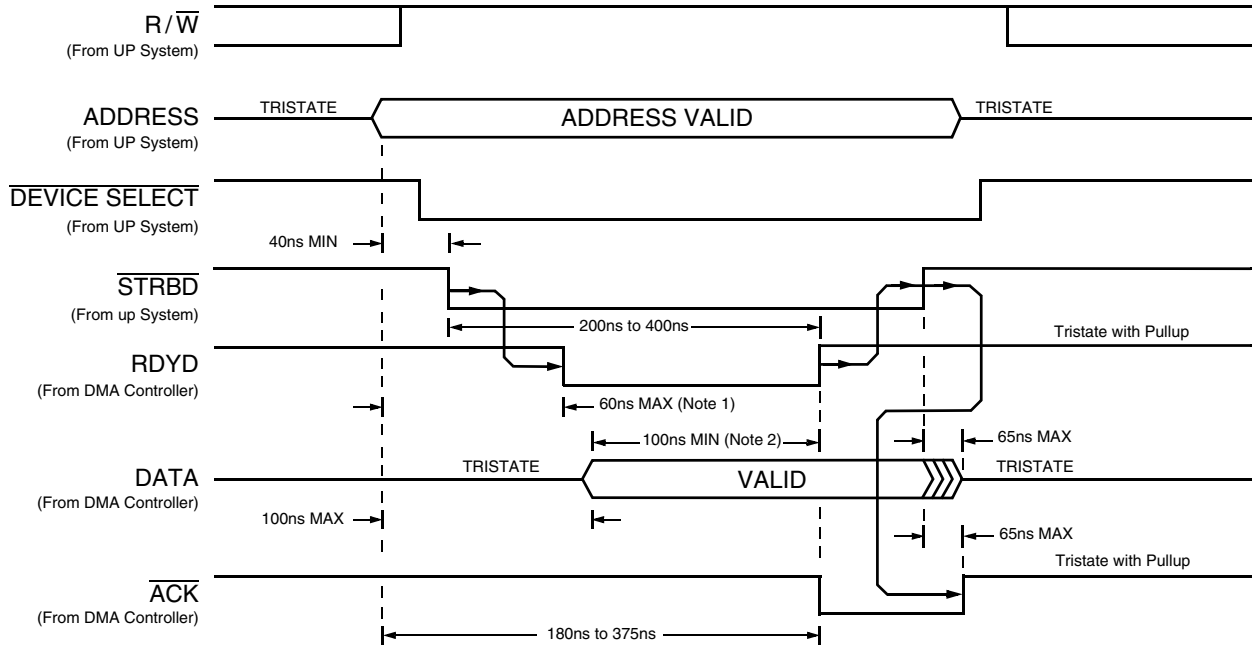
CT 1611

User's Guide

Example of DMA Data Transfer

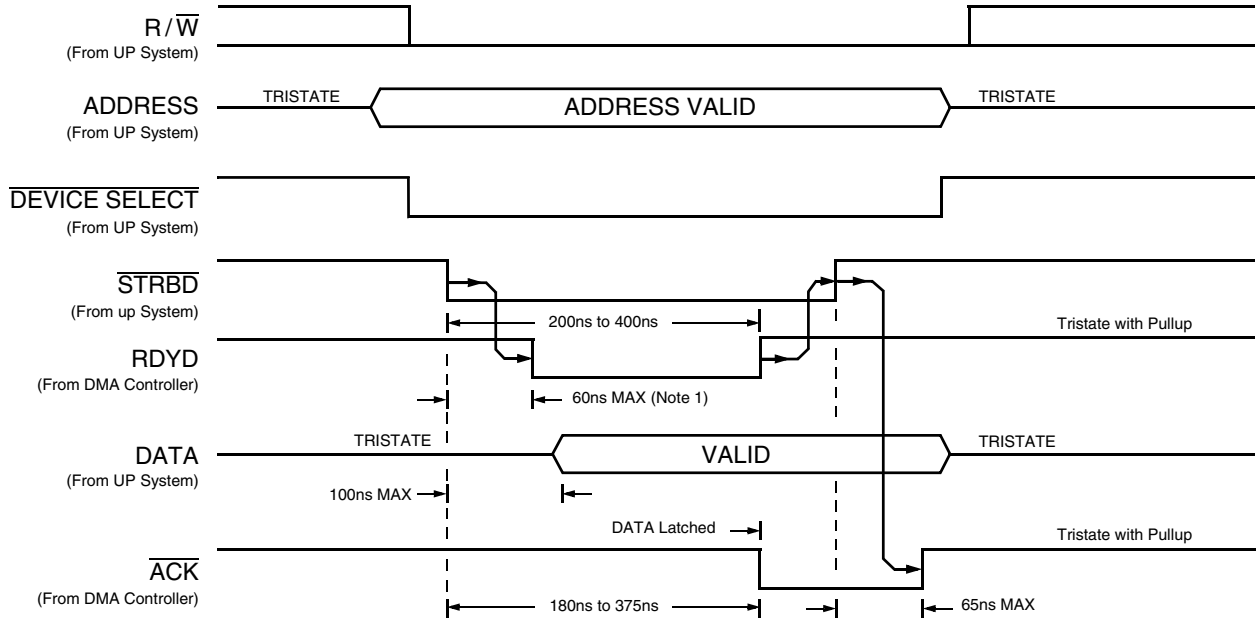
Transfer = 3-Word Receive Message in RTU Mode





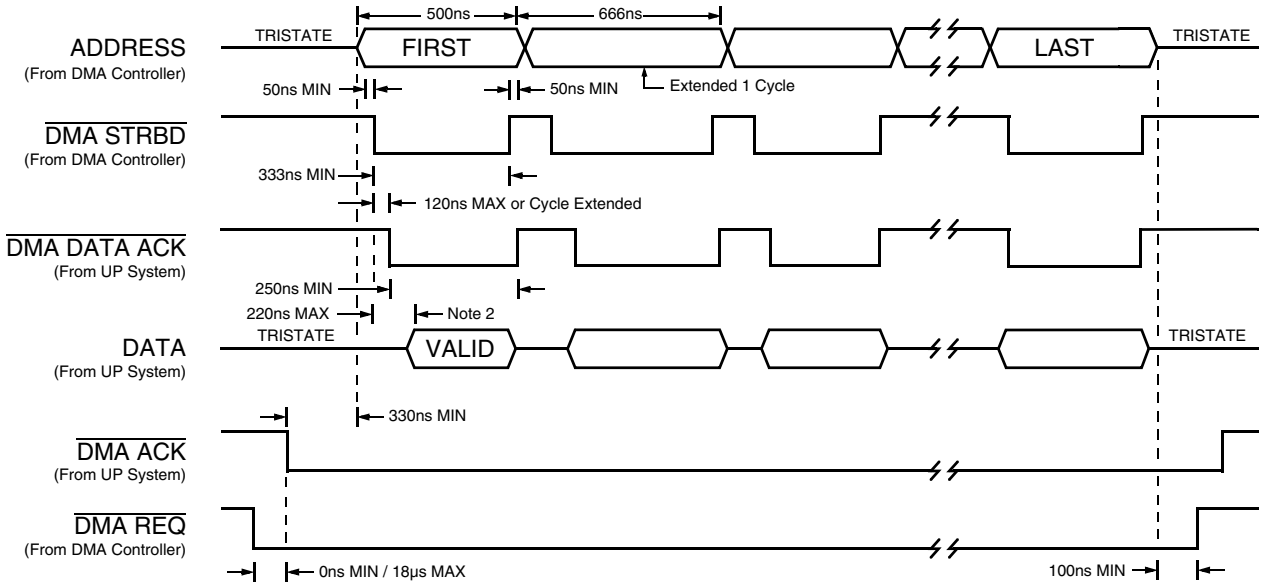
Notes:
1. Requires BOTH $\overline{\text{STRBD}}$ or $\overline{\text{DEVICE SELECT}}$ to be LOW.
2. DATA will be valid 100ns before RDYD goes HIGH, and $\overline{\text{ACK}}$ goes LOW.

I/O READ OPERATION



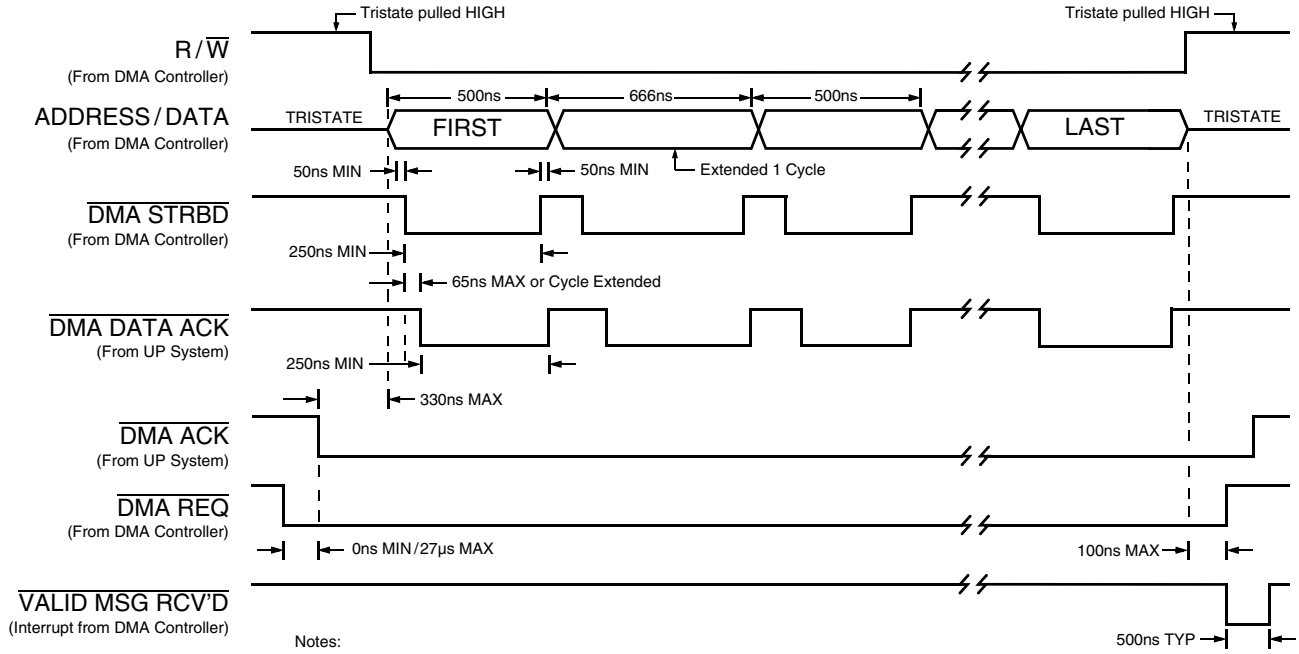
Notes:
1. Measured from $\overline{\text{STRBD}}$ or $\overline{\text{DEVICE SELECT}}$ whichever is valid LAST.
RDYD requires the coincidence of $\overline{\text{STRBD}}$ and $\overline{\text{DEVICE SELECT}}$.

I/O WRITE OPERATION



Notes:
1. R/$\overline{W}$ from DMA Controller = Logic "1".
2. DATA will be valid within 220ns of $\overline{STRBD}$ or VALID with $\overline{DMA\ DATA\ ACK}$.

DMA READ OPERATION



Notes:
1. If a $\overline{DMA\ DATA\ ACK}$ is not implemented in system, $\overline{DMA\ DATA\ ACK}$ should be either connected to $\overline{DMA\ STRBD}$ (preferred) or tied LOW.
2. Preferred method for resetting $\overline{DMA\ DATA\ ACK}$ HIGH is with trailing edge of $\overline{DMA\ STRBD}$.

DMA WRITE OPERATION

Summary of I/O Commands for CT1611 1553B Interface (All Codes HEX)

<table>
<tr><th colspan="2">Bus Controller I/O</th><th>Address Code (8 Bit Mode)</th><th>Description</th></tr>
<tr><td>(Read or Write)</td><td>Command Word # 1</td><td>XX00 (Low)
XX01 (High)</td><td>All Transfers</td></tr>
<tr><td>(Read or Write)</td><td>Command Word # 2</td><td>XX02</td><td>1. Second command word for RT to RT Transfers
2. Also associated mode data for mode change such as sync w/data
3. Also used for RTU vector word</td></tr>
<tr><td>(Read or Write)</td><td>Transaction Word</td><td>XX0C</td><td>Defines type of transfer and BUS selection
<table>
<tr><th colspan="3">Examples</th></tr>
<tr><th colspan="2">Function</th><th>Data</th></tr>
<tr><td>Normal xfer
Normal xfer</td><td>Bus 0
Bus 1</td><td>0000
0008</td></tr>
<tr><td>RT to RT</td><td>Bus 0
Bus 1</td><td>0001
0009</td></tr>
<tr><td>Mode (No Data)
Mode (No Data)</td><td>Bus 0
Bus 1</td><td>0003
000B</td></tr>
<tr><td>Mode (Rtn’d Data), i.e. vector word last cmd, etc.</td><td>Bus 0
Bus 1</td><td>0005
000D</td></tr>
<tr><td>Mode (ass’td Data), i.e. sync w/data</td><td>Bus 0
Bus 1</td><td>0007
000F</td></tr>
</table></td></tr>
<tr><td>(Write Only)</td><td>Trigger</td><td>XX2A</td><td>Triggers Bus Transaction
Note: Command word(s) and transaction code must be loaded</td></tr>
<tr><td>(Read Only)</td><td>Status Word 1</td><td>XX3C</td><td>Return status word for all transactions (first for RT to RT).
Note: This register is preset to FFFF at beginning of transaction and at reset.</td></tr>
<tr><td>BC (Read Only)</td><td>Status Word 2
Rtn’d Mode Data</td><td rowspan="2">XX3A</td><td rowspan="2">Second returned status word for RT to RT xfers, also preset FFFF. Also returned mode data, such as vector word and last command.</td></tr>
<tr><td>RTU (Read Only)</td><td>Sync w/Data
Sync Word</td></tr>
<tr><td>(Read Only)</td><td>Command Word</td><td>XX36</td><td>Received command word for all transactions. i.e. transmit, receive* and mode.
* use XX38</td></tr>
<tr><td>(Read Only)</td><td>Receive Command Word</td><td>XX38</td><td>Double Buffered version of above for valid receive commands (provides more I/O time).</td></tr>
<tr><td>(Read or Write)</td><td>Vector Word</td><td>XX02</td><td>Mode Data
-to be transmitted
- same reg as CW # 2</td></tr>
</table>

Summary of I/O Commands for CT1611 1553B Interface (All Codes HEX)

Bus Controller I/O		Address Code (8 Bit Mode)	Description
(Read Only)	Sync Word	XX3A	1. Mode Data -to be received 2. Same as returned mode in BC mode
(Write Only)	Reset I	XX2E	Resets CT1611 interface only
(Write Only)	Reset II	XX2C	Resets CT1611 and CT1610 front end, will reset bits in returning status word such as "TF" flag. Same as hard wired master reset used on power up.
(Read or Write)	Operational word	XX0A	Defines BC mode and RTU mode. Data FFF0 = RTU FFF1 = BC Note: Powers up and is reset to busy RTU.

RTU Mode

1. Conditions for Busy

When the CT1611 is declared busy, the DMA data transfer operation is inhibited. Mode data is stored in internal registers, and is therefore unaffected by busy. The bust bit is located in the Operation Register.

1.1 Busy Set by I/O and $\overline{\text{POR}}$ / $\overline{\text{RESET}}$

1.2 DMA not complete
(This in general should never occur).

1.3 FIFO Test

1.4 Receive Commands
If a Terminal is declared busy during the reception of a valid message, that message will be received and a DMA request will be generated.

Data will be held indefinately until the DMA request is acknowledged.

Once the DMA is completed, a valid message received interrupt will be generated.

1.5 Transmit Commands
If the subsystem is going to enter a non-interruptable mode and therefore declares itself busy and the condition exists that a transmit command may be received "simultaneously", the subsystem should wait 6µsec before beginning. (If a DMA request is not made during this time, none will be made until the terminal is declared not busy).

This insures:

a. HSFAIL will not occur because of the busy condition missing the command word.

b. DMA issued, that can't be acknowledged at a "non-interruptable time" by the microprocessor subsystem.

Interface Mode

MODE 1 / $\overline{\text{MODE 0}}$ ⟶ "0" is Motorola/Fairchild 9450 compatibility

"1" is Intel compatibility

M1 / $\overline{\text{M0}}$	Write Operations	Read Operations
0	$\overline{\text{RDSTB}}$ / R/$\overline{\text{W}}$ ⟶ R/$\overline{\text{W}}$ $\overline{\text{WTSTB}}$ / $\overline{\text{STRBD}}$ ⟶ $\overline{\text{STRBD}}$ R/$\overline{\text{W}}$ = 0 $\overline{\text{STRBD}}$ =	- Same- R/$\overline{\text{W}}$ = 1 $\overline{\text{STRBD}}$ =
1	$\overline{\text{RDSTB}}$ / R/$\overline{\text{W}}$ ⟶ $\overline{\text{RDSTB}}$ $\overline{\text{WTSTB}}$ / $\overline{\text{STRBD}}$ ⟶ $\overline{\text{WTSTB}}$ $\overline{\text{RDSTB}}$ = 0 $\overline{\text{WTSTB}}$ =	- Same- $\overline{\text{RDSTB}}$ = $\overline{\text{WTSTB}}$ = 1

Operational Commands

other than register reads and writes

	Operation	Op Code (DS = 0)	
	Test Triggers - must be in test mode, otherwise no operation results FIFO Reset Test trigger (load) Test trigger (unload)	X10100X	$XX28_H$
	Operational Triggers		
Must be in poll mode	START POLL (from offset)	X10000X	$XX20_H$
	START POLL (from 0) (resets offset reg.) *Reg. Address $000E_H$*	X10001X	$XX22_H$
	CONTINUE POLL (from next address)	X10010X	$XX24_H$
	CONTINUOUS MODE- starts new poll from beginning after "poll op cmplt" INTERRUPT Non-CONTINUOUS - "poll op cmplt" INTERRUPT - then no action		
	Note: Trigger (does not load new cmd WD (1) or transaction) generally used for non chained poll, single transaction in polling mode. This operation will repeat last, then continue.		
Resets	Reset I resets interface only Reset II same as master reset (hardware), also resets chip set	X10111X X10110X	$2E_H$ $2C_H$

Note: All Operational Codes are Write Operations.

BC Criteria for Valid Transactions

Valid Transactions result in generation of GOOD XFER (INT 0) Interrupt.
Invalid Transfer result in generation of INVALID TRANSFER (INT 1) Interrupt.
See Transaction Word for additional Status Word Criterion (i.e. bit masks)

Transaction Type		Specific Validity Criteria
1. Normal Data Transfer		
A. RT to BC		Status, then Valid Message
B. BC to *RT*	(Tx/Rx = 1)	Status
C. Broadcast	(Tx/Rx = 0)	No Status
	(Tx/Rx = 0)	
2. RT to RT Transfer		
A. Normal	(Tx/Rx = 1)	Status, Valid Message,then Status
B. Broadcast	(Tx/Rx = 1)	Status, then Valid Message only
3. Mode (no data)		
A. Normal		Status
B. Broadcast		No Status
4. Mode (associated data)		
A. Normal		Status
B. Broadcast		No Status
5. Mode (returned data)		Status, then returned data

General Validity Criteria - Applies to all transfers

A. Bus must be quiet, i.e. no additional data words, status words or command words after correct RT response before transaction is declared valid.
B. If data is returned, word count, must be correct. Data must also be contiguous, i.e. no gaps.
C. RTU Address(s) must be correct in returned status word(s).
D. RTU must respond within 14µsec (except for non RT to RT Broadcast).
E. No bits set in returned status word(s), except where masked in transaction word.

Interrupts In BC Mode

BC Interrupt Name	Signal Name	Conditions and Actions
Good Transfer	INT 0	1. Indicates fully valid transaction. 2. Initiates next poll operation, when in polling mode.
Invalid Transfer	INT 1	1. Non masked bits set (includes reserved bits). 2. No status (2 for non BCST RT to RT) word returned. 3. Status word has incorrect address. 4. Fail safe time out (1 millisec)for bus (RTU) to go quiet i.e. RTU loudmouthing. 5. Incorrect number of data words. 6. Busy (even if busy masked) when RTU should receive or transmit data. Note: busy mask only masks busy for mode cmds.
Poll Operation Complete	INT 2	1. Indicates end of poll,when end of poll is a valid transaction. 2. Delayed from good transfer interrupt. 3. Initiates poll sequence again (from offset) if in continuous mode. 4. If the I/O command "continue at next transaction" is issued at the last transaction command, this interrupt will be issued.

Interrupts in RTU Mode

RTU Interrupt Name	Signal Name	Conditions and Actions
Valid Message Received	INT 0	1. Indicates the reception of a complete and valid block of data. 2. Interrupt issued after complete block of data has been DMA'd to subsystem memory. 3. Command word for receive data block is located in double buffered receive command register.
SYNC With Data	INT 1	1. Issued after reception of valid SYNCHRONIZE with data mode command. (Interrupt is not generated if word count is high). 2. Command word located in command register. 3. SYNC data word located in SW2/RMD register.
Mode W/O Data	INT 2	1. Indicates reception of mode commands without data that may require subsystem action. These are: SYNCHRONIZE (W/O DATA) RESET DYNAMIC BUS CONTROL ACCEPTANCE 2. Command word located in command register.
Data Transmitted	INT 3	1. Indicates reception of valid transmit command or vector mode command. 2. If issued for transmit command,then issued after DMA. 3. If issued for vector, data transmitted from CW2/AMD/VEC register. 4. Command word located in command register.

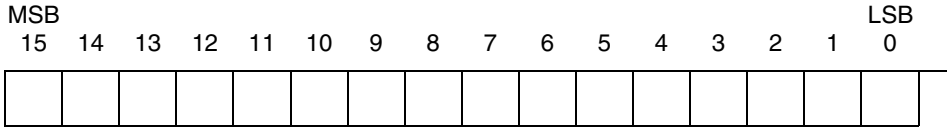
Bus Controller Poll Operation

Internal Triggers	Op Code
Trig A continues operation conditions - transaction -poll op enabled -BC mode	XX24
Trig B begin again (from offset) conditions - transaction = last (TB6 = 0) - poll op enable - BC mode - valid trans interrupt	XX20

Summary of Registers

Register Name	General Function	Op Code
BC Command WD 1 Register	1. Contains the command word for all bus transactions (first for RT to RT transfers). (BC only) 2. Automatically loaded in polling operation.	XX00
CW2 / AMD / VEC Register	1. Used in both RT and BC. 2. Contains second command word for RT to RT transfers. (BC only) 3. Contains associated mode data for mode command requiring transmitted data. (BC only) 4. Optionally automatically loaded in polling operation. (BC only) 5. Contains vector word. (RTU only)	XX02
Transaction Word Register	1. Contains additional information required to fully define a bus transaction, i.e. bus selection, transfer type (normal/mode). (BC only) 2. Automatically loaded in polling operation.	XX0C
Transaction Address Register	1. Contains starting address for BC polling operation.	XX0E
Last Transaction Register	1. Contains address of last transaction. 2. Used to determine where in command stack, a failed transaction command is located.	XX34
Operation Register	1. Sets operational mode i.e. Bus Controller Remote Terminal 2. Control of status word bits in RTU mode: a. BUSY b. SSERR c. SERVRQST	XX0A
Error Latch	1. Contains information on transactions occurring on 1553B bus. 2. Primarily used in bus controller mode. Useful in RTU mode especially during system debugging.	XX32
RTU Command Word Register	1. Contains all commands received by RTU. (RTU only). Includes normal data and mode commands.	XX36
RTU Receive Command Word Register	1. Contains only valid receive commands. (RTU only) 2. Loaded after data block validated. 3. Doubled buffered version of RTU command word register.	XX38
Stat Word 1 Register	1. Contains returned status word. (BC only). 2. Contains first returned status word for RT to RT transfers. (BC only)	XX3C
Stat WD2 / RMD Register	1. Contains second returned status word for RT to RT transfers. (BC only). 2. Contains returned rode data for mode commands. (BC only). Sync word as RTV.	XX3A

Operation Register



1. Power up and reset to busy RTU.

2. Used to define operating mode of 1553 interface, used for both BC and RTU modes

543210
3. Select Code = 00101X 001010 XX0AH $\overline{DS} = 0$

Reg. Bit	Name	Definition
0	$\overline{RT}$/BC	Terminal Mode 0 = RTU Mode 1 = BC Mode
1	POE	Poll Operation Enable Enables Polling Operation in BC Mode 0 = Not Enabled 1 = Enabled
2	CONT POLL	Continuous Poll Operation Enable causes polling operation to continuously loop when enabled and active. 0 = Not Enabled If this bit is reset during an active polling loop, poll will end at completion of polling frame. 1 = Enabled
3	PFO	Poll Fault Overide When not enabled, Poll Operation will halt immediately after a transaction failure. (Invalid Transfer Interrupt Generated). Note: Poll can be restarted, with last (failed transaction) or next transaction. When Enabled, poll will continue even if transaction failed. 0 = Not Enabled 1 = Enabled
4,5	REPEAT	If an Error condition is detected in BC mode, the interface can RETRY the command sequence based on the following table: **Bit 5 / Bit 4 / Repeat Count** 0 / 0 / None 0 / 1 / 1 1 / 0 / 2 1 / 1 / 3 The Interface will continue on to the next Transaction if the prescribed number of REPEAT attempts has transpired and the Error condition is still present.

Operation Register con't

<table>
<tr><th>Reg. Bit</th><th>Name</th><th>Definition</th></tr>
<tr><td>6,7</td><td>TEST</td><td>FIFO Loop Tests

A. 1553 Side Loop
NO DMA occurs

B. SUBYSTEM (Microprocessor) Side Loop

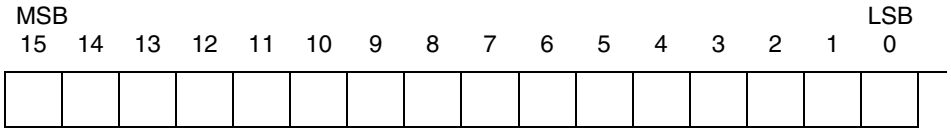
1553 Side Set BUSY
FIFO Exercised via

I/O Test Trigger Load Command
and
I/O Test Trigger Unload Command

<table>
<tr><th>Bit 7</th><th>Bit 6</th><th>Test</th></tr>
<tr><td>0</td><td>0</td><td>RESET</td></tr>
<tr><td>1</td><td>1</td><td>Test A</td></tr>
<tr><td>1</td><td>0</td><td>Test B</td></tr>
<tr><td>0</td><td>1</td><td>Not Valid</td></tr>
</table>
TEST A/$\overline{B}$
TEST ENABLE</td></tr>
<tr><td>8</td><td>NO OP</td><td>NO OPERATION (Wait) when in poll mode (BC).</td></tr>
<tr><td>9</td><td>PACT</td><td>POLL ACTIVE
PACT = 1 indicates that a POLLING operation has been triggered.</td></tr>
<tr><td>10</td><td>DBCACC</td><td>RTU Dynamic Bus Controll Acceptance when set in RTU Mode, Rtu will accept bus control request as per MIL-PRF-1553B
0 = Not Set
1 = Set</td></tr>
<tr><td>11</td><td>SSERR</td><td>Sets subsystem error flag in returned status word (RTU Mode Only).</td></tr>
<tr><td>12</td><td>BUSY</td><td>Sets busy bit in returned status word, inhibits DMA (RTU Mode only).</td></tr>
<tr><td>13</td><td>TRANSACT</td><td>TRANSFER ACTIVITY
TRANSACT = 1 indicates a Transaction has been initiated and is in progress.</td></tr>
<tr><td>14-15</td><td>SERVRQ</td><td>Sets Service Request in returned status word (RTU Mode only).

<table>
<tr><th>Bit 15</th><th>Bit 14</th><th>Flag</th></tr>
<tr><td>0</td><td>0</td><td>NOT Set</td></tr>
<tr><td>0</td><td>1</td><td>SET until reset</td></tr>
<tr><td>1</td><td>0</td><td>Set until VECTOR word is transmitted</td></tr>
<tr><td>1</td><td>1</td><td>Set until reset *</td></tr>
</table>
* Bit 15 is ALWAYS RESET after VECTOR Word is transmitted.</td></tr>
</table>

Error Register



The error Register is reset by: - I/O reg reset command
- I/O reset command
- Power on reset (master reset)
- Initiation of transfer in BC mode

Bit	Name	Indication (When Set)
0*	RTADER	- RTU address Error (Parity)
1*	PARER	- Parity error in command or data word
2*	ERROR	- Any waveform encoding error in received data - Bad Manchester - Bad Parity - Bad Data Sync - Non Contiguity of data
3*	LTFAIL	- Encoding error in terminals transmission - Includes RT address parity
4	HSFAIL	- Subsystem has not acknowledged DMA request in sufficient time.
5	TXTO	- Transmitter timeout error indicates 1553 transmitter has transmitted in excess of 680µsec and terminal fail safe timeout has turned off transmitter. NOTE: 1553B Max. is 800µs. If terminal timeout hardware (RT) fails self test mode command (Indicate self test), this bit will also be set.
6	DMA TO	- DMA Time Out Indicates failure in data transfer between CT1611 and subsystem. If DMA takes longer than 80µsec this flag will be set and DMA will be initiated.

* Additional information for interpretation of Register Bits 0-3.

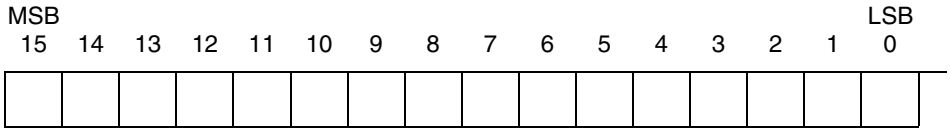
Reg. Bits				Indication
3	2	1	0	
0	1	0	0	Waveform encoding error (Manchester)
0	1	1	0	Data parity error
1	X	X	1	RTU address error

Bit	Name	Definition
7	DBCACC	Dynamic Bus Control Acceptance Active only in RTU mode. Indicates RTU has accepted bus controller request. RTU must switch to BC mode.
8	TRANS TO	Transaction Time Out Active BC mode only Indicates BC transfer has failed due to loopmouthing RTU or non functioning transceive in BC. Occurs approximately 780µsec after transfer is triggered.

Error Register con't

<table>
<tr><th>Bit</th><th>Name</th><th>Indication (When Set)</th></tr>
<tr><td>9</td><td>GBR</td><td>Good Block Received
Active BC mode only
Indicates valid message has been received by bus controller, set even if transaction is otherwise not valid.</td></tr>
<tr><td>10</td><td>RMD</td><td>Received Mode Data
Active only in BC mode
Indicates valid mode data has been returned from RT.
This bit is set even if transaction is otherwise not valid.</td></tr>
<tr><td>11</td><td>BIT SET</td><td>Bit(s) set in returned status word(s). Active in BCC mode only.
Indicates non masked bits in status word(s) are set.
Masked bits are masked in Transaction Word Register.
Bits include:
Message error bit
Instrumentation bit
Service Request
Reserved Bit(s) (3 bits)
Broadcast Cmd Rcvd bit
Busy bit
Subsystem Flag
Dynamic Bus Control Acceptance bit
Terminal Flag</td></tr>
<tr><td>12</td><td>AD ERR</td><td>Address in status word(s) error active only in BC mode.
Indicates RTU address in returned status word(s) is incorrect.</td></tr>
<tr><td>13. 14</td><td>SW CNT</td><td>Returned status word count.
Active only in BC mode.
Two bit non rollover counter for returned status words..
<table>
<tr><th>Bit 14</th><th>Bit 13</th><th>Count</th></tr>
<tr><td>0</td><td>0</td><td>None returned</td></tr>
<tr><td>0</td><td>1</td><td>One returned</td></tr>
<tr><td>1</td><td>0</td><td>Two returned</td></tr>
<tr><td>1</td><td>1</td><td>Three, or greater returned</td></tr>
</table></td></tr>
<tr><td>15</td><td>BUS ACT ERR</td><td>Bus Activity Error
Active in BC mode only.
This bit is set if the bus is active when should be quiet following:
A. Returned mode data (indicates word count high)
B. After status in normal receive, mode without data, and non broadcast RT to RT.</td></tr>
</table>

Transaction Word Register



Used only in BC mode
Contains information not explicitly contained in command word.

Defines:

1. Type of Transfer
2. Selection of bus
   - selects 1 of 4

   Note: Most systems are only dual redundant
3. Continue, for continuous poll operation
4. Conditions for defining an invalid transfer via Bit masks for returned status words.
5. Continue/last control bit for framing poll operations.

This register is loaded via I/O Command. It is also loaded during a Polling Operation, via DMA from the polling command stack.

<table>
<tr><th>Reg. Bit</th><th>Name</th><th>Definition</th></tr>
<tr><td>0 - 2</td><td>TRANS TYPE</td><td>Specifies Transaction Type
<table>
<tr><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Transaction</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>NORMAL Receive or Transmit</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RT to RT</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>No Operation</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Mode WITHOUT data</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>No Operation</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Mode with RETURNED data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>No Operation</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Mode with associated data</td></tr>
</table></td></tr>
<tr><td>3 - 4</td><td>BUS</td><td>Selection of Bus
<table>
<tr><th>Bit 4</th><th>Bit 3</th><th>Bus</th></tr>
<tr><td>0</td><td>0</td><td>"0" or "A"</td></tr>
<tr><td>0</td><td>1</td><td>"1" or "B"</td></tr>
<tr><td>1</td><td>0</td><td>"2" or "C"</td></tr>
<tr><td>1</td><td>1</td><td>"3" or "D"</td></tr>
</table></td></tr>
<tr><td>5</td><td>DMA3RD</td><td>Polling Sequence Option (Polling Mode only)
For use with RT to RT transfers and code with associated data transfers.
When set, during polling sequence, the second command word (for RT to RT transfers) or the data word (for mode with associated data transfers) is loaded from the command stack.
Otherwise the last entry in the second command/and register will be used in transfer.
0 = Not Set
1 = Set</td></tr>
</table>

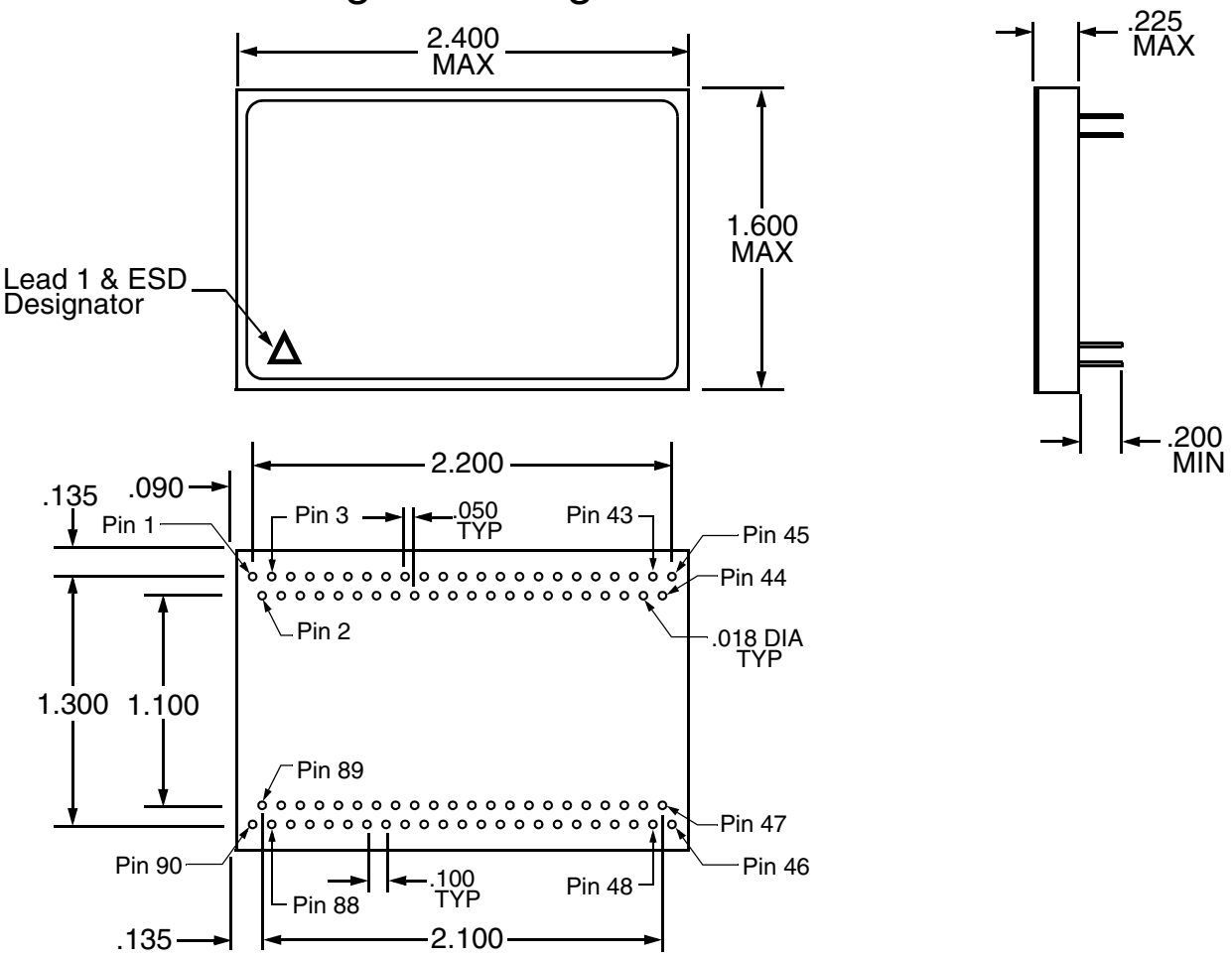
Transaction Word Register con't

<table>
<tr><th>Reg. Bit</th><th>Name</th><th>Definition</th></tr>
<tr><td>6</td><td>POLL CONT</td><td>Poll Operation Continue (Polling Mode only)
When set polling operation will continue with next command in command stack.
When Not Set, polling operation will terminate after transaction is complete. Last transfer in polling sequence must have this bit cleared.
0 = Not Set
1 = Set</td></tr>
<tr><td>7 - 15</td><td>MASK BITS</td><td>Returned Status Word Bit Masks
1 = Masked
0 = Not Masked
When a non masked bit in the returned status word(s) is set the transaction is declared not valid.
<table>
<tr><th>Bit</th><th>Status Bit</th></tr>
<tr><td>7</td><td>Terminal Flag</td></tr>
<tr><td>8</td><td>Dynamic Bus Control Acceptance</td></tr>
<tr><td>9</td><td>Subsystem Flag</td></tr>
<tr><td>10</td><td>Busy Bit *</td></tr>
<tr><td>11</td><td>Broadcast Command Received</td></tr>
<tr><td>12</td><td>Reserved Bits (any or all of 3)</td></tr>
<tr><td>13</td><td>Service Request Bit</td></tr>
<tr><td>14</td><td>Instrumentation Bit</td></tr>
<tr><td>15</td><td>Message Error Bit</td></tr>
</table>
* Note: Setting the busy bit mask will not mask a busy response (i.e. declare it valid). When data is not returned, in response to a transmit command.</td></tr>
</table>

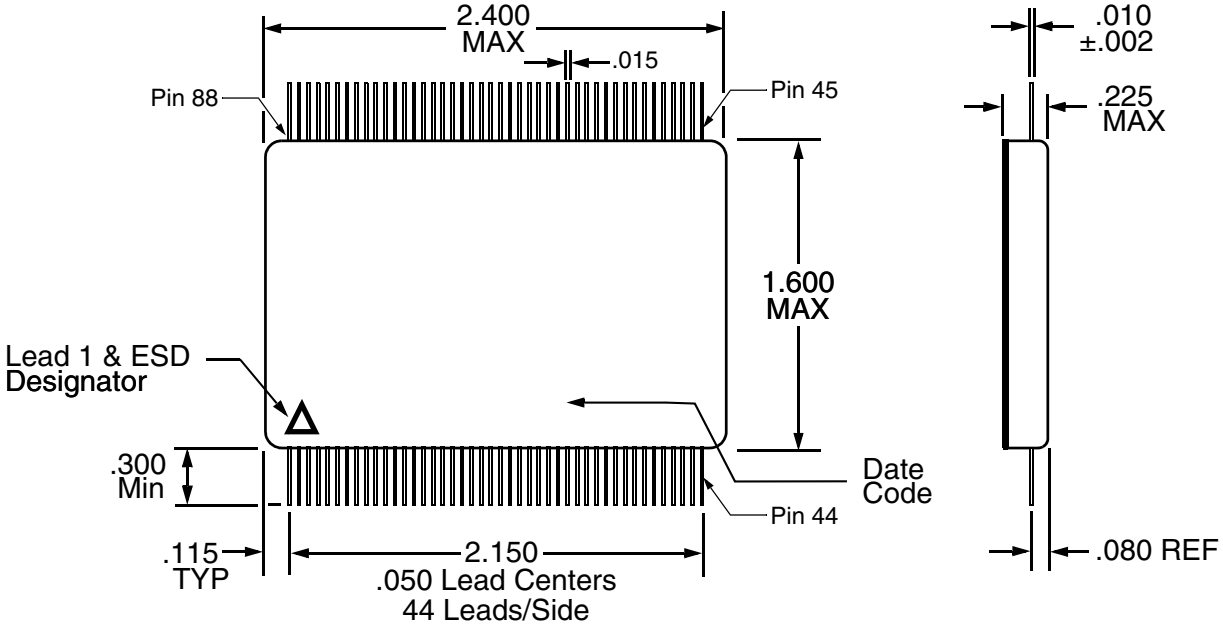
CT1611 – Pinouts vs Function

Pin #		Signal	Pin #		Signal
FP	DIP		FP	DIP	
1	1	$\overline{\text{SSERR}}$	88	90	+5V
2	2	TRANSMIT/$\overline{\text{RECEIVE}}$	87	89	$\overline{\text{BUSY}}$
3	3	POLL/$\overline{\text{DATA}}$	86	88	$\overline{\text{BITEN}}$ /RMDSTB
4	4	$\overline{\text{DS}}$	85	87	$\overline{\text{LSTCMD}}$ /$\overline{\text{CWEN}}$
5	5	R/$\overline{\text{W}}$ /$\overline{\text{RDSTB}}$	84	86	$\overline{\text{HSFAIL}}$
6	6	RDYD	83	85	$\overline{\text{GBR}}$
7	7	$\overline{\text{STRBD}}$ /$\overline{\text{WRSTB}}$ (OUT)	82	84	H/$\overline{\text{L}}$
8	8	$\overline{\text{STRBD}}$ /$\overline{\text{WRSTB}}$ (IN)	81	83	$\overline{\text{STATEN}}$ /STATSTB
9	9	$\overline{\text{ACK}}$	80	82	RT/$\overline{\text{BC}}$
10	10	$\overline{\text{DMA REQ}}$	79	81	$\overline{\text{DBCACC}}$
11	11	$\overline{\text{DMA ACK}}$	78	80	$\overline{\text{TXTO}}$
12	12	DB 0	77	79	$\overline{\text{SERVREQ}}$
13	13	DB 1	76	78	$\overline{\text{INCMD}}$
14	14	DB 2	75	77	$\overline{\text{EOT}}$
15	15	DB 3	74	76	$\overline{\text{DTRQ}}$
16	16	DB 4	73	75	$\overline{\text{VECTEN}}$ /$\overline{\text{DWEN}}$
17	17	DB 5	72	74	$\overline{\text{NBGT}}$
18	18	DB 6	71	73	$\overline{\text{SYNC}}$
19	19	DB 7	70	72	16/$\overline{\text{8}}$
20	20	DB 8	69	71	MODE 1/$\overline{\text{MODE 0}}$
21	21	DB 9	68	70	IUSTB
22	22	DB 10	67	69	$\overline{\text{DTACK}}$
23	23	DB 11	66	68	BCOP A
24	24	DB 12	65	67	$\overline{\text{BCOPSTB}}$
25	25	DB 13	64	66	$\overline{\text{RTADER}}$
26	26	DB 14	63	65	BCOP B
27	27	DB 15	62	64	$\overline{\text{PARER}}$
28	28	AD 0	61	63	$\overline{\text{MANER}}$
29	29	AD 1	60	62	$\overline{\text{LTFAIL}}$
30	30	AD 2	59	61	$\overline{\text{DMA DATA ACK}}$
31	31	AD 3	58	60	CLOCK IN (6MHZ)
32	32	AD 4	57	59	$\overline{\text{RTO}}$
33	33	AD 5	56	58	REQBUS B
34	34	AD 6	55	57	REQBUS A
35	35	AD 7	54	56	$\overline{\text{IHDIR}}$
36	36	AD 8	53	55	$\overline{\text{IHEN}}$
37	37	AD 9	52	54	IH08
38	38	AD 10	51	53	IH19
39	39	$\overline{\text{INT 3}}$	50	52	IH210
40	40	$\overline{\text{INT 1}}$	49	51	IH311
41	41	$\overline{\text{INT 0}}$	48	50	IH412
42	42	$\overline{\text{INT 2}}$	47	49	IH513
43	43	$\overline{\text{MASTER RESET}}$	46	48	IH614
44	44	COMMON/CASE	45	47	IH715
-	45	N/C	-	46	N/C

Plug In Package Outline



Flat Package Outline



Ordering Information

Model No.	Case
CT1611	Plug In
CT1611-FP	Flat Pack

PLAINVIEW, NEW YORK
Toll Free: 800-THE-1553
Fax: 516-694-6715

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

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