Benchmarq Products
from Texas Instruments

bq4802Y/LY

Y2K-Compliant Parallel RTC with CPU Supervisor

Features

- ➤ Real-Time Clock counts seconds through centuries in BCD format
- ➤ bq4802Y—5V operation, bq4802LY—3.3V operation
- ➤ Century register
- ➤ On-chip battery-backup switchover circuit with nonvolatile control for external SRAM
- ➤ Less than 500nA of clock operation current in backup mode
- ➤ Microprocessor reset with push-button override
- ➤ Independent watchdog timer with a programmable time-out period
- ➤ Power-fail interrupt warning
- ➤ Programmable clock alarm interrupt active in battery-backup mode
- ➤ Programmable periodic interrupt
- ➤ Battery-low warning
- ➤ 28-pin SOIC, TSSOP, and SNAPHAT package options

General Description

The bq4802Y/LY Real-Time Clock is a low-power microprocessor peripheral that integrates a time-of-day clock, a century based calendar, and a CPU supervisor in a 28-pin SOIC, TSSOP IC, or SNAPHAT module. The bq4802Y/LY is ideal for fax machines, copiers, industrial control systems, point-of-sale terminals, data loggers, and computers.

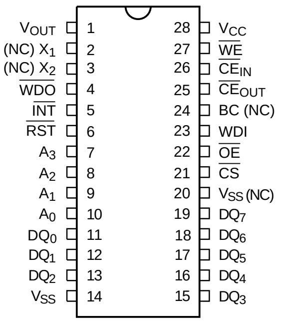
The bq4802Y/LY provides direct connections for a 32.768KHz quartz crystal and a 3V backup battery. Through the use of the conditional chip enable output ($\overline{\mathrm{CE}}_{\mathrm{OUT}}$) and battery voltage output (V_{OUT}) pins, the bq4802Y/LY can write-protect and make nonvolatile external SRAMs. The backup cell powers the real-time clock and maintains SRAM information in the absence of system voltage. The crystal and battery are contained within the modules for a more integrated solution

The bq4802Y/LY contains a temperature-compensated reference and comparator circuit that monitors the status of its voltage supply. When the bq4802Y/LY detects an out-of-tolerance condition, it generates an interrupt warning and subsequently a microprocessor reset. The reset stays active for 200ms after V_{CC} rises within tolerance, to allow for power supply and processor stabilization. The reset function also allows for an external push-button override

The bq4802Y/LY also has a built-in watchdog timer to monitor processor operation. If the microprocessor does not toggle the watchdog input (WDI) within the programmed time-out period, the bq4802Y/LY asserts $\overline{\mathrm{WDO}}$ and $\overline{\mathrm{RST}}$. WDI unconnected disables the watchdog timer.

The bq4802Y/LY can generate other interrupts based on a clock alarm condition, periodic setting, or watchdog timer. The alarm interrupt can be set to occur from once per second to once per month. The alarm can be made active in the battery-backup mode to serve as a system wake-up call. For interrupts at a rate beyond once per second, the periodic interrupt can be programmed with periods of 30.5µs to 500ms.

Pin Connections



28-pin, SOIC, TSSOP or SNAPHAT

SLUS464A—August 2000—Revised October 2000

Pin Names

A_0–A_3	Clock/control address inputs
DQ_0–DQ_7	Data inputs/outputs
$\overline{\mathrm{WE}}$	Write enable input
$\overline{\mathrm{OE}}$	Output enable input
$\overline{\mathrm{CS}}$	Chip select input
$\overline{\mathrm{CE}}_{\mathrm{IN}}$	External RAM chip enable input
$\overline{\mathrm{CE}}_{\mathrm{OUT}}$	Conditional RAM chip enable output
X1–X2	Crystal inputs
BC	Backup battery input
V_{OUT}	Back-up battery output
$\overline{\mathrm{INT}}$	Interrupt output
$\overline{\mathrm{RST}}$	Microprocessor reset output
WDI	Watchdog input
$\overline{\mathrm{WDO}}$	Watchdog output
V_{CC}	Input supply voltage
V_{SS}	Ground
NC	No connect

Pin Descriptions

X1–X2 **Crystal inputs**

X1–X2 are a direct connection for a 32.768kHZ, 6pF crystal. Not accessible in module packages.

$\overline{\text{RST}}$ **Reset output**

$\overline{\text{RST}}$ goes low whenever V_{CC} falls below the power fail threshold. $\overline{\text{RST}}$ will remain low for 200ms (typical) after V_{CC} crosses the threshold on power-up. The bq4802Y/LY will also enter the reset cycle when $\overline{\text{RST}}$ is released from being pulled low for more than 1µs.

$\overline{\text{INT}}$ **Interrupt output**

$\overline{\text{INT}}$ goes low when a power fail, periodic, or alarm condition occurs. $\overline{\text{INT}}$ is an open-drain output.

WDI **Watchdog input**

WDI is a three-level input. If WDI remains either high or low for longer than the watchdog time-out period (1.5 seconds default), $\overline{\text{WDO}}$ goes low. $\overline{\text{WDO}}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and V_{SS}, which sets it to mid-supply when left unconnected.

$\overline{\text{WDO}}$ **Watchdog output**

$\overline{\text{WDO}}$ goes low if WDI remains either high or low longer than the watchdog time-out period. $\overline{\text{WDO}}$ returns high on the next transition at WDI. $\overline{\text{WDO}}$ remains high if WDI is unconnected.

A_0–A_3 **Clock address inputs**

A_0–A_3 allow access to the 16 bytes of real-time clock and control registers.

DQ_0–DQ_7 **Data input and output**

DQ_0–DQ_7 provide x8 data for real-time clock information. These pins connect to the memory data bus.

V_{SS} **Ground**

$\overline{\text{CS}}$ **Chip select**

$\overline{\text{OE}}$ **Output enable**

$\overline{\text{OE}}$ provides the read control for the RTC memory locations.

$\overline{\text{CE}}_{OUT}$ **Chip enable output**

$\overline{\text{CE}}_{OUT}$ goes low only when $\overline{\text{CE}}_{IN}$ is low and V_{CC} is above the power fail threshold. If $\overline{\text{CE}}_{IN}$ is low, and power fail occurs, $\overline{\text{CE}}_{OUT}$ stays low for 100µs or until $\overline{\text{CE}}_{IN}$ goes high, whichever occurs first.

$\overline{\text{CE}}_{IN}$ **Chip enable input**

$\overline{\text{CE}}_{IN}$ is the input to the chip-enable gating circuit.

BC **Backup battery input**

BC should be connected to a 3V backup cell. A voltage within the V_{BC} range on the BC pin should be present upon power up to provide proper oscillator start-up. Not accessible in module packages.

V_{OUT} **Output supply voltage**

V_{OUT} provides the higher of V_{CC} or V_{BC}, switched internally, to supply external RAM.

$\overline{\text{WE}}$ **Write enable**

$\overline{\text{WE}}$ provides the write control for the RTC memory locations.

V_{CC} **Input supply voltage**

5V input or 3.3V input

Functional Description

Figure 1 is a block diagram of the bq4802Y/LY. The following sections describe the bq4802Y/LY functional operation including clock interface, data-retention modes, power-on reset timing, watchdog timer activation, and interrupt generation.

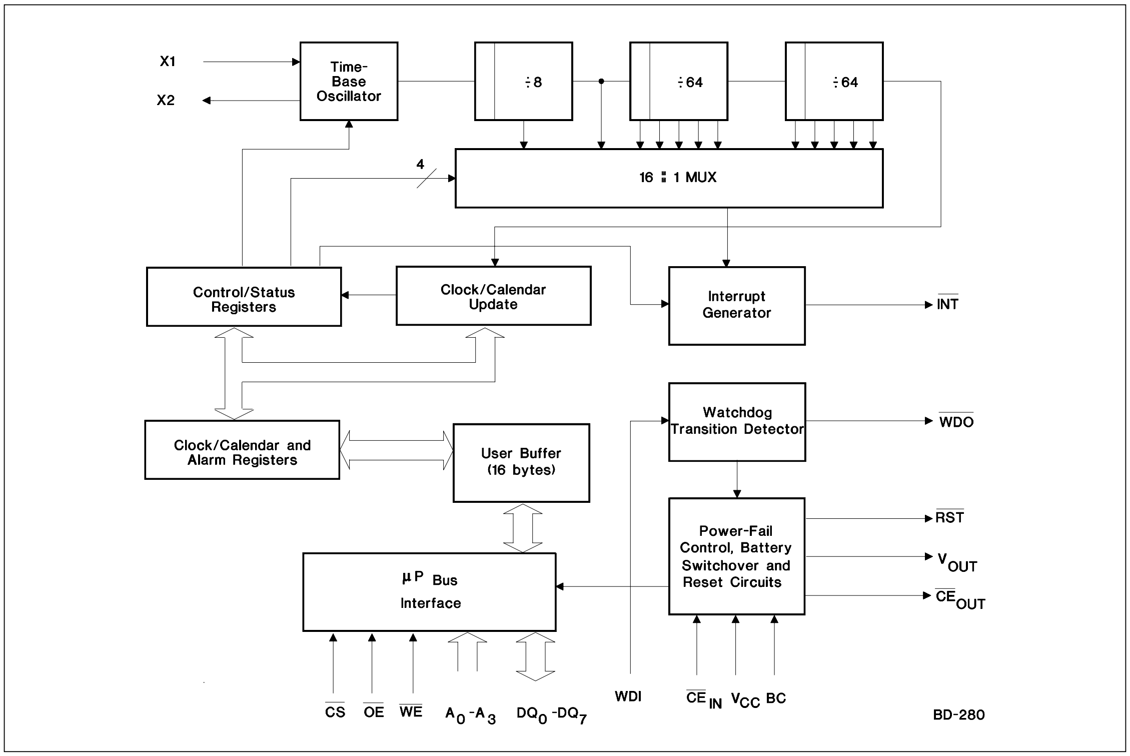


Figure 1. Block Diagram

Truth Table

V_{CC}	$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{CE}}_{OUT}$	V_{OUT}	Mode	DQ	Power
< V_{CC} (max.)	V_{IH}	X	X	$\overline{\text{CE}}_{IN}$	V_{OUT1}	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	$\overline{\text{CE}}_{IN}$	V_{OUT1}	Write	D_{IN}	Active
> V_{CC} (min.)	V_{IL}	V_{IL}	V_{IH}	$\overline{\text{CE}}_{IN}$	V_{OUT1}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	$\overline{\text{CE}}_{IN}$	V_{OUT1}	Read	High Z	Active
< V_{PFD} (min.) > V_{SO}	X	X	X	V_{OH}	V_{OUT1}	Deselect	High Z	CMOS standby
≤ V_{SO}	X	X	X	V_{OHB}	V_{OUT2}	Deselect	High Z	Battery-backup mode

Address Map

The bq4802Y/LY provides 16 bytes of clock and control status registers. Table 1 is a map of the bq4802Y/LY registers, and Table 2 describes the register bits.

Clock Memory Interface

The bq4802Y/LY has the same interface for clock/calendar and control information as standard SRAM. To read and write to these locations, the user must put the bq4802Y/LY in the proper mode and meet the timing requirements.

Read Mode

The bq4802Y/LY is in read mode whenever $\overline{OE}$ (Output enable) is low and $\overline{CS}$ (chip select) is low. The unique address, specified by the 4 address inputs, defines which one of the 16 clock/calendar bytes is to be accessed. The bq4802Y/LY makes valid data available at the data I/O pins within t_{AA} (address access time). This occurs after the last address input signal is stable, and providing the $\overline{CS}$ and $\overline{OE}$ (output enable) access times are met. If the $\overline{CS}$ and $\overline{OE}$ access times are not met, valid data is available after the latter of chip select access time (t_{ACS}) or output enable access time (t_{OE}).

$\overline{CS}$ and $\overline{OE}$ control the state of the eight three-state data I/O signals. If the outputs are activated before t_{AA},

Table 1. bq4802Y/LY Clock and Control Register Map

Address (h)	D7	D6	D5	D4	D3	D2	D1	D0	12-Hour Range (h)	Register
0	0	10-second digit			1-second digit				00–59	Seconds
1	ALM1	ALM0 10-second digit			1-second digit				00–59	Seconds alarm
2	0	10-minute digit			1-minute digit				00–59	Minutes
3	ALM1	ALM0 10-minute digit			1-minute digit				00–59	Minutes alarm
4	PM/AM	0	10-hour digit		1-hour digit				01–12 AM/ 81– 92 PM	Hours
5	ALM1 PM/AM	ALM0	10-hour digit		1-hour digit				01–12 AM/ 81–92 PM	Hours alarm
6	0	0	10-day digit		1-day digit				01–31	Day
7	ALM1	ALM0	10-day digit		1-day digit				01–31	Day alarm
8	0	0			0	Day-of-week digit			01–07	Day-of-week
9	0	0	0	10 mo.	1-month digit				01–12	Month
A	10-year digit				1-year digit				00–99	Year
B	*	WD2	WD1	WD0	RS3	RS2	RS1	RS0		Programmable rates
C	*	*			AIE	PIE	PWRIE	ABE		Interrupt enables
D	*	*			AF	PF	PWRF	BVF		Flags
E	*	*			UTI	$\overline{STOP}$	24/12	DSE		Control
F	10-century digit				1-century digit					Century

Notes:
* = Unused bits; unwritable and read as 0.
0 = should be set to 0 for valid time/calendar range.
Clock calendar data in BCD. Automatic leap year adjustment up to year 2100.
PM/AM = 1 for PM; PM/AM = 0 for AM.
DSE = 1 enables daylight savings adjustment.
24/12 = 1 enables 24-hour data representation; 24/12 = 0 enables 12-hour data representation.
Day-of-Week coded as Sunday = 1 through Saturday = 7.
BVF = 1 for valid battery.
$\overline{STOP}$ = 1 turns the RTC on; $\overline{STOP}$ = 0 stops the RTC in back-up mode.

Table 2. Clock and Control Register Bits

Bits	Description
24/12	24- or 12-hour representation
ABE	Alarm interrupt enable in battery-backup mode
AF	Alarm interrupt flag
AIE	Alarm interrupt enable
ALM0–ALM1	Alarm mask bits
BVF	Battery-valid flag
DSE	Daylight savings time enable
PF	Periodic interrupt flag
PIE	Periodic interrupt enable
PM/AM	PM or AM indication
PWRF	Power-fail interrupt flag
PWRIE	Power-fail interrupt enable
RS0–RS3	Periodic interrupt rate
$\overline{STOP}$	Oscillator stop and start
UTI	Update transfer inhibit
WD0 - WD2	Watchdog time-out rate

the data lines are driven to an indeterminate state until t_{AA}. If the address inputs are changed while $\overline{CS}$ and $\overline{OE}$ remain low, output data remains valid for t_{OH} (output data hold time), but goes indeterminate until the next address access.

Write Mode

The bq4802Y/LY is in write mode whenever $\overline{WE}$ and $\overline{CS}$ are active. The start of a write is referenced from the latter-occurring falling edge of $\overline{WE}$ or $\overline{CS}$. A write is terminated by the earlier rising edge of $\overline{WE}$ or $\overline{CS}$. The addresses must be held valid throughout the cycle. $\overline{CS}$ or $\overline{WE}$ must return high for a minimum of t_{WR2} from $\overline{CS}$ or t_{WR1} from $\overline{WE}$ prior to the initiation of another read or write cycle.

Data-in must be valid t_{DW} prior to the end of write and remain valid for t_{DH1} or t_{DH2} afterward. $\overline{OE}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{CS}$ and $\overline{OE}$, a low on $\overline{WE}$ disables the outputs t_{WZ} after $\overline{WE}$ falls.

Reading the Clock

Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4802Y/LY clock registers should be halted. Updating is halted by setting the update transfer inhibit (UTI) bit D3 of the control register E. As long as the UTI bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the UTI bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the UTI bit, reading the clock locations has no effect on clock accuracy. Once the UTI bit is reset to 0, the internal registers update within one second the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

Setting the Clock

The UTI bit must also be used to set the bq4802Y/LY clock. Once set, the locations can be written with the desired information in BCD format. Resetting the UTI bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second.

Stopping and Starting the Clock Oscillator

The bq4802Y/LY clock can be programmed to turn off when the part goes into battery back-up mode by setting $\overline{STOP}$ to 0 prior to power down. If the board using the bq4802Y/LY is to spend a significant period of time in storage, the $\overline{STOP}$ bit can be used to preserve some battery capacity. $\overline{STOP}$ set to 1 keeps the clock running when V_{CC} drops below V_{SO}. With V_{CC} greater than V_{SO}, the bq4802Y/LY clock runs regardless of the state of $\overline{STOP}$.

Power-Down/Power-Up Cycle

The bq4802Y/LY continuously monitors V_{CC} for out-of-tolerance. During a power failure, when V_{CC} falls below V_{PFD}, the bq4802Y/LY write-protects the clock and storage registers. The power source is switched to BC when V_{CC} is less than V_{PFD} and BC is greater than V_{PFD}, or when V_{CC} is less than V_{BC} and V_{BC} is less than V_{PFD}. RTC operation and storage data are sustained by a valid backup energy source. When V_{CC} is above V_{PFD}, the power source is V_{CC}. Write-protection continues for t_{CSR} time after V_{CC} rises above V_{PFD}.

An external CMOS static RAM is battery-backed using the V_{OUT} and chip enable output pins from the bq4802Y/LY. As the voltage input V_{CC} slews down during a power failure, the chip enable output, $\overline{CE}_{OUT}$, is forced inactive independent of the chip enable input $\overline{\text{CE}}_{\text{IN}}$.

This activity unconditionally write-protects the external SRAM as V_{CC} falls below V_{PFD}. If a memory access is in progress to the external SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time t_{WPT}, the chip enable output is unconditionally driven high, write-protecting the controlled SRAM.

As the supply continues to fall past V_{PFD}, an internal switching device forces V_{OUT} to the external backup energy source. $\overline{\text{CE}}_{\text{OUT}}$ is held high by the V_{OUT} energy source.

During power-up, V_{OUT} is switched back to the main supply as V_{CC} rises above the backup cell input voltage sourcing V_{OUT}. If $V_{PFD} < V_{BC}$ on the bq4802Y/LY the switch to the main supply occurs at V_{PFD}. $\overline{\text{CE}}_{\text{OUT}}$ is held inactive for time t_{CER} (200ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{\text{CE}}_{\text{IN}}$ input, to allow for processor stabilization.

During power-valid operation, the $\overline{\text{CE}}_{\text{IN}}$ input is passed through to the $\overline{\text{CE}}_{\text{OUT}}$ output with a propagation delay of less than 12ns.

Figure 2 shows the hardware hookup for the external RAM, battery, and crystal.

A primary backup energy source input is provided on the bq4802Y/LY. The BC input accepts a 3V primary battery, typically some type of lithium chemistry. Since the bq4802Y/LY provides for reverse battery charging protection, no diode or current limiting resistor is needed in series with the cell. To prevent battery drain when there is no valid data to retain, V_{OUT} and $\overline{\text{CE}}_{\text{OUT}}$ are internally isolated from BC by the initial connection of a battery. Following the first application of V_{CC} above V_{PFD}, this isolation is broken, and the backup cell provides power to V_{OUT} and $\overline{\text{CE}}_{\text{OUT}}$ for the external SRAM.

The crystal should be located as close to X1 and X2 as possible and meet the specifications in the Crystal Specification Table. With the specified crystal, the bq4802Y/LY RTC will be accurate to within one minute per month at room temperature. In the absence of a crystal, a 32.768 kHz waveform can be fed into X1 with X2 grounded.

The power source and crystal are integrated into the SNAPHAT modules.

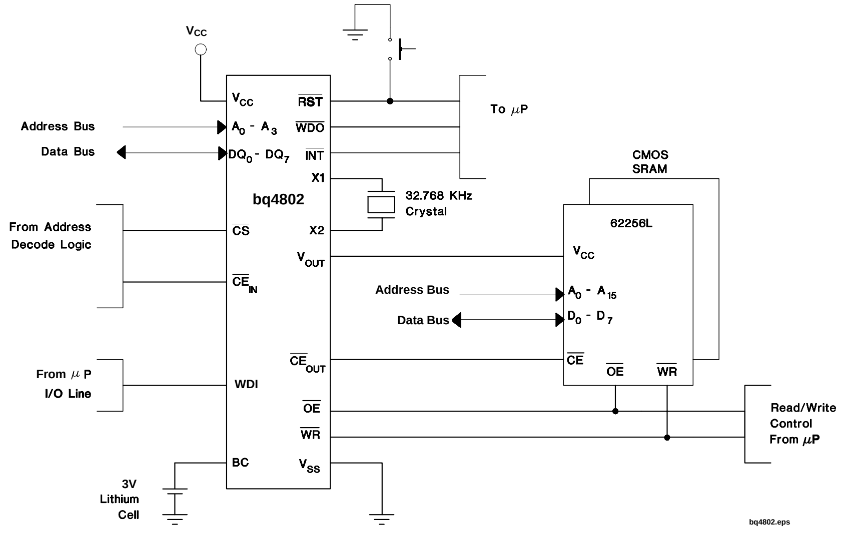


Figure 2. bq4802Y/LY Application Circuit

Power-On Reset

The bq4802Y/LY provides a power-on reset, which pulls the $\overline{\text{RST}}$ pin low on power-down and remains low on power-up for t_{RST} after V_{CC} passes V_{PFD}. With valid battery voltage on BC, $\overline{\text{RST}}$ remains valid for $V_{CC} = V_{SS}$.

Push-Button Reset

The bq4802Y/LY also provides a push-button override to the Reset when the device is not already in a reset cycle. When the $\overline{\text{RST}}$ pin is released after being pulled low for 1µs then the $\overline{\text{RST}}$ will stay low for 200ms (typical).

Watchdog Timer

The watchdog monitors microprocessor activity through the Watchdog input (WDI). To use the watchdog function, connect WDI to a bus line or a microprocessor I/O line. If WDI remains high or low for longer than the watchdog time-out period (1.5 seconds default), the bq4802Y/LY asserts $\overline{\text{WDO}}$ and $\overline{\text{RST}}$.

Watchdog Input

The bq4802Y/LY resets the watchdog timer if a change of state (high to low, low to high, or a minimum 100ns pulse) occurs at the Watchdog input (WDI) during the watchdog period. The watchdog time-out is set by WD0-WD2 in register B. The bq4802Y/LY maintains the watchdog time-out programming through power cycles. The default state (no valid battery power) of WD0-WD2 is 000 or 1.5s on power-up. Table 3 shows the programmable watchdog time-out rates. The watchdog time-out period immediately after a reset is equal to the programmed watchdog time-out.

To disable the watchdog function, leave WDI floating. An internal resistor network (100kΩ equivalent impedance at WDI) biases WDI to approximately 1.6V. Internal comparators detect this level and disable the watchdog timer. When V_{CC} is below the power-fail threshold, the bq4802Y/LY disables the watchdog function and disconnects WDI from its internal resistor network, thus making it high impedance.

Watchdog Output

The Watchdog output ($\overline{\text{WDO}}$) remains high if there is a transition or pulse at WDI during the watchdog time-out period. The bq4802Y/LY disables the watchdog function and $\overline{\text{WDO}}$ is a logic high when V_{CC} is below the power fail threshold, battery-backup mode is enabled, or WDI is an open circuit. In watchdog mode, if no transition occurs at WDI during the watchdog time-out period, the bq4802Y/LY asserts $\overline{\text{RST}}$ for the reset time-out period t_1. $\overline{\text{WDO}}$ goes low and remains low until the next transition at WDI. If WDI is held high or low indefi-

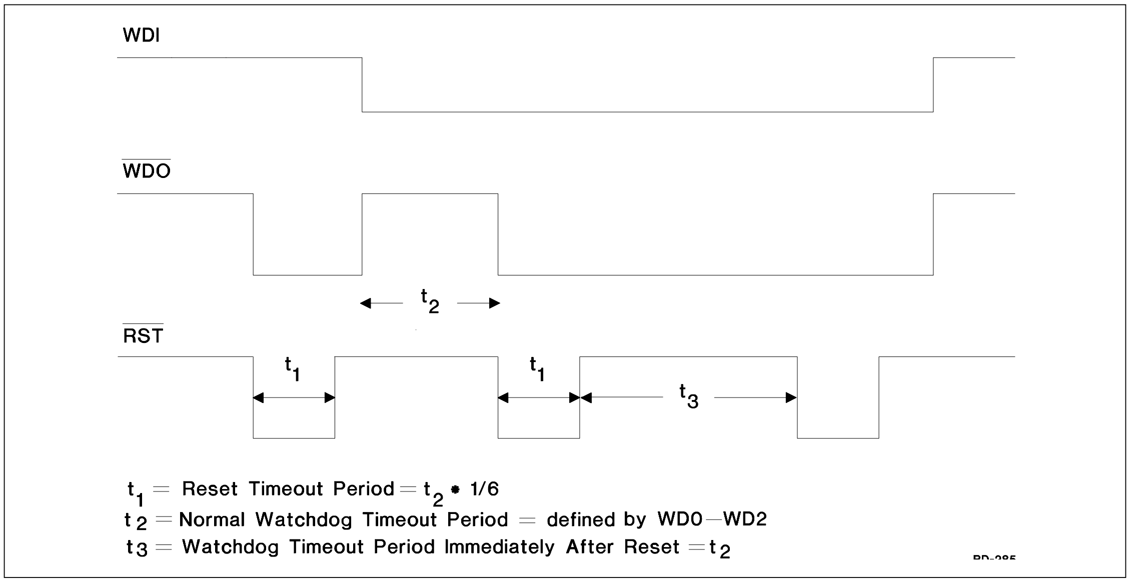


Figure 3. Watchdog Time-out Period and Reset Active Time

nitely, $\overline{\text{RST}}$ will generate pulses (t_1 seconds wide) every t_3 seconds. Figure 3 shows the watchdog timing.

Interrupts

The bq4802Y/LY allows three individually selected interrupt events to generate an interrupt request on the $\overline{\text{INT}}$ pin. These three interrupt events are:

The periodic interrupt, programmable to occur once every 30.5µs to 500ms

The alarm interrupt, programmable to occur once per second to once per month

The power-fail interrupt, which can be enabled to be asserted when the bq4802Y/LY detects a power failure

The periodic, alarm, and power-fail interrupts are enabled by an individual interrupt-enable bit in register C, the interrupts register. When an event occurs, its event flag bit in the flags register, register D, is set. If the corresponding event enable bit is also set, then an interrupt request is generated. Reading the flags register clears all flag bits and makes $\overline{\text{INT}}$ high impedance. To reset the flag register, the bq4802Y/LY addresses must be held stable at register D for at least 50ns to avoid inadvertent resets.

Periodic Interrupt

Bits RS3–RS0 in the interrupts register program the rate for the periodic interrupt. The user can interpret the interrupt in two ways: either by polling the flags register for PF assertion or by setting PIE so that $\overline{\text{INT}}$ goes active when the bq4802Y/LY sets the periodic flag. Reading the flags register resets the PF bit and returns $\overline{\text{INT}}$ to the high-impedance state. Table 4 shows the periodic rates.

Alarm Interrupt

Registers 1, 3, 5, and 7 program the real-time clock alarm. During each update cycle, the bq4802Y/LY compares the date, hours, minutes, and seconds in the clock registers with the corresponding alarm registers. If a match between all the corresponding bytes is found, the alarm flag AF in the flags register is set. If the alarm interrupt is enabled with AIE, an interrupt request is generated on $\overline{\text{INT}}$. The alarm condition is cleared by a read to the flags register. ALM1 – ALM0 in the alarm registers, mask each alarm compare byte. An alarm byte is masked by setting ALM1 (D7) and ALM0 (D6) to 1. Alarm byte masking can be used to select the frequency of the alarm interrupt, according to Table 5.

The alarm interrupt can be made active while the bq4802Y/LY is in the battery-backup mode by setting ABE in the interrupts register. Normally, the $\overline{\text{INT}}$ pin goes high-impedance during battery backup. With ABE set, however, $\overline{\text{INT}}$ is driven low if an alarm condition occurs and the AIE bit is set.

Power-Fail Interrupt

When V_{CC} falls to the power-fail-detect point, the power-fail flag PWRF is set. If the power-fail interrupt enable bit (PWRIE) is also set, then $\overline{\text{INT}}$ is asserted low. The power-fail interrupt occurs t_{WPT} before the bq4802Y/LY generates a reset and deselects.

Battery-Low Warning

The bq4802Y/LY checks the battery on power-up. When the battery voltage is approximately 2.1V, the battery-valid flag BVF in the flags register is set to a 0 indicating that clock and RAM data may be invalid.

Table 3. Watchdog Time-out Rates

WD2	WD1	WD0	Normal Watchdog Time-out Period (t_2, t_3)	Reset Time-out Period (t_1)
0	0	0	1.5s	0.25s
0	0	1	23.4375ms	3.9063ms
0	1	0	46.875ms	7.8125ms
0	1	1	93.75ms	15.625ms
1	0	0	187.5ms	31.25ms
1	0	1	375ms	62.5ms
1	1	0	750ms	125ms
1	1	1	3s	0.5s

Table 4. Periodic Interrupt Rates

Register B Bits				Periodic Interrupt	
RS3	**RS2**	**RS1**	**RS0**	**Period**	**Units**
0	0	0	0	None	
0	0	0	1	30.5175	µs
0	0	1	0	61.035	µs
0	0	1	1	122.070	µs
0	1	0	0	244.141	µs
0	1	0	1	488.281	µs
0	1	1	0	976.5625	µs
0	1	1	1	1.95315	ms
1	0	0	0	3.90625	ms
1	0	0	1	7.8125	ms
1	0	1	0	15.625	ms
1	0	1	1	31.25	ms
1	1	0	0	62.5	ms
1	1	0	1	125	ms
1	1	1	0	250	ms
1	1	1	1	500	ms

Table 5. Alarm Frequency (Alarm Bits D6 and D7 of Alarm Registers)

1h	3h	5h	7h	
ALM1 ALM0	**ALM1 ALM0**	**ALM1 ALM0**	**ALM1 ALM0**	**Alarm Frequency**
1	1	1	1	Once per second
0	1	1	1	Once per minute when seconds match
0	0	1	1	Once per hour when minutes, and seconds match
0	0	0	1	Once per day when hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 6.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 6.0	V	$V_T \leq V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +70	°C	Commercial
T_{STG}	Storage temperature	-55 to +125	°C	
T_{BIAS}	Temperature under bias	-40 to +85	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	bq4802Y
		2.7	3.3	3.6	V	bq4802LY
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	$V_{CC} + 0.3$	V	
V_{BC}	Backup cell voltage	2.4	-	4.0	V	
V_{PBRL}	Push button reset input low	-0.3	-	0.4	V	
V_{PBRH}	Push button reset input high	2.2		$V_{CC} + 0.3$	V	

Note: Typical values indicate operation at $T_A = 25°C$.

DC Electrical Characteristics ($T_A = T_{OPR}$, $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current	-	-	± 1	µA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
V_{OH}	Output high voltage	2.2	-	-	V	$I_{OH} = -2.0$ mA
V_{OHB}	$V_{OH,}$ BC Supply	V_{BC}- 0.3	-	-	V	$V_{BC} > V_{CC}$, $I_{OH} = -10\mu A$
V_{OL}	Output low voltage	-	-	0.4	V	$I_{OL} = 4.0$ mA
I_{CC}	Operating supply current	-	5	9	mA	Min. cycle, duty = 100%, $\overline{CS} = V_{IL}$, $I_{I/O} = 0$mA
I_{SB1}	Standby supply current	-	3	-	mA	$\overline{CS} = V_{IH}$
I_{SB2}	Standby supply current	-	1.5	-	mA	$\overline{CS} \geq V_{CC} - 0.2V$, $0V \leq V_{IN} \leq 0.2V$, or $V_{IN} \geq V_{CC} - 0.2V$
V_{SO}	Supply switch-over voltage	-	V_{PFD}	-	V	$V_{BC} > V_{PFD}$
			V_{BC}	-	V	$V_{BC} < V_{PFD}$
I_{CCB}	Battery operation current	-	0.3	0.5	µA	$V_{BC} = 3V$, $T_A = 25°C$, no load on V_{OUT} or $\overline{CE}_{OUT}$
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.5	V	bq4802Y
		2.4	2.53	2.65	V	bq4802LY
V_{OUT1}	V_{OUT} voltage	V_{CC} - 0.3V	-	-	V	$I_{OUT} = 80$mA, $V_{CC} > V_{BC}$
V_{OUT2}	V_{OUT} voltage	V_{BC} - 0.3V	-	-	V	$I_{OUT} = 100\mu A$, $V_{CC} < V_{BC}$
V_{RST}	$\overline{RST}$ output voltage	-	-	0.4V	-	$I_{RST} = 4$mA
V_{INT}	$\overline{INT}$ output voltage	-	-	0.4V	-	$I_{INT} = 4$mA
V_{WDO}	$\overline{WDO}$ output voltage	-	-	0.4V	-	$I_{SINK} = 4$mA
		2.4	-	-	-	$I_{SOURCE} = 2$mA
I_{WDIL}	Watchdog input low current	-50	-10	-	µA	$0 < V_{WDI} < 0.8V$
I_{WDIH}	Watchdog input high current	-	20	50	µA	$2.2 < V_{WDI} < V_{CC}$

Notes: Typical values indicate operation at $T_A = 25°C$, $V_{CC} = 3.3V$.
RST and $\overline{INT}$ are open-drain outputs.

Crystal Specifications (DT-26 or Equivalent)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_O	Oscillation frequency	-	32.768	-	kHz
C_L	Load capacitance	-	6	-	pF
T_P	Temperature turnover point	20	25	30	°C
k	Parabolic curvature constant	-	-	-0.042	ppm/°C
Q	Quality factor	40,000	70,000	-	
R_1	Series resistance	-	-	45	KΩ
C_0	Shunt capacitance	-	1.1	1.8	pF
C_0/C_1	Capacitance ratio	-	430	600	
D_L	Drive level	-	-	1	µW
$\Delta f/f_O$	Aging (first year at 25°C)	-	1	-	ppm

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 3.3V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	7	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	5	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions—bq4802Y/LY

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

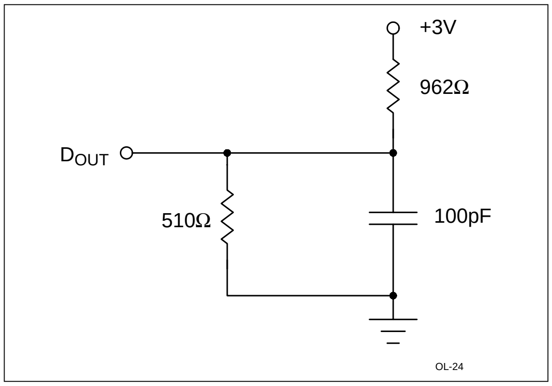


Figure 4. Output Load A

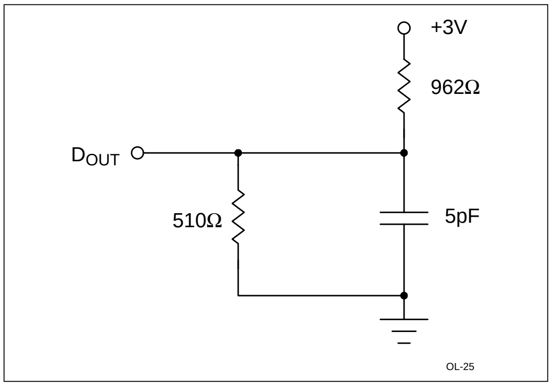


Figure 5. Output Load B

Read Cycle ($T_A = T_{OPR}$, $V_{CC} = 5V$)

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RC}	Read cycle time	200	-	ns	
t_{AA}	Address access time	-	100	ns	Output load A
t_{ACS}	Chip select access time	-	100	ns	Output load A
t_{OE}	Output enable to output valid	-	100	ns	Output load A
t_{CLZ}	Chip select to output in low Z	8	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	ns	Output load B
t_{CHZ}	Chip deselect to output in high Z	0	45	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	45	ns	Output load B
t_{OH}	Output hold from address change	10	-	ns	Output load A

Write Cycle ($T_A = T_{OPR}$, $V_{CC} = 5V$)

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WC}	Write cycle time	200	-	ns	
t_{CW}	Chip select to end of write	195	-	ns	(1)
t_{AW}	Address valid to end of write	195	-	ns	(1)
t_{AS}	Address setup time	30	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	165	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CS}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	50	-	ns	Measured to first low-to-high transition of either $\overline{CS}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CS}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	45	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	ns	I/O pins are in output state. (5)

Notes:

1. A write ends at the earlier transition of $\overline{CS}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

Read Cycle (T_A = T_{OPR}, V_{CC} = 3.3V)

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RC}	Read cycle time	300	-	ns	
t_{AA}	Address access time	-	150	ns	Output load A
t_{ACS}	Chip select access time	-	150	ns	Output load A
t_{OE}	Output enable to output valid	-	150	ns	Output load A
t_{CLZ}	Chip select to output in low Z	15	-	ns	Output load B
t_{OLZ}	Output enable to output in low Z	0	-	ns	Output load B
t_{CHZ}	Chip deselect to output in high Z	0	60	ns	Output load B
t_{OHZ}	Output disable to output in high Z	0	60	ns	Output load B
t_{OH}	Output hold from address change	18	-	ns	Output load A

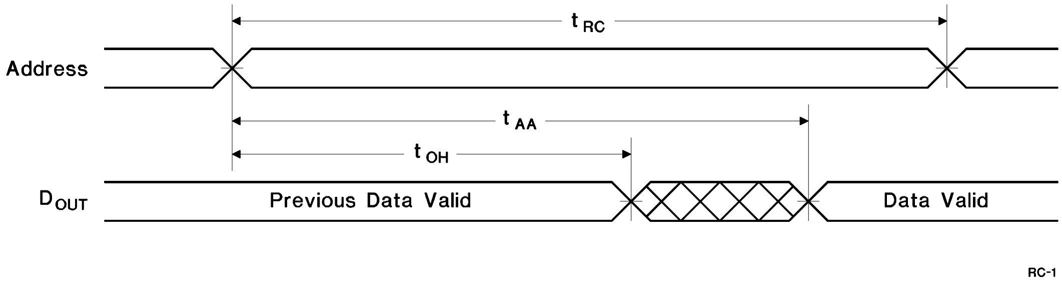
Write Cycle (T_A = T_{OPR} , V_{CC} = 3.3V)

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WC}	Write cycle time	300	-	ns	
t_{CW}	Chip select to end of write	250	-	ns	(1)
t_{AW}	Address valid to end of write	250	-	ns	(1)
t_{AS}	Address setup time	56	-	ns	Measured from address valid to beginning of write. (2)
t_{WP}	Write pulse width	280	-	ns	Measured from beginning of write to end of write. (1)
t_{WR1}	Write recovery time (write cycle 1)	8	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t_{WR2}	Write recovery time (write cycle 2)	25	-	ns	Measured from $\overline{CS}$ going high to end of write cycle. (3)
t_{DW}	Data valid to end of write	80	-	ns	Measured to first low-to-high transition of either $\overline{CS}$ or $\overline{WE}$.
t_{DH1}	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t_{DH2}	Data hold time (write cycle 2)	15	-	ns	Measured from $\overline{CS}$ going high to end of write cycle. (4)
t_{WZ}	Write enabled to output in high Z	0	60	ns	I/O pins are in output state. (5)
t_{OW}	Output active from end of write	0	-	ns	I/O pins are in output state. (5)

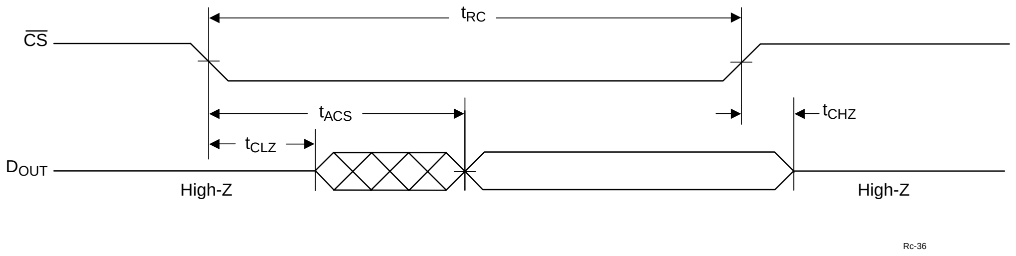
Notes:

1. A write ends at the earlier transition of $\overline{CS}$ going high and $\overline{WE}$ going high.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low and $\overline{WE}$ going low.
3. Either t_{WR1} or t_{WR2} must be met.
4. Either t_{DH1} or t_{DH2} must be met.
5. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high-impedance state.

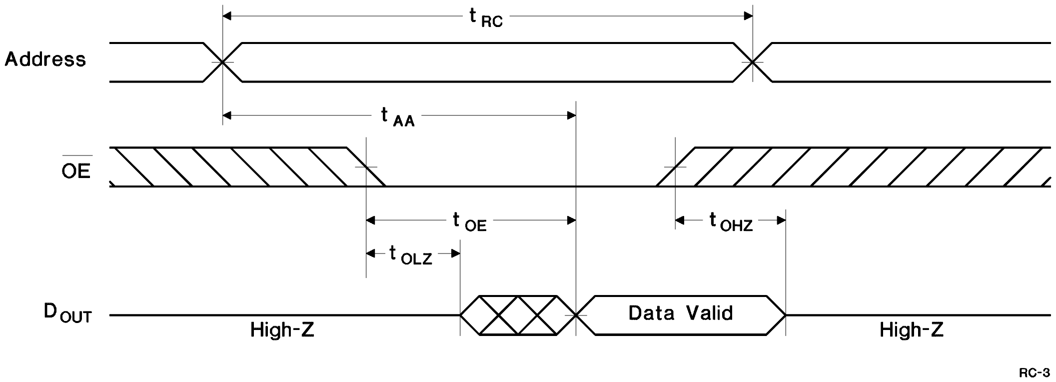
Read Cycle number 1 (Address Access) [1, 2]



Read Cycle number 2 (CS Access) [1, 3, 4]

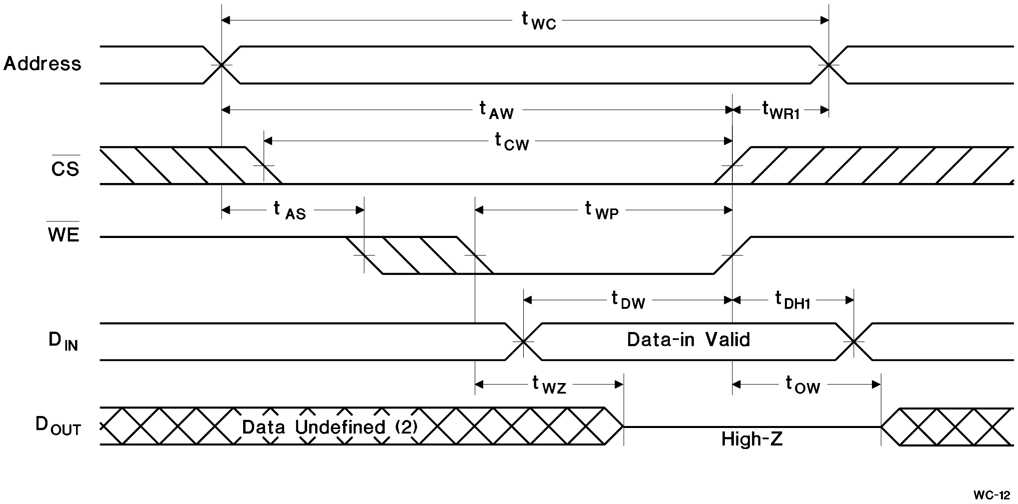


Read Cycle No. 3 (OE Access) [1,5]

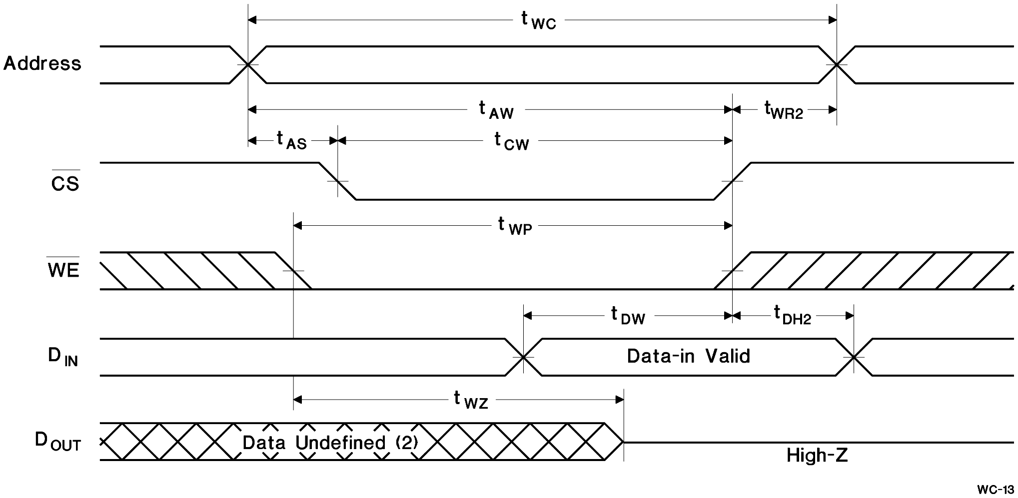


Notes:
1. $\overline{WE}$ is held high for a read cycle.
2. Device is continuously selected: $\overline{CS} = \overline{OE} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Device is continuously selected: $\overline{CS} = V_{IL}$.

Write Cycle No. 1 (WE-Controlled) [1,2,3]



Write Cycle No. 2 (CS-Controlled) [1,2,3,4,5]



Notes:

1. $\overline{\text{CS}}$ or $\overline{\text{WE}}$ must be high during address transition.
2. Because I/O may be active ($\overline{\text{OE}}$ low) during this period, data input signals of opposite polarity to the outputs must not be applied.
3. If $\overline{\text{OE}}$ is high, the I/O pins remain in a state of high impedance.
4. Either t_{WR1} or t_{WR2} must be met.
5. Either t_{DH1} or t_{DH2} must be met.

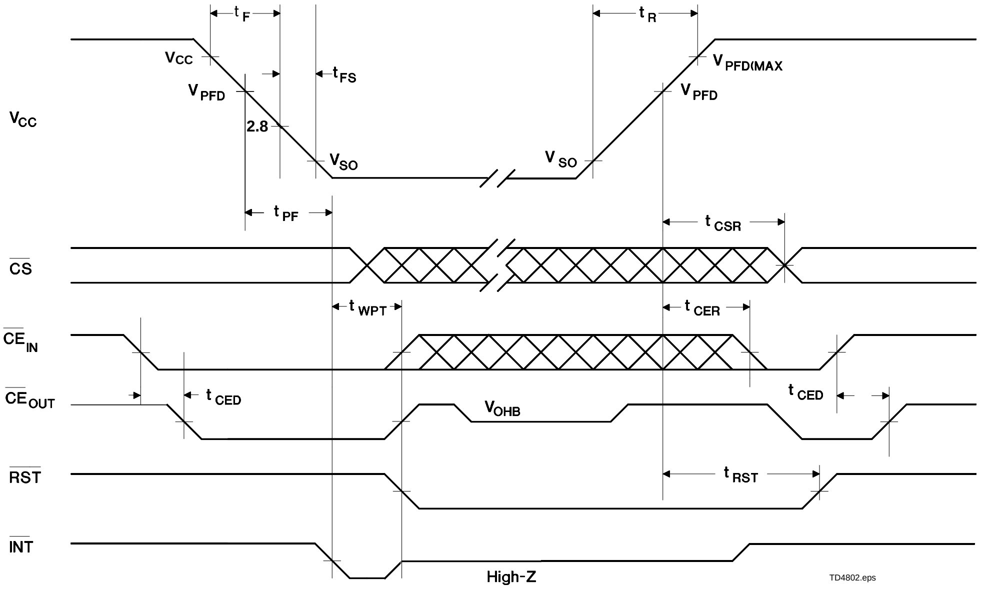
Power-Down/Power-Up Timing ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_F	V_{CC} slew from 3.0 to 0V	300	-	-	µs	
t_{FS}	V_{CC} slew from 0V to 3.0V	10	-	-	µs	
t_R	V_{CC} slew from V_{SO} to $V_{PFD(MAX)}$	100	-	-	µs	
t_{PF}	Interrupt delay from V_{PFD}	6	-	24	µs	bq4802Y
		10	-	40	µs	bq4802LY
t_{WPT}	Write-protect time for external RAM	90	100	125	µs	bq4802Y Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected and $\overline{RST}$ activated.
		150	170	210	µs	bq4802LY Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected and $\overline{RST}$ activated.
t_{CSR}	$\overline{CS}$ at V_{IH} after power-up	100	200	300	ms	bq4802Y Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
		170	330	500	ms	bq4802LY Internal write-protection period after V_{CC} passes V_{PFD} on power-up.
t_{RST}	V_{PFD} to $\overline{RST}$ inactive	t_{CSR}	-	t_{CSR}	ms	Reset active time-out period
t_{CER}	Chip enable recovery time	t_{CSR}	-	t_{CSR}	ms	Time during which external SRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{CED}	Chip enable propagation delay to external SRAM	-	9	15	ns	bq4802Y Output load A
			15	25	ns	bq4802LY Output load A
t_{PBL}	Push-button low time	1	-	-	µs	

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

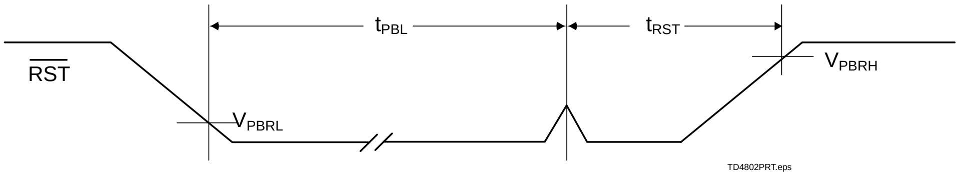
Note: Typical values indicate operation at $T_A = 25°C$.

Power-Down/Power-Up Timing

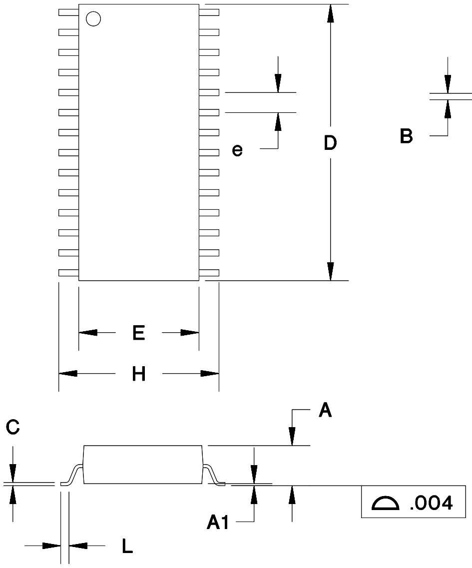


Notes: PWRIE set to “1” to enable power fail interrupt.
$\overline{\text{RST}}$ and $\overline{\text{INT}}$ are open drain and require an external pull-up resistor.

Push-Button Reset Timing



28-Pin SOIC (DW)



28-Pin SOIC (DW)

Dimension	Minimum	Maximum
A	0.095	0.105
A1	0.004	0.012
B	0.013	0.020
C	0.008	0.013
D	0.700	0.715
E	0.290	0.305
e	0.045	0.055
H	0.395	0.415
L	0.020	0.040

All dimensions are in inches.

28-Pin TSSOP (PW)

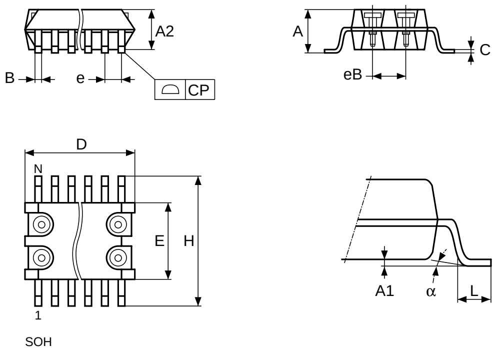
28-Pin TSSOP (PW)

	Inches		Millimeters	
Dimension	Min.	Max.	Min.	Max.
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
B	0.007	0.012	0.18	0.30
C	0.004	0.007	0.09	0.18
D	0.378	0.386	9.60	9.80
E	0.169	0.176	4.30	4.48
e	0.0256BSC		0.65BSC	
H	0.246	0.256	6.25	6.50
L	0.020	0.028	0.50	0.70

Notes:

1. Controlling dimension: millimeters. Inches shown for reference only.
2. 'D' and 'E' do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side
3. Each lead centerline shall be located within ±0.10mm of its exact true position.
4. Leads shall be coplanar within 0.08mm at the seating plane.
5. Dimension 'B' does not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed 'B' maximum by more than 0.08mm.
6. Dimension applies to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
7. 'A1' is defined as the distance from the seating plane to the lowest point of the package body (base plane).

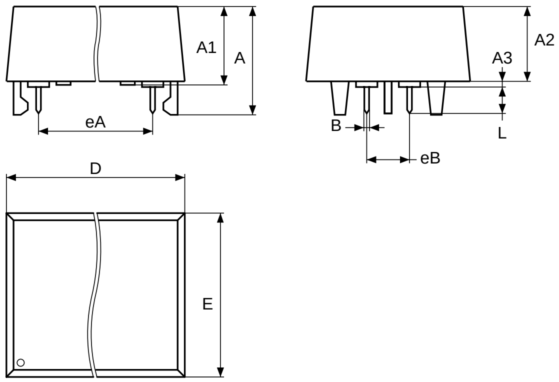
28-Pin SOIC for SNAPHAT Module



28-Pin DSH (SNAPHAT Base)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	-	0.120	-	3.05
A1	0.002	0.014	0.05	0.36
A2	0.092	0.106	2.34	2.69
B	0.014	0.020	0.36	0.51
C	0.006	0.012	0.15	0.32
D	0.697	0.728	17.71	18.49
E	0.324	0.350	8.23	8.89
e	0.050 typ.		1.27 typ.	
eB	0.126	0.142	3.20	3.61
H	0.453	0.500	11.51	12.70
L	0.016	0.050	0.41	1.27
α	0°	8°	0°	8°
N	28		28	
CP	-	0.004	-	0.10

SNAPHAT Housing for SOIC-28 SNAPHAT Module



28-Pin DSH (SNAPHAT Top)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	-	0.385	-	9.78
A1	0.265	0.285	6.73	7.24
A2	0.255	0.275	6.48	6.99
A3	-	0.015	-	0.38
B	0.018	0.022	0.46	0.56
D	0.835	0.860	21.21	21.84
E	0.560	0.590	14.22	14.99
eA	0.612	0.628	15.55	15.95
eB	0.126	0.142	3.20	3.61
L	0.080	0.090	2.03	2.29

Ordering Information

bq4802Y/LY DSH - ___

Temperature Range:
Blank = Commercial

Package Option:
DW = 28-pin SOIC
PW = 28-pin TSSOP
DSH= 28-pin SNAPHAT module SOIC base

Device:
bq4802Y Real-Time Clock with CPU Supervisor or
bq4802LY 3.3V Real-Time Clock with CPU Supervisor

Note: The SNAPHAT housing is ordered seperately under the part number bq48SH-x6 for plastic tube or bq48SH-x6TR in tape and reel form.

Caution: **Do not place the SNAPHAT battery/crystal package bq48SH-x6 in conductive foam, since this will drain the lithium button-cell battery.**

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