

Features

- 64-megabit (4M x 16) and 32-megabit (2M x 16) Flash Memories
- 2.7V - 3.1V Read/Write
- High Performance
 - Asynchronous Access Time – 70 ns
 - Page Mode Read Time – 20 ns
 - Synchronous Burst Frequency – 66 MHz
 - Configurable Burst Operation
- Sector Erase Architecture
 - Eight 4K Word Sectors with Individual Write Lockout
 - 32K Word Main Sectors with Individual Write Lockout
- Typical Sector Erase Time: 32K Word Sectors – 500 ms; 4K Word Sectors – 100 ms
- 32M, Four Plane Organization, Permitting Concurrent Read in Any of the Three Planes not Being Programmed/Erased
 - Memory Plane A: 4M of Memory Including Eight 4K Word Sectors
 - Memory Plane B: 4M of Memory Consisting of 32K Word Sectors
 - Memory Plane C: 12M of Memory Including Eight 32K Word Sectors
 - Memory Plane D: 12M of Memory Including Eight 32K Word Sectors
- 64M, AT49BN6408(T), Four Plane Organization, Permitting Concurrent Read in Any of the Three Planes not Being Programmed/Erased
 - Memory Plane A: 8M of Memory Including Eight 4K Word Sectors
 - Memory Plane B: 24M of Memory Consisting of 32K Word Sectors
 - Memory Plane C: 24M of Memory Consisting of 32K Word Sectors
 - Memory Plane D: 8M of Memory Consisting of 32K Word Sectors
- 64M, AT49BN6416(T), Four Plane Organization, Permitting Concurrent Read in Any of Three Planes not Being Programmed/Erased
 - Memory Plane A: 16M of Memory Including Eight 4K Word Sectors
 - Memory Plane B: 16M of Memory Consisting of 32K Word Sectors
 - Memory Plane C: 16M of Memory Consisting of 32K Word Sectors
 - Memory Plane D: 16M of Memory Consisting of 32K Word Sectors
- Suspend/Resume Feature for Erase and Program
 - Supports Reading and Programming Data from Any Sector by Suspending Erase of a Different Sector
 - Supports Reading Any Word by Suspending Programming of Any Other Word
- Low-power Operation
 - 30 mA Active
 - 10 μ A Standby
- 1.8V I/O Option Reduces Overall System Power
- Data Polling and Toggle Bit for End of Program Detection
- VPP Pin for Write Protection and Accelerated Program/Erase Operations
- RESET Input for Device Initialization
- TSOP or CBGA Package
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register
- Common Flash Interface (CFI)

Description

The AT49BN/BV64xx(T) and AT49BN3204(T) are 2.7-volt 64-megabit and 32-megabit Flash memories respectively. The memories are divided into multiple sectors and planes for erase operations. The devices can be read or reprogrammed off a single 2.7V power supply, making them ideally suited for in-system programming. The output voltage can be separately controlled down to 1.65V through the VCCQ supply pin. The devices can be configured to operate in the asynchronous/page read (default mode) or burst read mode (not available for the AT49BV641(T)). The burst read mode is used to achieve a faster data rate than is possible in the asynchronous/page read mode.



64-megabit (4M x 16) and 32-megabit (2M x 16) Burst/Page Mode 2.7-volt Flash Memory

AT49BV641
AT49BV641T
AT49BN6408
AT49BN6408T
AT49BN6416
AT49BN6416T
AT49BN3204
AT49BN3204T

Advance Information

Continued

Rev. 2481B–FLASH–03/02



Pin Configurations

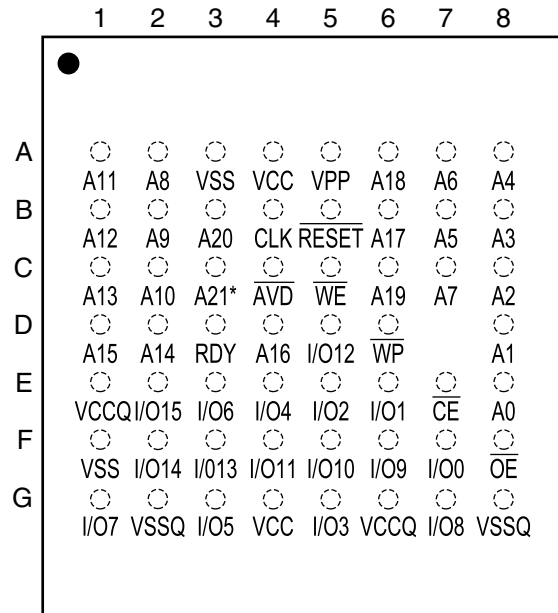
| Pin Name | Pin Function |
|--------------------|--|
| I/O0 - I/O15 | Data Inputs/Outputs |
| A0 - A21 | Addresses ⁽¹⁾ |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| \overline{WE} | Write Enable |
| \overline{AVD} | Address Latch Enable ⁽²⁾ |
| CLK | Clock ⁽²⁾ |
| \overline{RESET} | Reset |
| \overline{WP} | Write Protect |
| VPP | Write Protection and Power Supply for Accelerated Program/Erase Operations |
| RDY | Ready |
| VCCQ | Output Power Supply |

- Notes: 1. For the AT49BN/BV64xx(T), the address bits are A0 - A21, and for the AT49BN3204(T), the address bits are A0 - A20. In the following text, address bits A0 - A21 will be used when referring to both the 64M and 32M devices.
2. These signals are not available for use with the AT49BV641(T). The AT49BV641(T) can only be used in the asynchronous/page mode.

AT49BN64xx(T) or AT49BN3204(T)

CBGA

Top View

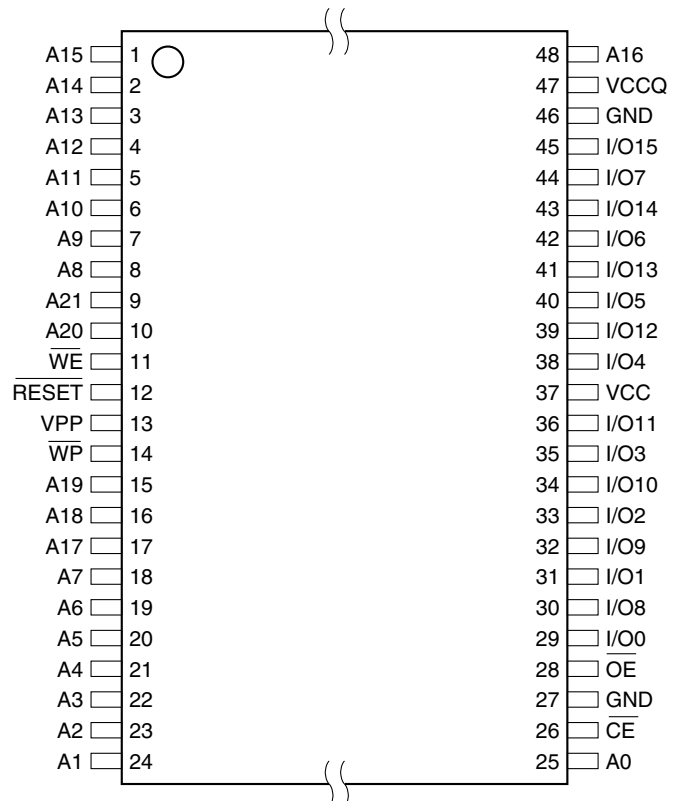


*A21 is a NC for the AT49BN3204(T).

AT49BV641(T)

TSOP Top View

Type 1



If the $\overline{\text{AVD}}$ and the CLK signals are both tied to GND, the device will behave like a standard asynchronous Flash memory. In the page mode, the $\overline{\text{AVD}}$ signal can be tied to GND or can be pulsed low to latch the page address. In both cases the CLK can be tied to GND.

The AT49BN/BV64xx(T) and AT49BN3204(T) are divided into four memory planes. A read operation can occur in any of the three planes which is not being programmed or erased. This concurrent operation allows improved system performance by not requiring the system to wait for a program or erase operation to complete before a read is performed. To further increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors. There is no reason to suspend the erase or program operation if the data to be read is in the other memory plane. The end of program or erase is detected by $\overline{\text{Data}}$ Polling or toggle bit.

The VPP pin provides data protection and faster programming and erase times. When the VPP input is below 0.8V, the program and erase functions are inhibited. When VPP is at 1.65V or above, normal program and erase operations can be performed. With VPP at 12.0V, the program and erase operations are accelerated.

With VPP at 12V, a six-byte command (Enter Single Pulse Program Mode) to remove the requirement of entering the three-byte program sequence is offered to further improve programming time. After entering the six-byte code, only single pulses on the write control lines are required for writing into the device. This mode (Single Pulse Word Program) is exited by powering down the device, by taking the $\overline{\text{RESET}}$ pin to GND or by a high-to-low transition on the VPP input. Erase, Erase Suspend/Resume, Program Suspend/Resume and Read Reset commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six-byte code reside in the software of the final product but only exist in external programming code.

Device Operation

COMMAND SEQUENCES: The device powers on in the read mode. Command sequences are used to place the device in other operating modes such as program and erase. After the completion of a program or an erase cycle, the device enters the read mode. The command sequences are written by applying a low pulse on the $\overline{\text{WE}}$ input with $\overline{\text{CE}}$ low and $\overline{\text{OE}}$ high or by applying a low-going pulse on the $\overline{\text{CE}}$ input with $\overline{\text{WE}}$ low and $\overline{\text{OE}}$ high. Prior to the low-going pulse on the $\overline{\text{CE}}$ or $\overline{\text{WE}}$ signal, the address input may be latched by a low-to-high transition on the $\overline{\text{AVD}}$ signal or the rising edge of the first clock pulse when $\overline{\text{AVD}}$ is low, whichever occurs first. If the $\overline{\text{AVD}}$ is not pulsed low, the address will be latched on the falling edge of the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse whichever occurs first. Valid data is latched on the rising edge of the $\overline{\text{WE}}$ or the $\overline{\text{CE}}$ pulse, whichever occurs first. The addresses used in the command sequences are not affected by entering the command sequences.

BURST CONFIGURATION COMMAND: The Program Burst Configuration Register command is used to program the burst configuration register. The burst configuration register determines several parameters that control the read operation of the device. Bit B15 determines whether synchronous burst reads are enabled or asynchronous reads are enabled. Since the page read operation is an asynchronous operation, bit B15 must be set for asynchronous reads to enable the page read feature. Bit B14 determines whether a four word page or an eight word page will be used. The rest of the bits in the burst configuration register are used only for the burst read mode. Bits B13 - B11 of the

burst configuration register determine the clock latency for the burst mode. The latency can be set to two, three, four, five or six cycles. The clock latency versus input clock frequency table is shown on page 16. The “Burst Read Waveform” as shown on page 29 illustrates a clock latency of four; the data is output from the device four clock cycles after the first low-to-high clock edge following the high-to-low $\overline{\text{AVD}}$ edge. The B10 bit of the configuration register determines the polarity of the RDY signal. The B9 bit of the burst configuration register determines the number of clocks that data will be held valid (see Figure 1). The B8 bit of the burst configuration register determines when the RDY signal will be asserted. When synchronous burst reads are enabled, an interleaved or linear burst sequence can be selected by setting bit B7. Table 4 shows the difference between the interleaved and burst sequence. Bit B6 selects whether the burst starts and the data output will be relative to the falling edge or the rising edge of the clock. Bits B2 - B0 of the burst configuration register determine whether a continuous or fixed-length burst will be used and also determine whether a four- or eight-word length will be used in the fixed-length mode. When a four or eight word burst length is selected, Bit B3 can be used to select whether burst accesses wrap within the burst length boundary or whether they cross word length boundaries to perform linear accesses. Please see Table 4. All other bits in the burst configuration register should be programmed as shown on page 16. The default state (after power-up or reset) of the burst configuration register is also shown on page 16. To read the burst configuration register, the Product ID Entry command is given, followed by a normal read operation from address location 00005H. After reading the burst configuration register, the Product ID Exit command must be given prior to performing any other operation.

ASYNCHRONOUS READ: There are two types of asynchronous reads – $\overline{\text{AVD}}$ pulsed and standard asynchronous reads. The $\overline{\text{AVD}}$ pulsed read operation of the device is controlled by $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{AVD}}$ inputs. The outputs are put in the high-impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention. The data at the address location defined by A0 - A21 and captured by the $\overline{\text{AVD}}$ signal will be read when $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low. The address location passes into the device when $\overline{\text{CE}}$ and $\overline{\text{AVD}}$ are low; the address is latched on the low-to-high transition of $\overline{\text{AVD}}$. Low input levels on the $\overline{\text{OE}}$ and $\overline{\text{CE}}$ pins allow the data to be driven out of the device. The access time is measured from stable address, falling edge of $\overline{\text{AVD}}$ or falling edge of $\overline{\text{CE}}$, whichever occurs last. During the $\overline{\text{AVD}}$ pulsed read, the CLK signal may be static high or static low. For standard asynchronous reads, the $\overline{\text{AVD}}$ and CLK signal should be tied to GND. The asynchronous read diagrams are shown on page 26.

PAGE READ: The page read operation of the device is controlled by $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{AVD}}$ inputs. The CLK input is ignored during a page read operation and should be tied to GND. The page size can be four words (default value) or eight words depending on what value bit B14 of the burst configuration register is programmed to. During a page read, the $\overline{\text{AVD}}$ signal can transition low and then transition high, transition low and remain low, or can be tied to GND. If a high to low transition on the $\overline{\text{AVD}}$ signal occurs, as shown in Page Read Cycle Waveform 1, the page address is latched by the low-to-high transition of the $\overline{\text{AVD}}$ signal. However, if the $\overline{\text{AVD}}$ signal remains low after the high-to-low transition or if the $\overline{\text{AVD}}$ signal is tied to GND, as shown in Page Read Cycle Waveform 2, then the page address (determined by A21 - A3 for an eight word page and A21 - A2 for a four word page) cannot change during a page read operation. The first word access of the page read is the same as the asynchronous read. The first word is read at an asynchronous speed of 80 ns. Once the first word is read, toggling A0 and A1 (four word page mode) or toggling A0, A1, and A2 (eight word page mode) will result in subsequent reads within the page being output at a speed of 20 ns. If the $\overline{\text{AVD}}$ and the CLK pins are both tied to GND, the device will behave like a standard asynchronous Flash memory. The page read diagrams are shown on page 27.

SYNCHRONOUS READS: Synchronous reads (not available on the AT49BV641(T)) are used to achieve a faster data rate that is possible in the asynchronous/page read mode. The device can be configured for continuous or fixed-length burst access. The burst read operation of the device is controlled by \overline{CE} , \overline{OE} , CLK and \overline{AVD} inputs. The initial read location is determined as for the \overline{AVD} pulsed asynchronous read operation; it can be any memory location in the device. In the burst access, the address is latched on the rising edge of the first clock pulse when \overline{AVD} is low or the rising edge of the \overline{AVD} signal, whichever occurs first. The CLK input signal controls the flow of data from the device for a burst operation. After the clock latency cycles, the data at the next burst address location is read for each following clock cycle.

CONTINUOUS BURST READ: During a continuous burst read, any number of addresses can be read from the memory. When a page boundary in the memory is transitioned, additional time may be required for the device to continue the burst read. To indicate that it is not ready to continue the burst, the device will drive the RDY pin low ($B10 = 0$) during the clock cycles in which new data is not being presented. Once the RDY pin is driven high ($B10 = 0$), the next data will be valid. Starting with address zero, page boundaries occur every 128 words in the memory. During a continuous burst read, the first page boundary transition may occur before 128 words are read, depending on the initial burst address. The RDY signal will be tri-stated when the \overline{CE} or \overline{OE} signal is high.

In the “Burst Read Waveform” as shown on page 29, data D0 is valid asynchronously from point A, the time when the addresses are latched. D0 is valid within 13.0 ns of the clock edge for the specified clock latency (the waveforms show a clock latency of four). The low-to-high transition of the clock at point C results in D1 being read. The transition of the clock at point D results in a burst read of the last word of the page, D127. The clock transition at point E does not cause new data to appear on the output lines because the RDY signal goes low ($B10$ and $B8 = 0$) after the clock transition, which signifies that a page boundary in the memory has been crossed and that new data is not available. The clock transition at point F does cause a burst read of data D128 because the RDY signal goes high ($B10$ and $B8 = 0$) after the clock transition indicating that new data is available. Additional clock transitions, like at point G, will continue to result in burst reads until the next page boundary is crossed between words D255 and D256.

FIXED-LENGTH BURST READS: During a fixed-length burst mode read, four or eight words of data may be burst from the device, depending upon the configuration. The device supports a linear or interleaved burst mode. The burst sequence is shown on page 17. The RDY output remains high ($B10 = 0$) during fixed-length bursts. The “Four-word Burst Read Waveform” on page 29 illustrates a fixed-length burst cycle. As in the continuous burst read, the data D0 is valid asynchronously from point A, the time when the addresses are latched. D0 is valid within 13.0 ns of the clock edge for the specified clock latency (shown for the case of a latency of four). The low-to-high transition of the clock at point C results in D1 being read. Similarly, D2 and D3 are output following the next two clock cycles. Returning \overline{CE} high ends the read cycle.

RESET: A \overline{RESET} input pin is provided to ease some system applications. When \overline{RESET} is at a logic high level, the device is in its standard operating mode. A low level on the \overline{RESET} pin halts the present device operation and puts the outputs of the device in a high-impedance state. When a high level is reasserted on the \overline{RESET} pin, the device returns to read or standby mode, depending upon the state of the control pins.

ERASE: Before a word can be reprogrammed it must be erased. The erased state of the memory bits is a logical “1”. The entire memory can be erased by using the Chip Erase command or individual planes or sectors can be erased by using the Plane Erase or Sector Erase commands.

CHIP ERASE: Chip Erase is a six-bus cycle operation. The automatic erase begins on the rising edge of the last \overline{WE} pulse. Chip Erase does not alter the data of the protected sectors. After the full chip erase the device will return back to the read mode. The hardware reset during Chip Erase will stop the erase but the data will be of unknown state. Any command during Chip Erase except Erase Suspend will be ignored.

PLANE ERASE: As an alternative to a full chip erase, the device is organized into four planes that can be individually erased. The plane erase command is a six-bus cycle operation. The plane whose address is valid at the sixth falling edge of \overline{WE} will be erased provided none of the sectors within the plane are protected.

SECTOR ERASE: As an alternative to a full chip erase or a plane erase, the device is organized into multiple sectors that can be individually erased. The Sector Erase command is a six-bus cycle operation. The sector whose address is valid at the sixth falling edge of \overline{WE} will be erased provided the given sector has not been protected.

WORD PROGRAMMING: The device is programmed on a word-by-word basis. Programming is accomplished via the internal device command register and is a four-bus cycle operation. The programming address and data are latched in the fourth cycle. The device will automatically generate the required internal programming pulses. Please note that a “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s.

FLEXIBLE SECTOR PROTECTION: The AT49BN/BV64xx(T)/3204(T) offers two sector protection modes, the Softlock and the Hardlock. The Softlock mode is optimized as sector protection for sectors whose content changes frequently. The Hardlock protection mode is recommended for sectors whose content changes infrequently. Once either of these two modes is enabled, the contents of the selected sector is read-only and cannot be erased or programmed. Each sector can be independently programmed for either the Softlock or Hardlock sector protection mode. At power-up and reset, all sectors have their Softlock protection mode enabled.

SOFTLOCK AND UNLOCK: The Softlock protection mode can be disabled by issuing a two-bus cycle Unlock command to the selected sector. Once a sector is unlocked, its contents can be erased or programmed. To enable the Softlock protection mode, a six-bus cycle Softlock command must be issued to the selected sector.

HARDLOCK AND WRITE PROTECT (\overline{WP}): The Hardlock sector protection mode operates in conjunction with the Write Protection (\overline{WP}) pin. The Hardlock sector protection mode can be enabled by issuing a six-bus cycle Hardlock software command to the selected sector. The state of the Write Protect pin affects whether the Hardlock protection mode can be overridden.

- When the \overline{WP} pin is low and the Hardlock protection mode is enabled, the sector cannot be unlocked and the contents of the sector is read-only.
- When the \overline{WP} pin is high, the Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.

To disable the Hardlock sector protection mode, the chip must be either reset or power cycled.

Table 1. Hardlock and Softlock Protection Configurations in Conjunction with \overline{WP}

| V_{PP} | \overline{WP} | Hard lock | Soft lock | Erase/ Prog Allowed? | Comments |
|-------------|-----------------|-----------|-----------|----------------------|---|
| $V_{CC}/5V$ | 0 | 0 | 0 | Yes | No sector is locked |
| $V_{CC}/5V$ | 0 | 0 | 1 | No | Sector is Softlocked. The Unlock command can unlock the sector. |
| $V_{CC}/5V$ | 0 | 1 | 1 | No | Hardlock protection mode is enabled. The sector cannot be unlocked. |
| $V_{CC}/5V$ | 1 | 0 | 0 | Yes | No sector is locked. |
| $V_{CC}/5V$ | 1 | 0 | 1 | No | Sector is Softlocked. The Unlock command can unlock the sector. |
| $V_{CC}/5V$ | 1 | 1 | 0 | Yes | Hardlock protection mode is overridden and the sector is not locked. |
| $V_{CC}/5V$ | 1 | 1 | 1 | No | Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command. |
| V_{IL} | x | x | x | No | Erase and Program Operations cannot be performed. |

SECTOR PROTECTION DETECTION: A software method is available to determine if the sector protection Softlock or Hardlock features are enabled. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from the I/O0 and I/O1 at address location 00002H within a sector will show if the sector is unlocked, softlocked, or hardlocked.

Table 2. Sector Protection Status

| I/O1 | I/O0 | Sector Protection Status |
|------|------|------------------------------------|
| 0 | 0 | Sector Not Locked |
| 0 | 1 | Softlock Enabled |
| 1 | 0 | Hardlock Enabled |
| 1 | 1 | Both Hardlock and Softlock Enabled |

PROGRAM/ERASE STATUS: The device provides several bits to determine the status of a program or erase operation: I/O2, I/O3, I/O5, I/O6, and I/O7. The Table 3 on page 13 and the following four sections describe the function of these bits. To provide greater flexibility for system designers, the AT49BN/BV64xx(T)/3204(T) contains a programmable configuration register. The configuration register allows the user to specify the status bit operation. The configuration register can be set to one of two different values, “00” or “01”. If the configuration register is set to “00”, the part will automatically return to the read mode after a successful program or erase operation. If the configuration register is set to a “01”, a Product ID Exit command must be given after a successful program or erase operation before the part will return to the read mode. It is important to note that whether the configuration register is set to a “00” or to a “01”, any unsuccessful program

or erase operation requires using the Product ID Exit command to return the device to read mode. The default value (after power-up) for the configuration register is “00”. Using the four-bus cycle set configuration register command as shown in the Command Definition table on page 14, the value of the configuration register can be changed. Voltages applied to the reset pin will not alter the value of the configuration register. The value of the configuration register will affect the operation of the I/O7 status bit as described below.

DATA POLLING: The AT49BN/BV64xx(T)/3204(T) features $\overline{\text{Data}}$ Polling to indicate the end of a program cycle. If the status configuration register is set to a “00”, during a program cycle an attempted read of the last byte/word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a “0” on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{Data}}$ Polling may begin at any time during the program cycle. Please see Table 3 on page 13 for more details.

If the status bit configuration register is set to a “01”, the I/O7 status bit will be low while the device is actively programming or erasing data. I/O7 will go high when the device has completed a program or erase operation. Once I/O7 has gone high, status information on the other pins can be checked.

The $\overline{\text{Data}}$ Polling status bit must be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 2 and 3.

TOGGLE BIT: In addition to $\overline{\text{Data}}$ Polling, the AT49BN/BV64xx(T)/3204(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the memory will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle. Please see Table 3 on page 13 for more details.

The toggle bit status bit should be used in conjunction with the erase/program and V_{PP} status bit as shown in the algorithm in Figures 4 and 5 on page 12.

ERASE/PROGRAM STATUS BIT: The device offers a status bit on I/O5 that indicates whether the program or erase operation has exceeded a specified internal pulse count limit. If the status bit is a “1”, the device is unable to verify that an erase or a byte/word program operation has been successfully performed. The device may also output a “1” on I/O5 if the system tries to program a “1” to a location that was previously programmed to a “0”. Only an erase operation can change a “0” back to a “1”. If a program (Sector Erase) command is issued to a protected sector, the protected sector will not be programmed (erased). The device will go to a status read mode and the I/O5 status bit will be set high, indicating the program (erase) operation did not complete as requested. Once the erase/program status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. The erase/program status bit is a “0” while the erase or program operation is still in progress. Please see Table 3 on page 13 for more details.

V_{PP} STATUS BIT: The AT49BN/BV64xx(T)/3204(T) provides a status bit on I/O3 that provides information regarding the voltage level of the VPP pin. During a program or erase operation, if the voltage on the VPP pin is not high enough to perform the desired operation successfully, the I/O3 status bit will be a “1”. Once the V_{PP} status bit has been set to a “1”, the system must write the Product ID Exit command to return to the read mode. On the other hand, if the voltage level is high enough to perform a program or erase operation successfully, the V_{PP} status bit will output a “0”. Please see Table 3 on page 13 for more details.

ERASE SUSPEND/ERASE RESUME: The Erase Suspend command allows the system to interrupt a sector erase operation and then program or read data from a different sector within the same plane. Since this device has a dual plane architecture, there is no need to use the erase suspend feature while erasing a sector when you want to read data from a sector in the other plane. After the Erase Suspend command is given, the device requires a maximum time of 15 μ s to suspend the erase operation. After the erase operation has been suspended, the plane that contains the suspended sector enters the erase-suspend-read mode. The system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command, which does require the plane address. The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

PROGRAM SUSPEND/PROGRAM RESUME: The Program Suspend command allows the system to interrupt a programming operation and then read data from a different word within the memory. After the Program Suspend command is given, the device requires a maximum of 10 μ s to suspend the programming operation. After the programming operation has been suspended, the system can then read from any other word within the device. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same, and the command sequence for the erase resume and program resume are the same.

128-BIT PROTECTION REGISTER: The AT49BN/BV64xx(T)/3204(T) contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit blocks. The two blocks are designated as block A and block B. The data in block A is non-changeable and is programmed at the factory with a unique number. The data in block B is programmed by the user and can be locked out such that data in the block cannot be reprogrammed. To program block B in the protection register, the four-bus cycle Program Protection Register command must be used as shown in the Command Definition in Hex table on page 14. To lock out block B, the four-bus cycle lock protection register command must be used as shown in the Command Definition in Hex table. Data bit D1 must be zero during the fourth bus cycle. All other data bits during the fourth bus cycle are don't cares. To determine whether block B is locked out, the Product ID Entry command is given followed by a read operation from address 80H. If data bit D1 is zero, block B is locked. If data bit D1 is one, block B can be reprogrammed. Please see the Protection Register Addressing Table on page 15 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether block B is protected or not or reading the protection register, the Product ID Exit command must be given prior to performing any other operation.

CFI: Common Flash Interface (CFI) is a published, standardized data structure that may be read from a flash device. CFI allows system software to query the installed device to determine the configurations, various electrical and timing parameters, and functions supported by the device. CFI is used to allow the system to learn how to interface to the flash device most optimally. The two primary benefits of using CFI are ease of upgrading and second source availability. The command to enter the CFI Query mode is a one-bus cycle command which requires writing data 98h to address 55h. The

CFI Query command can be written when the device is ready to read data or can also be written when the part is in the product ID mode. Once in the CFI Query mode, the system can read CFI data at the addresses given in Table 5 on page 35. To exit the CFI Query mode, the product ID exit command must be given. If the CFI Query command is given while the part is in the product ID mode, then the product ID exit command must first be given to return the part to the product ID mode. Once in the product ID mode, it will be necessary to give another product ID exit command to return the part to the read mode.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49BN/BV64xx(T)/3204(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time-out 10 ms (typical) before programming. (c) Program inhibit: holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the \overline{WE} or \overline{CE} inputs will not initiate a program cycle. (e) V_{PP} is less than V_{ILPP} .

INPUT LEVELS: While operating with a 2.7V to 3.1V power supply, the address inputs and control inputs (\overline{OE} , \overline{CE} and \overline{WE}) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can be driven from 0 to $V_{CCQ} + 0.6V$.

OUTPUT LEVELS: For the AT49BN/BV64xx(T)/3204(T), output high levels are equal to $V_{CCQ} - 0.1V$ (not V_{CC}). For 2.7V to 3.1V output levels, V_{CCQ} must be tied to V_{CC} .

Figure 1. Output Configuration

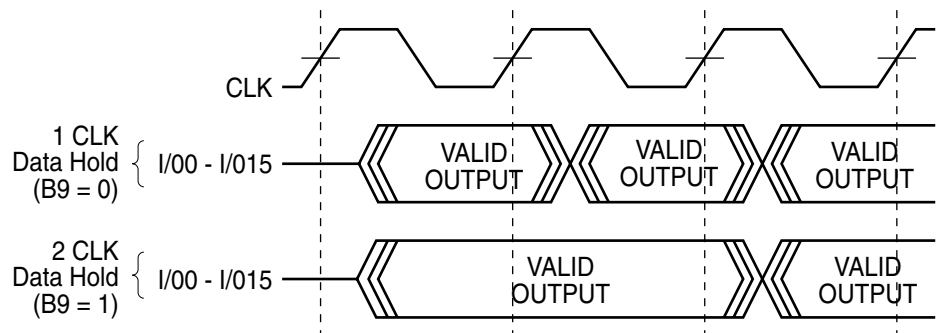


Figure 2. Data Polling Algorithm
(Configuration Register = 00)

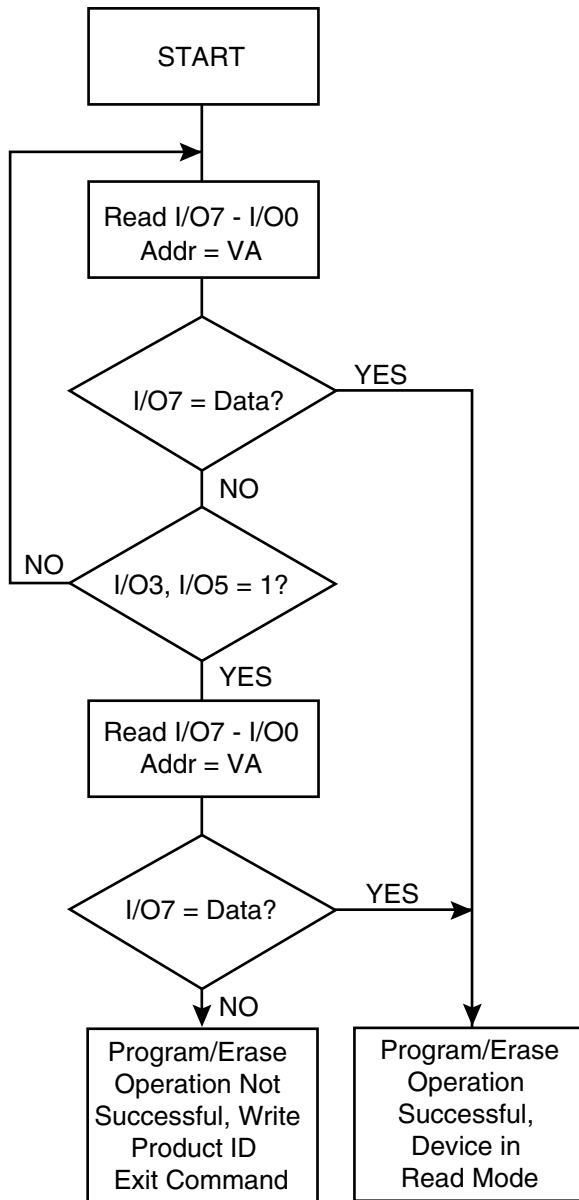
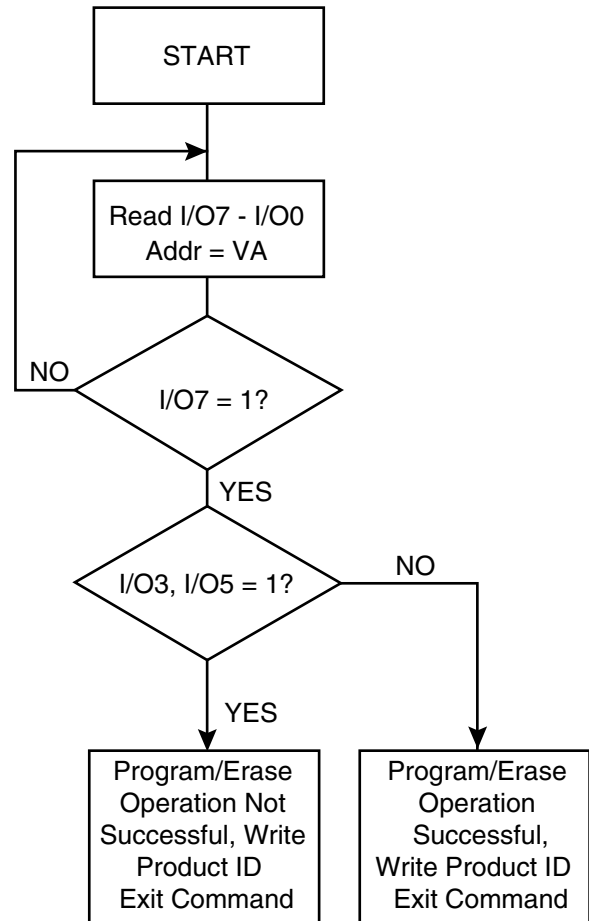


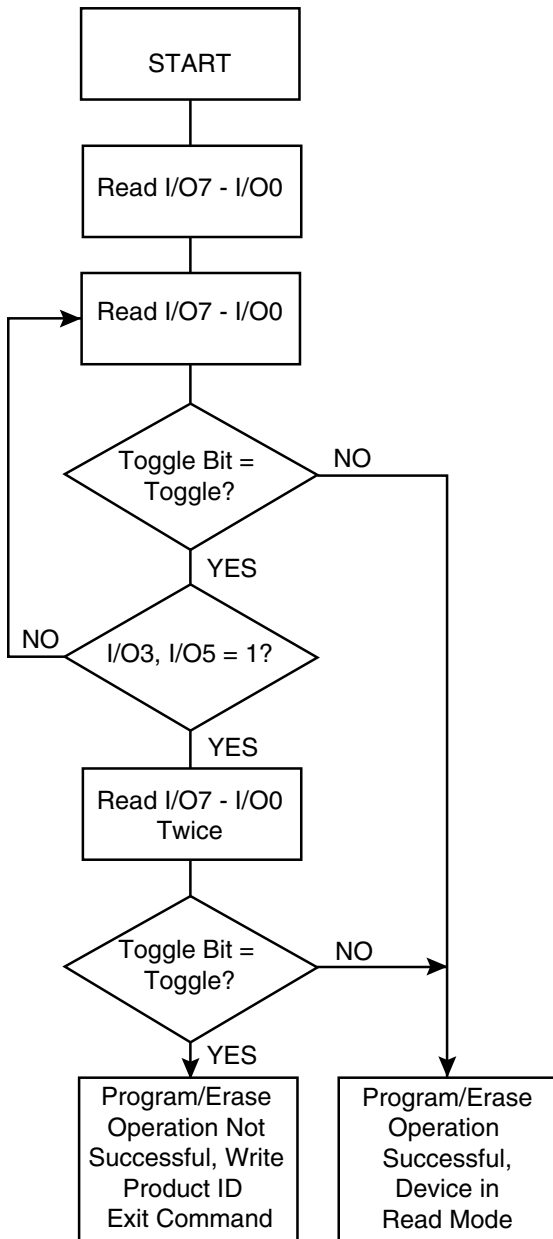
Figure 3. Data Polling Algorithm
(Configuration Register = 01)



Note: 1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

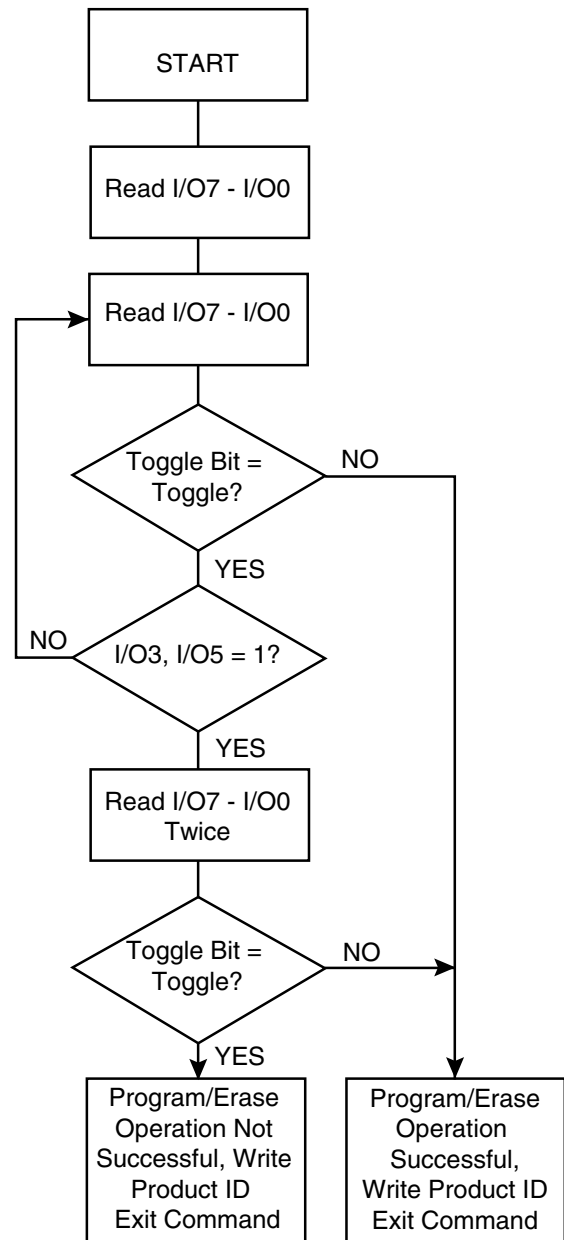
- Notes:
1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
 2. I/O7 should be rechecked even if I/O5 = "1" because I/O7 may change simultaneously with I/O5.

Figure 4. Toggle Bit Algorithm
(Configuration Register = 00)



Note: 1. The system should recheck the toggle bit even if I/O5 = "1" because the toggle bit may stop toggling as I/O5 changes to "1".

Figure 5. Toggle Bit Algorithm
(Configuration Register = 01)



Note: 1. The system should recheck the toggle bit even if I/O5 = "1" because the toggle bit may stop toggling as I/O5 changes to "1".

Table 3. Status Bit Table

| | I/O7 | | | | I/O6 | | | | I/O2 | | | |
|---|---------------------|---------------------|---------------------|---------------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Configuration Register: | 00/01 | 00/01 | 00/01 | 00/01 | 00/01 | 00/01 | 00/01 | 00/01 | 00/01 | 00/01 | 00/01 | 00/01 |
| Read Address In | Plane A | Plane B | Plane C | Plane D | Plane A | Plane B | Plane C | Plane D | Plane A | Plane B | Plane C | Plane D |
| While | | | | | | | | | | | | |
| | | | | | | | | | | | | |
| Programming in Plane A | $\overline{I/O7}/0$ | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | 1 | DATA | DATA | DATA |
| Programming in Plane B | DATA | $\overline{I/O7}/0$ | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | 1 | DATA | DATA |
| Programming in Plane C | DATA | DATA | $\overline{I/O7}/0$ | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | 1 | DATA |
| Programming in Plane D | DATA | DATA | DATA | $\overline{I/O7}/0$ | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | 1 |
| Erasing in Plane A | 0/0 | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA |
| Erasing in Plane B | DATA | 0/0 | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | TOGGLE | DATA | DATA |
| Erasing in Plane C | DATA | DATA | 0/0 | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | TOGGLE | DATA |
| Erasing in Plane D | DATA | DATA | DATA | 0/0 | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | TOGGLE |
| Erase Suspended & Read Erasing Sector | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | TOGGLE | TOGGLE | TOGGLE | TOGGLE |
| Erase Suspended & Read Non-erasing Sector | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA | DATA |
| Erase Suspended & Program Non-erasing Sector in Plane A | $\overline{I/O7}/0$ | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA |
| Erase Suspended & Program Non-erasing Sector in Plane B | DATA | $\overline{I/O7}/0$ | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | TOGGLE | DATA | DATA |
| Erase Suspended & Program Non-erasing Sector in Plane C | DATA | DATA | $\overline{I/O7}/0$ | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | TOGGLE | DATA |
| Erase Suspended & Program Non-erasing Sector in Plane D | DATA | DATA | DATA | $\overline{I/O7}/0$ | DATA | DATA | DATA | TOGGLE | DATA | DATA | DATA | TOGGLE |

Command Definition in (Hex)⁽¹⁾

| Command Sequence | Bus Cycles | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | | 4th Bus Cycle | | 5th Bus Cycle | | 6th Bus Cycle | |
|---------------------------------------|------------|-------------------|------------------|--------------------|------|--------------------|------|---------------|---------------------------------|---------------|------|----------------------|------|
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read | 1 | Addr | D _{OUT} | | | | | | | | | | |
| Chip Erase | 6 | 555 | AA | AAA ⁽²⁾ | 55 | 555 | 80 | 555 | AA | AAA | 55 | 555 | 10 |
| Plane Erase | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | PA ⁽⁶⁾ | 20 |
| Sector Erase | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | SA ⁽⁴⁾ | 30 |
| Word Program | 4 | 555 | AA | AAA | 55 | 555 | A0 | Addr | D _{IN} | | | | |
| Enter Single-pulse Program Mode | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | 555 | A0 |
| Single-pulse Word Program Mode | 1 | Addr | D _{IN} | | | | | | | | | | |
| Sector Softlock | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | SA ⁽⁴⁾ | 40 |
| Sector Unlock | 2 | 555 | AA | SA ⁽⁴⁾ | 70 | | | | | | | | |
| Sector Hardlock | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | SA ⁽⁴⁾⁽⁵⁾ | 60 |
| Erase/Program Suspend | 1 | xxx | B0 | | | | | | | | | | |
| Erase/Program Resume | 1 | PA ⁽⁶⁾ | 30 | | | | | | | | | | |
| Product ID Entry | 3 | 555 | AA | AAA | 55 | xxx ⁽⁷⁾ | 90 | | | | | | |
| Product ID Exit ⁽³⁾ | 3 | 555 | AA | AAA | 55 | 555 | F0 | | | | | | |
| Product ID Exit ⁽³⁾ | 1 | xxx | FX | | | | | | | | | | |
| Program Burst Configuration Register | 4 | 555 | AA | AAA | 55 | 555 | D0 | xxx | ⁽⁸⁾ | | | | |
| Read Burst Configuration Register | 4 | 555 | AA | AAA | 55 | xxx ⁽⁷⁾ | 90 | 005 | D _{OUT} | | | | |
| Program Protection Register – Block B | 4 | 555 | AA | AAA | 55 | 555 | C0 | Addr | D _{IN} | | | | |
| Lock Protection Register – Block B | 4 | 555 | AA | AAA | 55 | 555 | C0 | 080 | X0 | | | | |
| Status of Block B Protection | 4 | 555 | AA | AAA | 55 | 555 | 90 | 80 | D _{OUT} ⁽⁹⁾ | | | | |
| Set Configuration Register | 4 | 555 | AA | AAA | 55 | 555 | E0 | xxx | 00/01 ⁽¹⁰⁾ | | | | |
| CFI Query | 1 | X55 | 98 | | | | | | | | | | |

- Notes:
- The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex). The ADDRESS FORMAT in each bus cycle is as follows: A11 - A0 (Hex), A11 - A21 (Don't Care).
 - Since A11 is a Don't Care, AAA can be replaced with 2AA.
 - Either one of the Product ID Exit commands can be used.
 - SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 18 - 23 for details).
 - Once a sector is in the Hardlock protection mode, it cannot be disabled unless the chip is reset or power cycled.
 - PA is the plane address (A21 - A19 for the AT49BN6408(T), A21 - A20 for the AT49BN6416(T)/BV641(T), A20 - A18 for the AT49BN3204(T)).
 - For the AT49BN3204T:
 xxx = 00X555 Status Read from Plane A
 xxx = 05X555 Status Read from Plane B
 xxx = 11X555 Status Read from Plane C
 xxx = 1FX555 Status Read from Plane D
 For the AT49BN6408T:
 xxx = 0XX555 Status Read from Plane A
 xxx = 1XX555 Status Read from Plane B
 xxx = 2XX555 Status Read from Plane C
 xxx = 38X555 Status Read from Plane D
 For the AT49BN6416(T)/BV641T:
 xxx = 0XX555 Status Read from Plane A
 xxx = 1XX555 Status Read from Plane B
 xxx = 2XX555 Status Read from Plane C
 xxx = 3XX555 Status Read from Plane D
 For the AT49BN6408T:
 xxx = 38X555 Status Read from Plane A
 xxx = 2XX555 Status Read from Plane B
 xxx = 1XX555 Status Read from Plane C
 xxx = 00X555 Status Read from Plane D
 For the AT49BN6416(T)/BV641T:
 xxx = 3XX555 Status Read from Plane A
 xxx = 2XX555 Status Read from Plane B
 xxx = 1XX555 Status Read from Plane C
 xxx = 0XX555 Status Read from Plane D
 - See "Burst Configuration Register" on page 16.
 - If data bit D1 is "0", block B is locked. If data bit D1 is "1", block B can be reprogrammed.
 - The default state (after power-up) of the configuration register is "00".

Absolute Maximum Ratings*

| | |
|---|---------------------------|
| Temperature under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| All Input Voltages Except V_{PP} (including NC Pins) with Respect to Ground | -0.6V to +6.25V |
| V_{PP} Input Voltage with Respect to Ground | 0V to 13.0V |
| All Output Voltages with Respect to Ground | -0.6V to $V_{CCQ} + 0.6V$ |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Protection Register Addressing Table

| Word | Use | Block | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|------|---------|-------|----|----|----|----|----|----|----|----|
| 0 | Factory | A | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | Factory | A | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 2 | Factory | A | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 3 | Factory | A | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 4 | User | B | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 5 | User | B | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 6 | User | B | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 7 | User | B | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Note: 1. All address lines not specified in the above table must be 0 when accessing the Protection Register, i.e., A21 - A8 = 0.

Burst Configuration Register

| | | |
|------------|--|--|
| B15 | 0 1 ⁽¹⁾ | Synchronous Burst Reads Enabled Asynchronous/Page Reads Enabled |
| B14 | 0 ⁽¹⁾ 1 | Four Word Page Eight Word Page |
| B13 - B11: | 010 011 100 101 110 ⁽¹⁾ | Clock Latency of Two Clock Latency of Three Clock Latency of Four Clock Latency of Five Clock Latency of Six |
| B10 | 0 1 ⁽¹⁾ | RDY Signal is Active Low RDY Signal is Active High |
| B9 | 0 1 ⁽¹⁾ | Hold Data for One Clock Hold Data for Two Clocks |
| B8 | 0 1 ⁽¹⁾ | RDY Asserted during Clock Cycle in which Data is Valid RDY Asserted One Clock Cycle before Data is Valid |
| B7 | 0 1 ⁽¹⁾ | Interleaved Burst Sequence Linear Burst Sequence |
| B6 | 0 1 ⁽¹⁾ | Burst Starts and Data Output on Falling Clock Edge Burst Starts and Data Output on Rising Clock Edge |
| B5 - B4 | 00 ⁽¹⁾ | Reserved for Future Use |
| B3 | 0 1 ⁽¹⁾ | Wrap Burst Within Burst length set by B2 - B0 Don't Wrap Accesses Within Burst Length set by B2 - B0 |
| B2 - B0 | 001 010 111 ⁽¹⁾ | Four-word Burst Eight-word Burst Continuous Burst |

Note: 1. Default State

Clock Latency versus Input Clock Frequency

| Minimum Clock Latency (Minimum Number of Clocks Following Address Latch) | Input Clock Frequency |
|---|-----------------------|
| 6 | ≤ 54 MHz |
| 4 | ≤ 40 MHz |
| 2 | ≤ 20 MHz |

Table 4. Sequence and Burst Length

| Start Addr. (Decimal) | Wrap B3 = 0 | Wrap B3 = 1 | Burst Addressing Sequence (Decimal) | | | | |
|--------------------------|----------------|----------------|--------------------------------------|-------------|--------------------------------------|-----------------|-----------------------------------|
| | | | 4-word Burst Length B2 – B0 = 001 | | 8-word Burst Length B2 – B0 = 010 | | Continuous Burst B2 – B0 = 111 |
| | | | Linear | Interleaved | Linear | Interleaved | Linear |
| 0 | 0 | | 0-1-2-3 | 0-1-2-3 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6... |
| 1 | 0 | | 1-2-3-0 | 1-0-3-2 | 1-2-3-4-5-6-7-0 | 1-0-3-2-5-4-7-6 | 1-2-3-4-5-6-7... |
| 2 | 0 | | 2-3-0-1 | 2-3-0-1 | 2-3-4-5-6-7-0-1 | 2-3-0-1-6-7-4-5 | 2-3-4-5-6-7-8... |
| 3 | 0 | | 3-0-1-2 | 3-2-1-0 | 3-4-5-6-7-0-1-2 | 3-2-1-0-7-6-5-4 | 3-4-5-6-7-8-9... |
| 4 | 0 | | | | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 | 4-5-6-7-8-9-10... |
| 5 | 0 | | | | 5-6-7-0-1-2-3-4 | 5-4-7-6-1-0-3-2 | 5-6-7-8-9-10-11... |
| 6 | 0 | | | | 6-7-0-1-2-3-4-5 | 6-7-4-5-2-3-0-1 | 6-7-8-9-10-11-12... |
| 7 | 0 | | | | 7-0-1-2-3-4-5-6 | 7-6-5-4-3-2-1-0 | 7-8-9-10-11-12-13... |
| ... | ... | ... | ... | ... | ... | ... | ... |
| 14 | 0 | | | | | | 14-15-16-17-18-19-20 |
| 15 | 0 | | | | | | 15-16-17-18-19-20-21 |
| ... | ... | ... | ... | ... | ... | ... | ... |
| 0 | | 1 | 0-1-2-3 | N/A | 0-1-2-3-4-5-6-7 | N/A | 0-1-2-3-4-5-6... |
| 1 | | 1 | 1-2-3-4 | N/A | 1-2-3-4-5-6-7-8 | N/A | 1-2-3-4-5-6-7... |
| 2 | | 1 | 2-3-4-5 | N/A | 2-3-4-5-6-7-8-9 | N/A | 2-3-4-5-6-7-8... |
| 3 | | 1 | 3-4-5-6 | N/A | 3-4-5-6-7-8-9-10 | N/A | 3-4-5-6-7-8-9... |
| 4 | | 1 | | | 4-5-6-7-8-9-10-11 | N/A | 4-5-6-7-8-9-10... |
| 5 | | 1 | | | 5-6-7-8-9-10-11-12 | N/A | 5-6-7-8-9-10-11... |
| 6 | | 1 | | | 6-7-8-9-10-11-12-13 | N/A | 6-7-8-9-10-11-12... |
| 7 | | 1 | | | 7-8-9-10-11-12-13-14 | N/A | 7-8-9-10-11-12-13... |
| ... | ... | ... | ... | ... | ... | ... | ... |
| 14 | | 1 | | | | | 14-15-16-17-18-19-20 |
| 15 | | 1 | | | | | 15-16-17-18-19-20-21 |

Memory Organization – AT49BN3204

| Plane | Sector | Size (Words) | x16 Address Range (A20 - A0) |
|-------|--------|--------------|---------------------------------|
| A | SA0 | 4K | 00000 - 00FFF |
| A | SA1 | 4K | 01000 - 01FFF |
| A | SA2 | 4K | 02000 - 02FFF |
| A | SA3 | 4K | 03000 - 03FFF |
| A | SA4 | 4K | 04000 - 04FFF |
| A | SA5 | 4K | 05000 - 05FFF |
| A | SA6 | 4K | 06000 - 06FFF |
| A | SA7 | 4K | 07000 - 07FFF |
| A | SA8 | 32K | 08000 - 0FFFF |
| A | SA9 | 32K | 10000 - 17FFF |
| A | SA10 | 32K | 18000 - 1FFFF |
| A | SA11 | 32K | 20000 - 27FFF |
| A | SA12 | 32K | 28000 - 2FFFF |
| A | SA13 | 32K | 30000 - 37FFF |
| A | SA14 | 32K | 38000 - 3FFFF |
| B | SA15 | 32K | 40000 - 47FFF |
| B | SA16 | 32K | 48000 - 4FFFF |
| B | SA17 | 32K | 50000 - 57FFF |
| B | SA18 | 32K | 58000 - 5FFFF |
| B | SA19 | 32K | 60000 - 67FFF |
| B | SA20 | 32K | 68000 - 6FFFF |
| B | SA21 | 32K | 70000 - 77FFF |
| B | SA22 | 32K | 78000 - 7FFFF |
| C | SA23 | 32K | 80000 - 87FFF |
| C | SA24 | 32K | 88000 - 8FFFF |
| C | SA25 | 32K | 90000 - 97FFF |
| C | SA26 | 32K | 98000 - 9FFFF |
| C | SA27 | 32K | A0000 - A7FFF |
| C | SA28 | 32K | A8000 - AFFFF |
| C | SA29 | 32K | B0000 - B7FFF |
| C | SA30 | 32K | B8000 - BFFFF |
| C | SA31 | 32K | C0000 - C7FFF |
| C | SA32 | 32K | C8000 - CFFFF |
| C | SA33 | 32K | D0000 - D7FFF |
| C | SA34 | 32K | D8000 - DFFFF |
| C | SA35 | 32K | E0000 - E7FFF |

Memory Organization – AT49BN3204 (Continued)

| Plane | Sector | Size (Words) | x16 Address Range (A20 - A0) |
|-------|--------|--------------|---------------------------------|
| C | SA36 | 32K | E8000 - EFFFF |
| C | SA37 | 32K | F0000 - F7FFF |
| C | SA38 | 32K | F8000 - FFFFF |
| C | SA39 | 32K | 100000 - 107FFF |
| C | SA40 | 32K | 108000 - 10FFFF |
| C | SA41 | 32K | 110000 - 117FFF |
| C | SA42 | 32K | 118000 - 11FFFF |
| C | SA43 | 32K | 120000 - 127FFF |
| C | SA44 | 32K | 128000 - 12FFFF |
| C | SA45 | 32K | 130000 - 137FFF |
| C | SA46 | 32K | 138000 - 13FFFF |
| D | SA47 | 32K | 140000 - 147FFF |
| D | SA48 | 32K | 148000 - 14FFFF |
| D | SA49 | 32K | 150000 - 157FFF |
| D | SA50 | 32K | 158000 - 15FFFF |
| D | SA51 | 32K | 160000 - 167FFF |
| D | SA52 | 32K | 168000 - 16FFFF |
| D | SA53 | 32K | 170000 - 177FFF |
| D | SA54 | 32K | 178000 - 17FFFF |
| D | SA55 | 32K | 180000 - 187FFF |
| D | SA56 | 32K | 188000 - 18FFFF |
| D | SA57 | 32K | 190000 - 197FFF |
| D | SA58 | 32K | 198000 - 19FFFF |
| D | SA59 | 32K | 1A0000 - 1A7FFF |
| D | SA60 | 32K | 1A8000 - 1AFFFF |
| D | SA61 | 32K | 1B0000 - 1B7FFF |
| D | SA62 | 32K | 1B8000 - 1BFFFF |
| D | SA63 | 32K | 1C0000 - 1C7FFF |
| D | SA64 | 32K | 1C8000 - 1CFFFF |
| D | SA65 | 32K | 1D0000 - 1D7FFF |
| D | SA66 | 32K | 1D8000 - 1DFFFF |
| D | SA67 | 32K | 1E0000 - 1E7FFF |
| D | SA68 | 32K | 1E8000 - 1EFFFF |
| D | SA69 | 32K | 1F0000 - 1F7FFF |
| D | SA70 | 32K | 1F8000 - 1FFFFF |

Memory Organization – AT49BN3204T

| Plane | Sector | Size (Words) | x16 Address Range (A20 - A0) |
|-------|--------|--------------|---------------------------------|
| D | SA0 | 32K | 00000 - 07FFF |
| D | SA1 | 32K | 08000 - 0FFFF |
| D | SA2 | 32K | 10000 - 17FFF |
| D | SA3 | 32K | 18000 - 1FFFF |
| D | SA4 | 32K | 20000 - 27FFF |
| D | SA5 | 32K | 28000 - 2FFFF |
| D | SA6 | 32K | 30000 - 37FFF |
| D | SA7 | 32K | 38000 - 3FFFF |
| D | SA8 | 32K | 40000 - 47FFF |
| D | SA9 | 32K | 48000 - 4FFFF |
| D | SA10 | 32K | 50000 - 57FFF |
| D | SA11 | 32K | 58000 - 5FFFF |
| D | SA12 | 32K | 60000 - 67FFF |
| D | SA13 | 32K | 68000 - 6FFFF |
| D | SA14 | 32K | 70000 - 77FFF |
| D | SA15 | 32K | 78000 - 7FFFF |
| D | SA16 | 32K | 80000 - 87FFF |
| D | SA17 | 32K | 88000 - 8FFFF |
| D | SA18 | 32K | 90000 - 97FFF |
| D | SA19 | 32K | 98000 - 9FFFF |
| D | SA20 | 32K | A0000 - A7FFF |
| D | SA21 | 32K | A8000 - AFFFF |
| D | SA22 | 32K | B0000 - B7FFF |
| D | SA23 | 32K | B8000 - BFFFF |
| C | SA24 | 32K | C0000 - C7FFF |
| C | SA25 | 32K | C8000 - CFFFF |
| C | SA26 | 32K | D0000 - D7FFF |
| C | SA27 | 32K | D8000 - DFFFF |
| C | SA28 | 32K | E0000 - E7FFF |
| C | SA29 | 32K | E8000 - EFFFF |
| C | SA30 | 32K | F0000 - F7FFF |
| C | SA31 | 32K | F8000 - FFFFF |
| C | SA32 | 32K | 100000 - 107FFF |
| C | SA33 | 32K | 108000 - 10FFFF |
| C | SA34 | 32K | 110000 - 117FFF |
| C | SA35 | 32K | 118000 - 11FFFF |

Memory Organization – AT49BN3204T (Continued)

| Plane | Sector | Size (Words) | x16 Address Range (A20 - A0) |
|-------|--------|--------------|---------------------------------|
| C | SA36 | 32K | 120000 - 127FFF |
| C | SA37 | 32K | 128000 - 12FFFF |
| C | SA38 | 32K | 130000 - 137FFF |
| C | SA39 | 32K | 138000 - 13FFFF |
| C | SA40 | 32K | 140000 - 147FFF |
| C | SA41 | 32K | 148000 - 14FFFF |
| C | SA42 | 32K | 150000 - 157FFF |
| C | SA43 | 32K | 158000 - 15FFFF |
| C | SA44 | 32K | 160000 - 167FFF |
| C | SA45 | 32K | 168000 - 16FFFF |
| C | SA46 | 32K | 170000 - 177FFF |
| C | SA47 | 32K | 178000 - 17FFFF |
| B | SA48 | 32K | 180000 - 187FFF |
| B | SA49 | 32K | 188000 - 18FFFF |
| B | SA50 | 32K | 190000 - 197FFF |
| B | SA51 | 32K | 198000 - 19FFFF |
| B | SA52 | 32K | 1A0000 - 1A7FFF |
| B | SA53 | 32K | 1A8000 - 1AFFFF |
| B | SA54 | 32K | 1B0000 - 1B7FFF |
| B | SA55 | 32K | 1B8000 - 1BFFFF |
| A | SA56 | 32K | 1C0000 - 1C7FFF |
| A | SA57 | 32K | 1C8000 - 1CFFFF |
| A | SA58 | 32K | 1D0000 - 1D7FFF |
| A | SA59 | 32K | 1D8000 - 1DFFFF |
| A | SA60 | 32K | 1E0000 - 1E7FFF |
| A | SA61 | 32K | 1E8000 - 1EFFFF |
| A | SA62 | 32K | 1F0000 - 1F7FFF |
| A | SA63 | 4K | 1F8000 - 1F8FFF |
| A | SA64 | 4K | 1F9000 - 1F9FFF |
| A | SA65 | 4K | 1FA000 - 1FAFFF |
| A | SA66 | 4K | 1FB000 - 1FBFFF |
| A | SA67 | 4K | 1FC000 - 1FCFFF |
| A | SA68 | 4K | 1FD000 - 1FDFFF |
| A | SA69 | 4K | 1FE000 - 1FEFFF |
| A | SA70 | 4K | 1FF000 - 1FFFFF |

Memory Organization – AT49BN/BV64xx

| 6408 Plane | 641x Plane | Sector | Size (Words) | x16 Address Range (A21 - A0) |
|------------|------------|--------|--------------|------------------------------|
| A | A | SA0 | 4K | 00000 - 00FFF |
| A | A | SA1 | 4K | 01000 - 01FFF |
| A | A | SA2 | 4K | 02000 - 02FFF |
| A | A | SA3 | 4K | 03000 - 03FFF |
| A | A | SA4 | 4K | 04000 - 04FFF |
| A | A | SA5 | 4K | 05000 - 05FFF |
| A | A | SA6 | 4K | 06000 - 06FFF |
| A | A | SA7 | 4K | 07000 - 07FFF |
| A | A | SA8 | 32K | 08000 - 0FFFF |
| A | A | SA9 | 32K | 10000 - 17FFF |
| A | A | SA10 | 32K | 18000 - 1FFFF |
| A | A | SA11 | 32K | 20000 - 27FFF |
| A | A | SA12 | 32K | 28000 - 2FFFF |
| A | A | SA13 | 32K | 30000 - 37FFF |
| A | A | SA14 | 32K | 38000 - 3FFFF |
| A | A | SA15 | 32K | 40000 - 47FFF |
| A | A | SA16 | 32K | 48000 - 4FFFF |
| A | A | SA17 | 32K | 50000 - 57FFF |
| A | A | SA18 | 32K | 58000 - 5FFFF |
| A | A | SA19 | 32K | 60000 - 67FFF |
| A | A | SA20 | 32K | 68000 - 6FFFF |
| A | A | SA21 | 32K | 70000 - 77FFF |
| A | A | SA22 | 32K | 78000 - 7FFFF |
| B | A | SA23 | 32K | 80000 - 87FFF |
| B | A | SA24 | 32K | 88000 - 8FFFF |
| B | A | SA25 | 32K | 90000 - 97FFF |
| B | A | SA26 | 32K | 98000 - 9FFFF |
| B | A | SA27 | 32K | A0000 - A7FFF |
| B | A | SA28 | 32K | A8000 - AFFFF |
| B | A | SA29 | 32K | B0000 - B7FFF |
| B | A | SA30 | 32K | B8000 - BFFFF |
| B | A | SA31 | 32K | C0000 - C7FFF |
| B | A | SA32 | 32K | C8000 - CFFFF |
| B | A | SA33 | 32K | D0000 - D7FFF |
| B | A | SA34 | 32K | D8000 - DFFFF |
| B | A | SA35 | 32K | E0000 - E7FFF |
| B | A | SA36 | 32K | E8000 - EFFFF |
| B | A | SA37 | 32K | F0000 - F7FFF |
| B | A | SA38 | 32K | F8000 - FFFFF |
| B | B | SA39 | 32K | 100000 - 107FFF |
| B | B | SA40 | 32K | 108000 - 10FFFF |
| B | B | SA41 | 32K | 110000 - 117FFF |
| B | B | SA42 | 32K | 118000 - 11FFFF |
| B | B | SA43 | 32K | 120000 - 127FFF |
| B | B | SA44 | 32K | 128000 - 12FFFF |

Memory Organization – AT49BN/BV64xx (Continued)

| 6408 Plane | 641x Plane | Sector | Size (Words) | x16 Address Range (A21 - A0) |
|------------|------------|--------|--------------|------------------------------|
| B | B | SA45 | 32K | 130000 - 137FFF |
| B | B | SA46 | 32K | 138000 - 13FFFF |
| B | B | SA47 | 32K | 140000 - 147FFF |
| B | B | SA48 | 32K | 148000 - 14FFFF |
| B | B | SA49 | 32K | 150000 - 157FFF |
| B | B | SA50 | 32K | 158000 - 15FFFF |
| B | B | SA51 | 32K | 160000 - 167FFF |
| B | B | SA52 | 32K | 168000 - 16FFFF |
| B | B | SA53 | 32K | 170000 - 177FFF |
| B | B | SA54 | 32K | 178000 - 17FFFF |
| B | B | SA55 | 32K | 180000 - 187FFF |
| B | B | SA56 | 32K | 188000 - 18FFFF |
| B | B | SA57 | 32K | 190000 - 197FFF |
| B | B | SA58 | 32K | 198000 - 19FFFF |
| B | B | SA59 | 32K | 1A0000 - 1A7FFF |
| B | B | SA60 | 32K | 1A8000 - 1AFFFF |
| B | B | SA61 | 32K | 1B0000 - 1B7FFF |
| B | B | SA62 | 32K | 1B8000 - 1BFFFF |
| B | B | SA63 | 32K | 1C0000 - 1C7FFF |
| B | B | SA64 | 32K | 1C8000 - 1CFFFF |
| B | B | SA65 | 32K | 1D0000 - 1D7FFF |
| B | B | SA66 | 32K | 1D8000 - 1DFFFF |
| B | B | SA67 | 32K | 1E0000 - 1E7FFF |
| B | B | SA68 | 32K | 1E8000 - 1EFFFF |
| B | B | SA69 | 32K | 1F0000 - 1F7FFF |
| B | B | SA70 | 32K | 1F8000 - 1FFFFF |
| C | C | SA71 | 32K | 200000 - 207FFF |
| C | C | SA72 | 32K | 208000 - 20FFFF |
| C | C | SA73 | 32K | 210000 - 217FFF |
| C | C | SA74 | 32K | 218000 - 21FFFF |
| C | C | SA75 | 32K | 220000 - 227FFF |
| C | C | SA76 | 32K | 228000 - 22FFFF |
| C | C | SA77 | 32K | 230000 - 237FFF |
| C | C | SA78 | 32K | 238000 - 23FFFF |
| C | C | SA79 | 32K | 240000 - 247FFF |
| C | C | SA80 | 32K | 248000 - 24FFFF |
| C | C | SA81 | 32K | 250000 - 257FFF |
| C | C | SA82 | 32K | 258000 - 25FFFF |
| C | C | SA83 | 32K | 260000 - 267FFF |
| C | C | SA84 | 32K | 268000 - 26FFFF |
| C | C | SA85 | 32K | 270000 - 277FFF |
| C | C | SA86 | 32K | 278000 - 27FFFF |
| C | C | SA87 | 32K | 280000 - 287FFF |
| C | C | SA88 | 32K | 288000 - 28FFFF |
| C | C | SA89 | 32K | 290000 - 297FFF |

Memory Organization – AT49BN/BV64xx (Continued)

| 6408 Plane | 641x Plane | Sector | Size (Words) | x16 Address Range (A21 - A0) |
|------------|------------|--------|--------------|------------------------------|
| C | C | SA90 | 32K | 298000 - 29FFFF |
| C | C | SA91 | 32K | 2A0000 - 2A7FFF |
| C | C | SA92 | 32K | 2A8000 - 2AFFFF |
| C | C | SA93 | 32K | 2B0000 - 2B7FFF |
| C | C | SA94 | 32K | 2B8000 - 2BFFFF |
| C | C | SA95 | 32K | 2C0000 - 2C7FFF |
| C | C | SA96 | 32K | 2C8000 - 2CFFFF |
| C | C | SA97 | 32K | 2D0000 - 2D7FFF |
| C | C | SA98 | 32K | 2D8000 - 2DFFFF |
| C | C | SA99 | 32K | 2E0000 - 2E7FFF |
| C | C | SA100 | 32K | 2E8000 - 2EFFFF |
| C | C | SA101 | 32K | 2F0000 - 2F7FFF |
| C | D | SA102 | 32K | 2F8000 - 2FFFFF |
| C | D | SA103 | 32K | 300000 - 307FFF |
| C | D | SA104 | 32K | 308000 - 30FFFF |
| C | D | SA105 | 32K | 310000 - 317FFF |
| C | D | SA106 | 32K | 318000 - 31FFFF |
| C | D | SA107 | 32K | 320000 - 327FFF |
| C | D | SA108 | 32K | 328000 - 32FFFF |
| C | D | SA109 | 32K | 330000 - 337FFF |
| C | D | SA110 | 32K | 338000 - 33FFFF |
| C | D | SA111 | 32K | 340000 - 347FFF |
| C | D | SA112 | 32K | 348000 - 34FFFF |

Memory Organization – AT49BN/BV64xx (Continued)

| 6408 Plane | 641x Plane | Sector | Size (Words) | x16 Address Range (A21 - A0) |
|------------|------------|--------|--------------|------------------------------|
| C | D | SA113 | 32K | 350000 - 357FFF |
| C | D | SA114 | 32K | 358000 - 35FFFF |
| C | D | SA115 | 32K | 360000 - 367FFF |
| C | D | SA116 | 32K | 368000 - 36FFFF |
| C | D | SA117 | 32K | 370000 - 377FFF |
| C | D | SA118 | 32K | 378000 - 37FFFF |
| D | D | SA119 | 32K | 380000 - 387FFF |
| D | D | SA120 | 32K | 388000 - 38FFFF |
| D | D | SA121 | 32K | 390000 - 397FFF |
| D | D | SA122 | 32K | 398000 - 39FFFF |
| D | D | SA123 | 32K | 3A0000 - 3A7FFF |
| D | D | SA124 | 32K | 3A8000 - 3AFFFF |
| D | D | SA125 | 32K | 3B0000 - 3B7FFF |
| D | D | SA126 | 32K | 3B8000 - 3BFFFF |
| D | D | SA127 | 32K | 3C0000 - 3C7FFF |
| D | D | SA128 | 32K | 3C8000 - 3CFFFF |
| D | D | SA129 | 32K | 3D0000 - 3D7FFF |
| D | D | SA130 | 32K | 3D8000 - 3DFFFF |
| D | D | SA131 | 32K | 3E0000 - 3E7FFF |
| D | D | SA132 | 32K | 3E8000 - 3EFFFF |
| D | D | SA133 | 32K | 3F0000 - 3F7FFF |
| D | D | SA134 | 32K | 3F8000 - 3FFFFF |

Memory Organization – AT49BN/BV64xxT

| 6408T Plane | 641xT Plane | Sector | Size (Words) | x16 Address Range (A21 - A0) |
|-------------|-------------|--------|--------------|------------------------------|
| D | D | SA0 | 32K | 00000 - 07FFF |
| D | D | SA1 | 32K | 08000 - 0FFFF |
| D | D | SA2 | 32K | 10000 - 17FFF |
| D | D | SA3 | 32K | 18000 - 1FFFF |
| D | D | SA4 | 32K | 20000 - 27FFF |
| D | D | SA5 | 32K | 28000 - 2FFFF |
| D | D | SA6 | 32K | 30000 - 37FFF |
| D | D | SA7 | 32K | 38000 - 3FFFF |
| D | D | SA8 | 32K | 40000 - 47FFF |
| D | D | SA9 | 32K | 48000 - 4FFFF |
| D | D | SA10 | 32K | 50000 - 57FFF |
| D | D | SA11 | 32K | 58000 - 5FFFF |
| D | D | SA12 | 32K | 60000 - 67FFF |
| D | D | SA13 | 32K | 68000 - 6FFFF |
| D | D | SA14 | 32K | 70000 - 77FFF |
| D | D | SA15 | 32K | 78000 - 7FFFF |
| C | D | SA16 | 32K | 80000 - 87FFF |
| C | D | SA17 | 32K | 88000 - 8FFFF |
| C | D | SA18 | 32K | 90000 - 97FFF |
| C | D | SA19 | 32K | 98000 - 9FFFF |
| C | D | SA20 | 32K | A0000 - A7FFF |
| C | D | SA21 | 32K | A8000 - AFFFF |
| C | D | SA22 | 32K | B0000 - B7FFF |
| C | D | SA23 | 32K | B8000 - BFFFF |
| C | D | SA24 | 32K | C0000 - C7FFF |
| C | D | SA25 | 32K | C8000 - CFFFF |
| C | D | SA26 | 32K | D0000 - D7FFF |
| C | D | SA27 | 32K | D8000 - DFFFF |
| C | D | SA28 | 32K | E0000 - E7FFF |
| C | D | SA29 | 32K | E8000 - EFFFF |
| C | D | SA30 | 32K | F0000 - F7FFF |
| C | D | SA31 | 32K | F8000 - FFFFF |
| C | C | SA32 | 32K | 100000 - 107FFF |
| C | C | SA33 | 32K | 108000 - 10FFFF |
| C | C | SA34 | 32K | 110000 - 117FFF |
| C | C | SA35 | 32K | 118000 - 11FFFF |
| C | C | SA36 | 32K | 120000 - 127FFF |
| C | C | SA37 | 32K | 128000 - 12FFFF |
| C | C | SA38 | 32K | 130000 - 137FFF |
| C | C | SA39 | 32K | 138000 - 13FFFF |
| C | C | SA40 | 32K | 140000 - 147FFF |
| C | C | SA41 | 32K | 148000 - 14FFFF |
| C | C | SA42 | 32K | 150000 - 157FFF |
| C | C | SA43 | 32K | 158000 - 15FFFF |
| C | C | SA44 | 32K | 160000 - 167FFF |

Memory Organization – AT49BN/BV64xxT (Continued)

| 6408T Plane | 641xT Plane | Sector | Size (Words) | x16 Address Range (A21 - A0) |
|-------------|-------------|--------|--------------|------------------------------|
| C | C | SA45 | 32K | 168000 - 16FFFF |
| C | C | SA46 | 32K | 170000 - 177FFF |
| C | C | SA47 | 32K | 178000 - 17FFFF |
| C | C | SA48 | 32K | 180000 - 187FFF |
| C | C | SA49 | 32K | 188000 - 18FFFF |
| C | C | SA50 | 32K | 190000 - 197FFF |
| C | C | SA51 | 32K | 198000 - 19FFFF |
| C | C | SA52 | 32K | 1A0000 - 1A7FFF |
| C | C | SA53 | 32K | 1A8000 - 1AFFFF |
| C | C | SA54 | 32K | 1B0000 - 1B7FFF |
| C | C | SA55 | 32K | 1B8000 - 1BFFFF |
| C | C | SA56 | 32K | 1C0000 - 1C7FFF |
| C | C | SA57 | 32K | 1C8000 - 1CFFFF |
| C | C | SA58 | 32K | 1D0000 - 1D7FFF |
| C | C | SA59 | 32K | 1D8000 - 1DFFFF |
| C | C | SA60 | 32K | 1E0000 - 1E7FFF |
| C | C | SA61 | 32K | 1E8000 - 1EFFFF |
| C | C | SA62 | 32K | 1F0000 - 1F7FFF |
| C | C | SA63 | 32K | 1F8000 - 1FFFFF |
| B | B | SA64 | 32K | 200000 - 207FFF |
| B | B | SA65 | 32K | 208000 - 20FFFF |
| B | B | SA66 | 32K | 210000 - 217FFF |
| B | B | SA67 | 32K | 218000 - 21FFFF |
| B | B | SA68 | 32K | 220000 - 227FFF |
| B | B | SA69 | 32K | 228000 - 22FFFF |
| B | B | SA70 | 32K | 230000 - 237FFF |
| B | B | SA71 | 32K | 238000 - 23FFFF |
| B | B | SA72 | 32K | 240000 - 247FFF |
| B | B | SA73 | 32K | 248000 - 24FFFF |
| B | B | SA74 | 32K | 250000 - 257FFF |
| B | B | SA75 | 32K | 258000 - 25FFFF |
| B | B | SA76 | 32K | 260000 - 267FFF |
| B | B | SA77 | 32K | 268000 - 26FFFF |
| B | B | SA78 | 32K | 270000 - 277FFF |
| B | B | SA79 | 32K | 278000 - 27FFFF |
| B | B | SA80 | 32K | 280000 - 287FFF |
| B | B | SA81 | 32K | 288000 - 28FFFF |
| B | B | SA82 | 32K | 290000 - 297FFF |
| B | B | SA83 | 32K | 298000 - 29FFFF |
| B | B | SA84 | 32K | 2A0000 - 2A7FFF |
| B | B | SA85 | 32K | 2A8000 - 2AFFFF |
| B | B | SA86 | 32K | 2B0000 - 2B7FFF |
| B | B | SA87 | 32K | 2B8000 - 2BFFFF |
| B | B | SA88 | 32K | 2C0000 - 2C7FFF |
| B | B | SA89 | 32K | 2C8000 - 2CFFFF |

Memory Organization – AT49BN/BV64xxT (Continued)

| 6408T Plane | 641xT Plane | Sector | Size (Words) | x16 Address Range (A21 - A0) |
|-------------|-------------|--------|--------------|------------------------------|
| B | B | SA90 | 32K | 2D0000 - 2D7FFF |
| B | B | SA91 | 32K | 2D8000 - 2DFFFF |
| B | B | SA92 | 32K | 2E0000 - 2E7FFF |
| B | B | SA93 | 32K | 2E8000 - 2EFFFF |
| B | B | SA94 | 32K | 2F0000 - 2F7FFF |
| B | B | SA95 | 32K | 2F8000 - 2FFFFF |
| B | A | SA96 | 32K | 300000 - 307FFF |
| B | A | SA97 | 32K | 308000 - 30FFFF |
| B | A | SA98 | 32K | 310000 - 317FFF |
| B | A | SA99 | 32K | 318000 - 31FFFF |
| B | A | SA100 | 32K | 320000 - 327FFF |
| B | A | SA101 | 32K | 328000 - 32FFFF |
| B | A | SA102 | 32K | 330000 - 337FFF |
| B | A | SA103 | 32K | 338000 - 33FFFF |
| B | A | SA104 | 32K | 340000 - 347FFF |
| B | A | SA105 | 32K | 348000 - 34FFFF |
| B | A | SA106 | 32K | 350000 - 357FFF |
| B | A | SA107 | 32K | 358000 - 35FFFF |
| B | A | SA108 | 32K | 360000 - 367FFF |
| B | A | SA109 | 32K | 368000 - 36FFFF |
| B | A | SA110 | 32K | 370000 - 377FFF |
| B | A | SA111 | 32K | 378000 - 37FFFF |
| A | A | SA112 | 32K | 380000 - 387FFF |

Memory Organization – AT49BN/BV64xxT (Continued)

| 6408T Plane | 641xT Plane | Sector | Size (Words) | x16 Address Range (A21 - A0) |
|-------------|-------------|--------|--------------|------------------------------|
| A | A | SA113 | 32K | 388000 - 38FFFF |
| A | A | SA114 | 32K | 390000 - 397FFF |
| A | A | SA115 | 32K | 398000 - 39FFFF |
| A | A | SA116 | 32K | 3A0000 - 3A7FFF |
| A | A | SA117 | 32K | 3A8000 - 3AFFFF |
| A | A | SA118 | 32K | 3B0000 - 3B7FFF |
| A | A | SA119 | 32K | 3B8000 - 3BFFFF |
| A | A | SA120 | 32K | 3C0000 - 3C7FFF |
| A | A | SA121 | 32K | 3C8000 - 3CFFFF |
| A | A | SA122 | 32K | 3D0000 - 3D7FFF |
| A | A | SA123 | 32K | 3D8000 - 3DFFFF |
| A | A | SA124 | 32K | 3E0000 - 3E7FFF |
| A | A | SA125 | 32K | 3E8000 - 3EFFFF |
| A | A | SA126 | 32K | 3F0000 - 3F7FFF |
| A | A | SA127 | 4K | 3F8000 - 3F8FFF |
| A | A | SA128 | 4K | 3F9000 - 3F9FFF |
| A | A | SA129 | 4K | 3FA000 - 3FAFFF |
| A | A | SA130 | 4K | 3FB000 - 3FBFFF |
| A | A | SA131 | 4K | 3FC000 - 3FCFFF |
| A | A | SA132 | 4K | 3FD000 - 3FDFFF |
| A | A | SA133 | 4K | 3FE000 - 3FEFFF |
| A | A | SA134 | 4K | 3FF000 - 3FFFFF |

DC and AC Operating Range

| | | AT49BN/BV64xx(T)/3204(T) - 70 | AT49BN/BV64xx(T)/3204(T) - 85 |
|------------------------------|------------|-------------------------------|-------------------------------|
| Operating Temperature (Case) | Industrial | -40°C - 85°C | -40°C - 85°C |
| V _{CC} Power Supply | | 2.7V - 3.1V | 2.7V - 3.1V |

Operating Modes

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | \overline{RESET} | V _{PP} ⁽⁶⁾ | Ai | I/O |
|------------------------------|-----------------|------------------|-----------------|--------------------|----------------------------------|--|----------------------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | V _{IH} | X | Ai | D _{OUT} |
| Burst Read | V _{IL} | V _{IL} | V _{IH} | V _{IH} | X | Ai | D _{OUT} |
| Program/Erase ⁽³⁾ | V _{IL} | V _{IH} | V _{IL} | V _{IH} | V _{IHPP} ⁽⁷⁾ | Ai | D _{IN} |
| Standby/Program Inhibit | V _{IH} | X ⁽¹⁾ | X | V _{IH} | X | X | High Z |
| Program Inhibit | X | X | V _{IH} | V _{IH} | X | | |
| | X | V _{IL} | X | V _{IH} | X | | |
| | X | X | X | X | V _{ILPP} ⁽⁸⁾ | | |
| Output Disable | X | V _{IH} | X | V _{IH} | X | | High Z |
| Reset | X | X | X | V _{IL} | X | X | High Z |
| Product Identification | | | | | | | |
| Hardware | V _{IL} | V _{IL} | V _{IH} | V _{IH} | | A1 - A21 = V _{IL} , A9 = V _H ⁽³⁾ , A0 = V _{IL} | Manufacturer Code ⁽⁴⁾ |
| | | | | | | A1 - A21 = V _{IL} , A9 = V _H ⁽³⁾ , A0 = V _{IH} | Device Code ⁽⁴⁾ |
| Software ⁽⁵⁾ | | | | V _{IH} | | A0 = V _{IL} , A1 - A21 = V _{IL} | Manufacturer Code ⁽⁴⁾ |
| | | | | | | A0 = V _{IH} , A1 - A21 = V _{IL} | Device Code ⁽⁴⁾ |

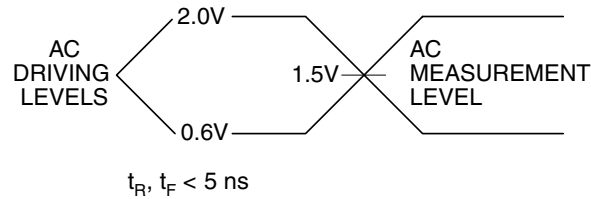
- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Refer to AC programming waveforms.
 3. V_H = 12.0V ± 0.5V.
 4. Manufacturer Code: 001FH; Device Code: 00D4H – AT49BN3204; 00D7H – AT49BN3204T; 00D6H - AT49BN6416/BV641; 00D2H - AT49BN6416T/BV641T.
 5. See details under “Software Product Identification Entry/Exit” on page 34.
 6. The V_{PP} pin can be tied to V_{CC}. For faster program/erase operations, V_{PP} can be set to 12.0V ± 0.5V.
 7. V_{IHPP} (min) = 1.65V.
 8. V_{ILPP} (max) = 0.8V.

DC Characteristics

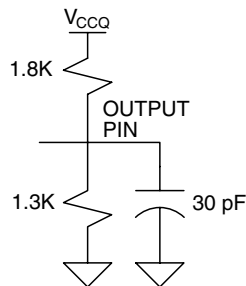
| Symbol | Parameter | Condition | Min | Max | Units |
|----------------|-----------------------------------|--|-----------------|------|---------|
| I_{LI} | Input Load Current | $V_{IN} = 0V$ to V_{CC} | | 1 | μA |
| I_{LO} | Output Leakage Current | $V_{I/O} = 0V$ to V_{CC} | | 1 | μA |
| I_{SB1} | V_{CC} Standby Current CMOS | $\overline{CE} = V_{CCQ} - 0.3V$ to V_{CC} | | 10 | μA |
| $I_{CC}^{(1)}$ | V_{CC} Active Current | $f = 66\text{ MHz}; I_{OUT} = 0\text{ mA}$ | | 30 | mA |
| I_{CCRE} | V_{CC} Read While Erase Current | $f = 66\text{ MHz}; I_{OUT} = 0\text{ mA}$ | | 50 | mA |
| I_{CCRW} | V_{CC} Read While Write Current | $f = 66\text{ MHz}; I_{OUT} = 0\text{ mA}$ | | 50 | mA |
| V_{IL} | Input Low Voltage | | | 0.6 | V |
| V_{IH} | Input High Voltage | | $V_{CCQ} - 0.6$ | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1\text{ mA}$ | | 0.45 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -100\text{ }\mu A; V_{CCQ} = 1.65V - 2.2V$ | $V_{CCQ} - 0.1$ | | V |
| | | $I_{OH} = -400\text{ }\mu A; V_{CCQ} = 2.7V - 3.1V$ | 2.4 | | |

Note: 1. In the erase mode, I_{CC} is 30 mA.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

$f = 1\text{ MHz}, T = 25^\circ C^{(1)}$

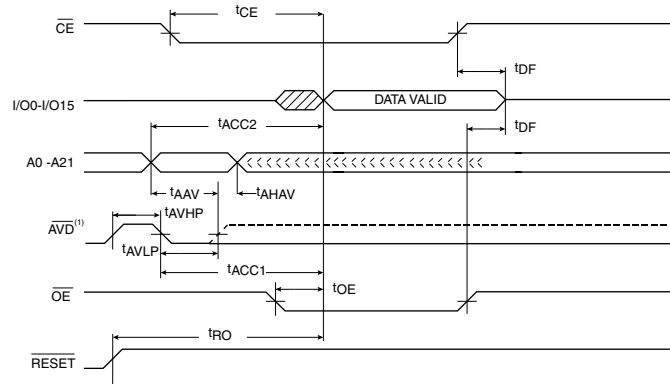
| | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 4 | 6 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 8 | 12 | pF | $V_{OUT} = 0V$ |

Note: 1. This parameter is characterized and is not 100% tested.

AC Asynchronous Read Timing Characteristics

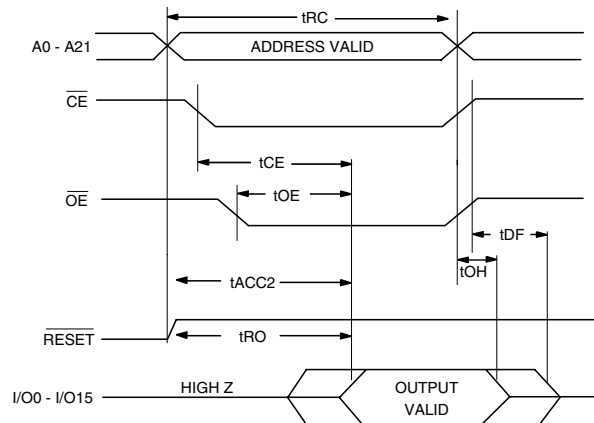
| Symbol | Parameter | Min | Max | Units |
|------------|--|-----|-----|-------|
| t_{ACC1} | Access, \overline{AVD} To Data Valid | | 70 | ns |
| t_{ACC2} | Access, Address to Data Valid | | 70 | ns |
| t_{CE} | Access, \overline{CE} to Data Valid | | 70 | ns |
| t_{OE} | \overline{OE} to Data Valid | | 20 | ns |
| t_{AHAV} | Address Hold from \overline{AVD} | 9 | | ns |
| t_{AVLP} | \overline{AVD} Low Pulse Width | 10 | | ns |
| t_{AVHP} | \overline{AVD} High Pulse Width | 10 | | ns |
| t_{AAV} | Address Valid to \overline{AVD} | 7 | | ns |
| t_{DF} | \overline{CE} , \overline{OE} High to Data Float | | 25 | ns |
| t_{RO} | \overline{RESET} to Output Delay | | 150 | ns |

\overline{AVD} Pulsed Asynchronous Read Cycle Waveform⁽¹⁾⁽²⁾



- Note:
1. After the high-to-low transition on \overline{AVD} , \overline{AVD} may remain low as long as the address is stable.
 2. CLK may be static high or static low.

Asynchronous Read Cycle Waveform⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

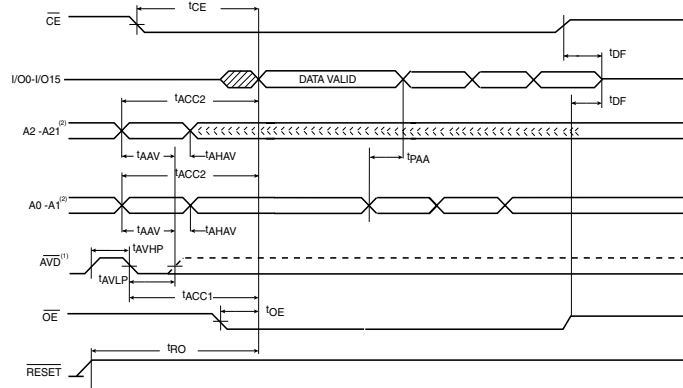


- Notes:
1. \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 3. t_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first (CL = 5 pF).
 4. \overline{AVD} and CLK should be tied low.

AC Asynchronous Read Timing Characteristics

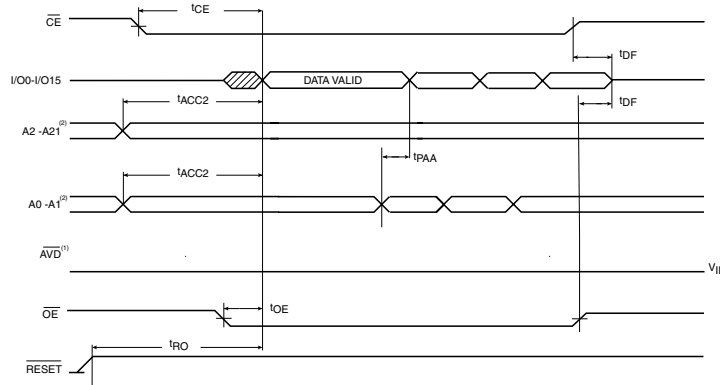
| Symbol | Parameter | Min | Max | Units |
|------------|--|-----|-----|-------|
| t_{ACC1} | Access, \overline{AVD} To Data Valid | | 70 | ns |
| t_{ACC2} | Access, Address to Data Valid | | 70 | ns |
| t_{CE} | Access, \overline{CE} to Data Valid | | 70 | ns |
| t_{OE} | \overline{OE} to Data Valid | | 20 | ns |
| t_{AHAV} | Address Hold from \overline{AVD} | 9 | | ns |
| t_{AVLP} | \overline{AVD} Low Pulse Width | 10 | | ns |
| t_{AVHP} | \overline{AVD} High Pulse Width | 10 | | ns |
| t_{AAV} | Address Valid to \overline{AVD} | 7 | | ns |
| t_{DF} | \overline{CE} , \overline{OE} High to Data Float | | 25 | ns |
| t_{RO} | \overline{RESET} to Output Delay | | 150 | ns |
| t_{PAA} | Page Address Access Time | | 20 | ns |

Page Read Cycle Waveform 1⁽¹⁾⁽²⁾



- Notes:
1. After the high-to-low transition on \overline{AVD} , \overline{AVD} may remain low as long as the page address is stable.
 2. The diagram shown is for a four-word page read. For an eight-word page read A0 - A1 becomes A0 - A2 and A2 - A21 becomes A3 - A21.

Page Read Cycle Waveform 2⁽¹⁾⁽²⁾

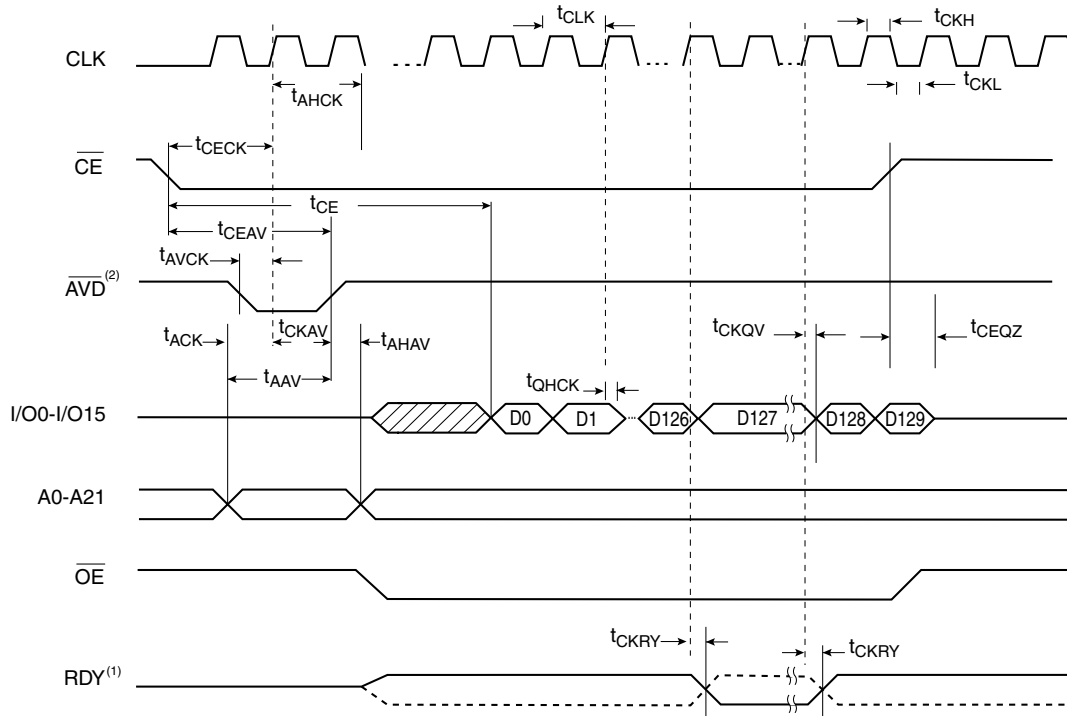


- Notes:
1. \overline{AVD} may remain low as long as the page address is stable.
 2. The diagram shown is for a four-word page read. For an eight-word page read A0 - A1 becomes A0 - A2 and A2 - A21 becomes A3 - A21.

AC Burst Read Timing Characteristics

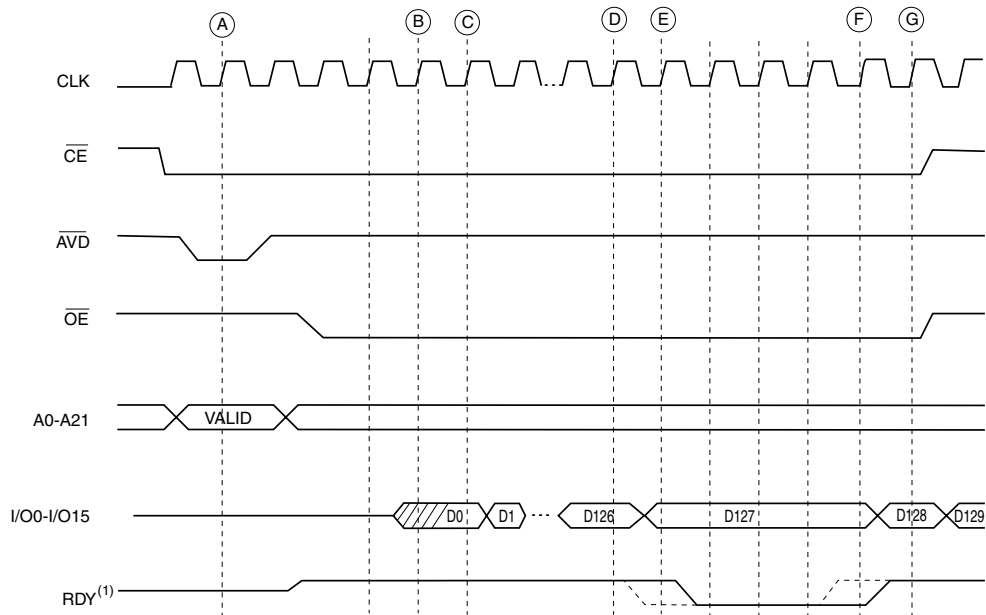
| Symbol | Parameter | Min | Max | Units |
|------------|---|-----|------|-------|
| t_{CLK} | CLK Period | 15 | | ns |
| t_{CKH} | CLK High Time | 4 | | ns |
| t_{CKL} | CLK Low Time | 4 | | ns |
| t_{CKRT} | CLK Rise Time | | 3.5 | ns |
| t_{CKFT} | CLK Fall Time | | 3.5 | ns |
| t_{ACK} | Address Valid to Clock | 7 | | ns |
| t_{AVCK} | \overline{AVD} Low to Clock | 7 | | ns |
| t_{CECK} | \overline{CE} Low to Clock | 7 | | ns |
| t_{CKAV} | Clock to \overline{AVD} High | 3 | | ns |
| t_{QHCK} | Output Hold from Clock | 3 | | ns |
| t_{AHCK} | Address Hold from Clock | 8 | | ns |
| t_{CKRY} | Clock to RDY Delay | | 13.0 | ns |
| t_{CEAV} | \overline{CE} Setup to \overline{AVD} | 7 | | ns |
| t_{AAV} | Address Valid to \overline{AVD} | 7 | | ns |
| t_{AHAV} | Address Hold From \overline{AVD} | 9 | | ns |
| t_{CKQV} | CLK to Data Delay | | 13.0 | ns |
| t_{CEQZ} | \overline{CE} High to Output High-Z | | 10 | ns |

Burst Read Cycle Waveform



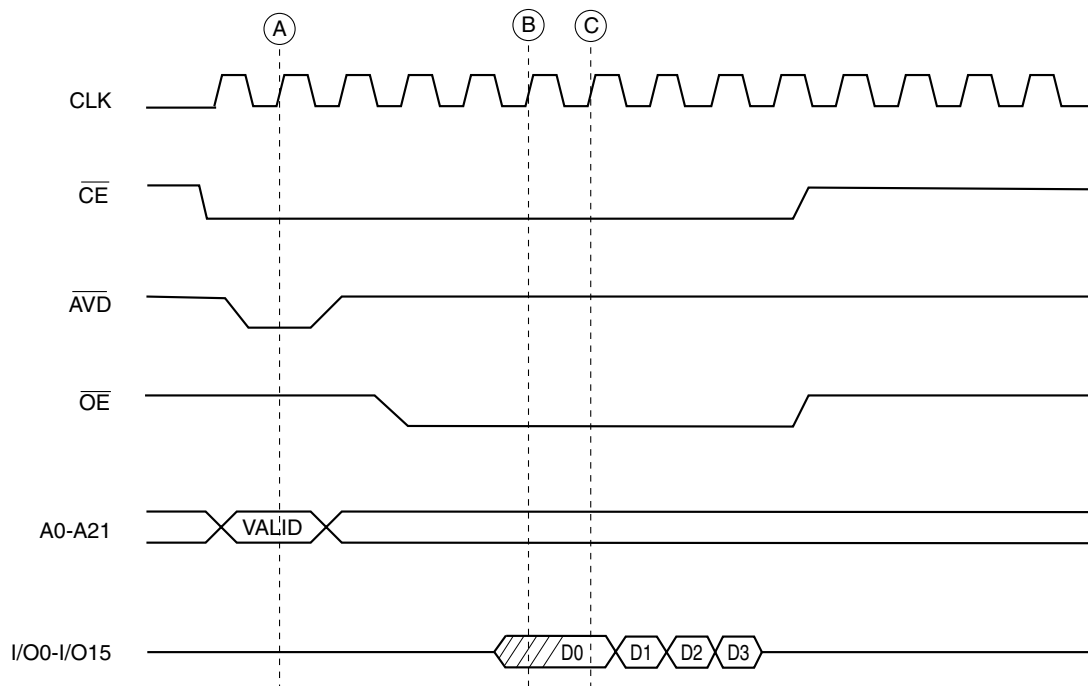
- Notes:
1. The RDY signal (solid line) shown is for a burst configuration register setting of B10 and B8 = 0. The RDY Signal (dashed line) shown is for a burst configuration setting of B10 = 1 and B8 = 0.
 2. After the high-to-low transition on \overline{AVD} , \overline{AVD} may remain low.

Burst Read Waveform (Clock Latency of 4)



Note: 1. Solid line reflects a B10 and B8 setting of 0 in the configuration register. Dashed line reflects a B10 setting of 0 and B8 setting of 1 in the configuration register.

Four-word Burst Read Waveform (Clock Latency of 4)

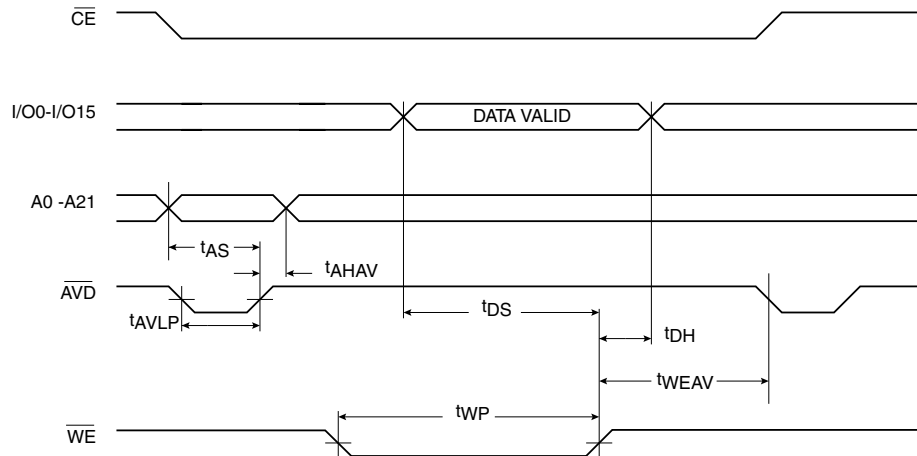


AC Word Load Characteristics 1

| Symbol | Parameter | Min | Max | Units |
|------------|--|-----|-----|-------|
| t_{AS} | Address, \overline{CE} Setup Time to \overline{AVD} High | 10 | | ns |
| t_{AHAV} | Address Hold Time from \overline{AVD} High | 9 | | ns |
| t_{AVLP} | \overline{AVD} Low Pulse Width | 10 | | ns |
| t_{DS} | Data Setup Time | 15 | | ns |
| t_{DH} | Data Hold Time | 0 | | ns |
| t_{CEAV} | \overline{CE} Setup to \overline{AVD} | 10 | | ns |
| t_{WP} | \overline{CE} or \overline{WE} Low Pulse Width | 35 | | ns |
| t_{WPH} | \overline{CE} or \overline{WE} High Pulse Width | 25 | | ns |
| t_{WEAV} | \overline{WE} High Time to \overline{AVD} Low | 25 | | ns |
| t_{CEAV} | \overline{CE} High Time to \overline{AVD} Low | 25 | | ns |

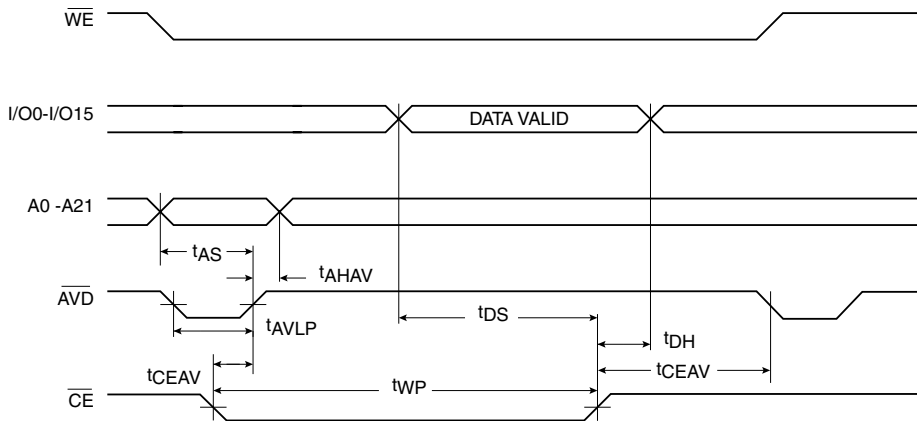
AC Word Load Waveforms 1

\overline{WE} Controlled⁽¹⁾



Note: 1. After the high-to-low transition on \overline{AVD} , \overline{AVD} may remain low as long as the CLK input does not toggle.

\overline{CE} Controlled⁽¹⁾



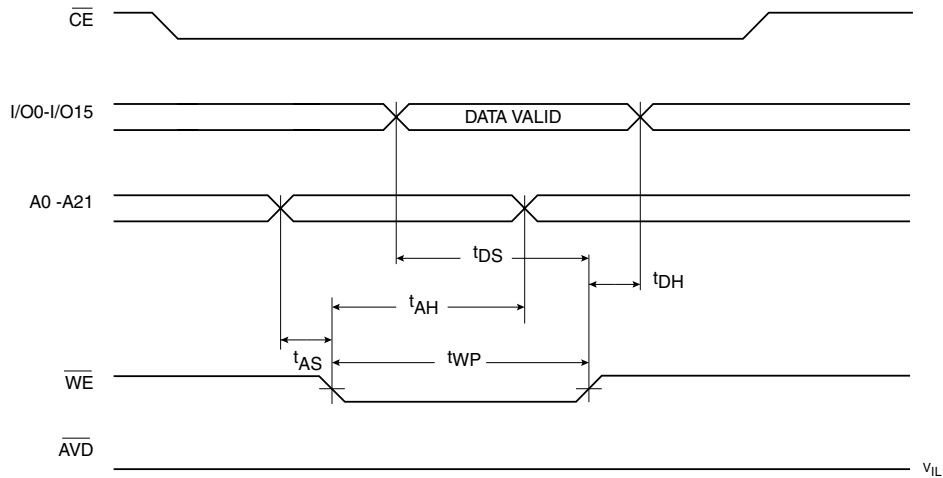
Note: 1. After the high-to-low transition on \overline{AVD} , \overline{AVD} may remain low as long as the CLK input does not toggle.

AC Word Load Characteristics 2

| Symbol | Parameter | Min | Max | Units |
|-----------|---|-----|-----|-------|
| t_{AS} | Address Setup Time to \overline{WE} and \overline{CE} Low | 0 | | ns |
| t_{AH} | Address Hold Time | 20 | | ns |
| t_{DS} | Data Setup Time | 20 | | ns |
| t_{DH} | Data Hold Time | 0 | | ns |
| t_{WP} | \overline{CE} or \overline{WE} Low Pulse Width | 35 | | ns |
| t_{WPH} | \overline{CE} or \overline{WE} High Pulse Width | 25 | | ns |

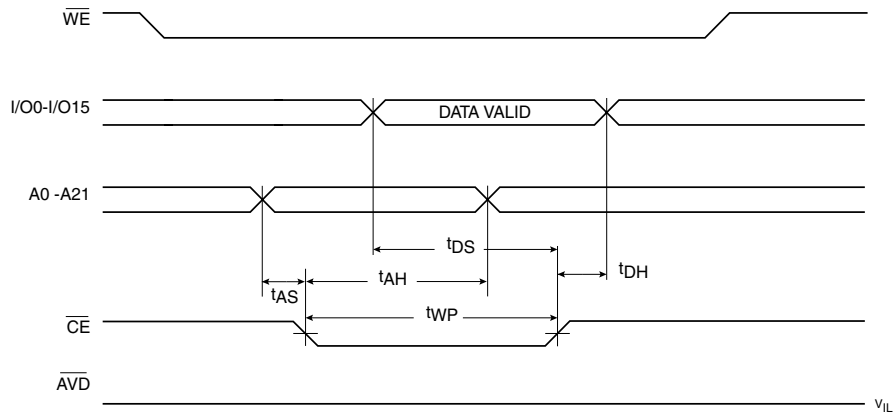
AC Word Load Waveforms 2

\overline{WE} Controlled⁽¹⁾



Note: 1. The CLK input should not toggle.

\overline{CE} Controlled⁽¹⁾

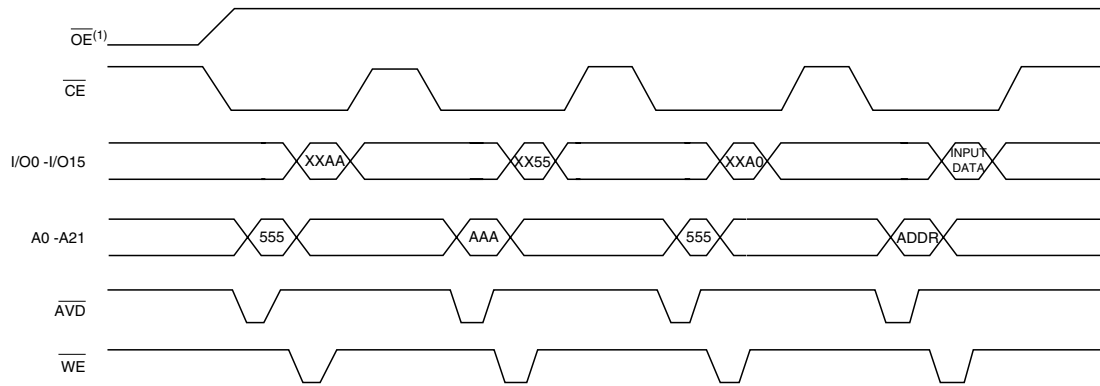


Note: 1. The CLK input should not toggle.

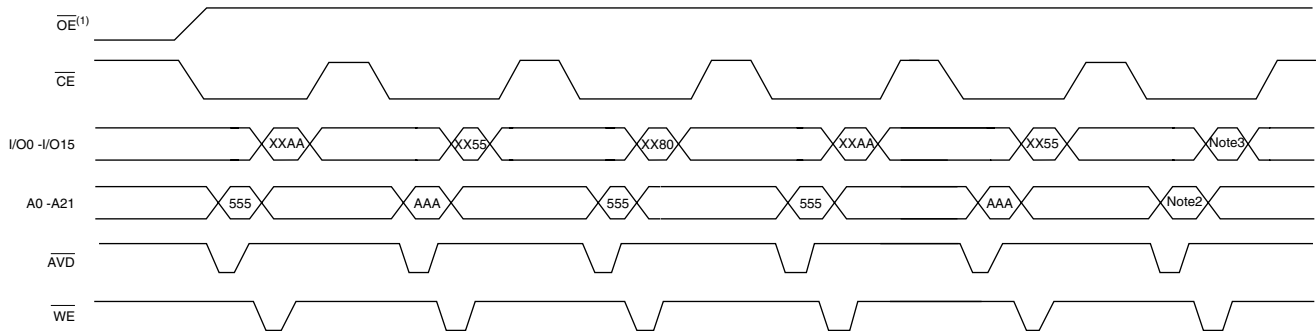
Program Cycle Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|-------------|---|-----|-----|-----|---------|
| t_{BP} | Word Programming Time ($V_{pp} = V_{CC}$) | | 22 | | μs |
| t_{BPVPP} | Word Programming Time ($V_{pp} \geq 11.5V$) | | 10 | | μs |
| t_{SEC1} | Sector Erase Cycle Time (4K word sectors) | | 100 | | ms |
| t_{SEC2} | Sector Erase Cycle Time (32K word sectors) | | 500 | | ms |
| t_{ES} | Erase Suspend Time | | | 15 | μs |
| t_{PS} | Program Suspend Time | | | 10 | μs |

Program Cycle Waveforms



Sector, Plane or Chip Erase Cycle Waveforms



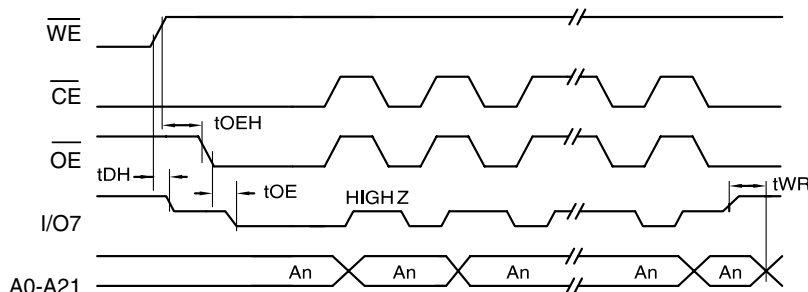
- Notes:
- \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.
 - For chip erase, the address should be 555. For plane or sector erase, the address depends on what plane or sector is to be erased. (See note 3 and 5 under Command Definitions on page 14.)
 - For chip erase, the data should be XX10H, for plane erase, the data should be XX20H, and for sector erase, the data should be XX30H
 - The waveforms shown above use the \overline{WE} controlled AC Word Load Waveforms 1.

Data Polling Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|--|-----|-----|-----|-------|
| t_{DH} | Data Hold Time | 10 | | | ns |
| $t_{OE\overline{H}}$ | \overline{OE} Hold Time | 10 | | | ns |
| t_{OE} | \overline{OE} to Output Delay ⁽²⁾ | | | | ns |
| t_{WR} | Write Recovery Time | 0 | | | ns |

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec on page 26.

Data Polling Waveforms

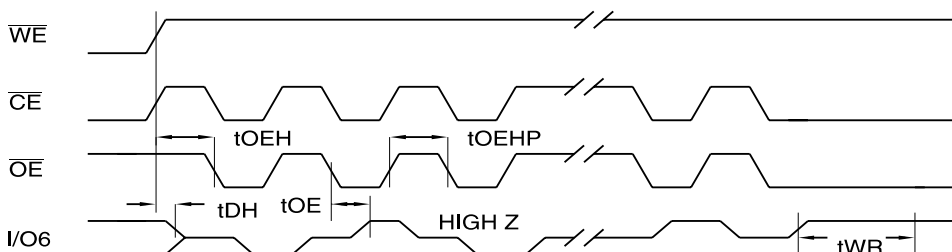


Toggle Bit Characteristics⁽¹⁾

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|--|-----|-----|-----|-------|
| t_{DH} | Data Hold Time | 10 | | | ns |
| $t_{OE\overline{H}}$ | \overline{OE} Hold Time | 10 | | | ns |
| t_{OE} | \overline{OE} to Output Delay ⁽²⁾ | | | | ns |
| t_{OEHP} | \overline{OE} High Pulse | 50 | | | ns |
| t_{WR} | Write Recovery Time | 0 | | | ns |

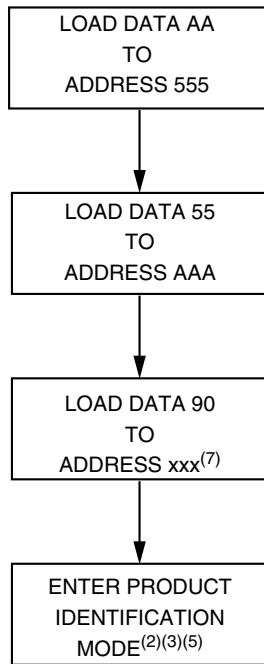
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in page 26.

Toggle Bit Waveforms⁽¹⁾⁽²⁾⁽³⁾

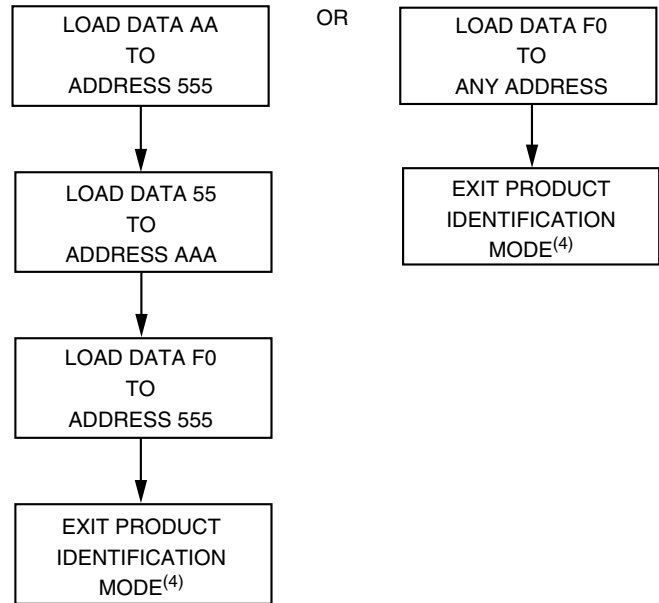


Notes: 1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.
The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry⁽¹⁾



Software Product Identification Exit⁽¹⁾⁽⁶⁾



- Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A11 - A0 (Hex); A12 - A21 (Don't Care).
 2. A1 - A21 = V_{IL} .
Manufacturer Code is read for A0 = V_{IL} ;
Device Code is read for A0 = V_{IH} .
 3. The device does not remain in identification mode if powered down.
 4. The device returns to standard operation mode.
 5. Manufacturer Code: 001FH
Device Code: 00D4H - AT49BN3204; 00D7H - AT49BN3204T;
00D6H - AT49BN6416/BV641; 00D2H - AT49BN6416T/BV641T.
 6. Either one of the Product ID Exit commands can be used.
 7. For the AT49BN3204:
xxx = 00X555 Status Read from Plane A
xxx = 05X555 Status Read from Plane B
xxx = 11X555 Status Read from Plane C
xxx = 1FX555 Status Read from Plane D

For the AT49BN6408:

xxx = 00X555 Status Read from Plane A
xxx = 1XX555 Status Read from Plane B
xxx = 2XX555 Status Read from Plane C
xxx = 38X555 Status Read from Plane D

For the AT49BN6416/BV641:

xxx = 0XX555 Status Read from Plane A
xxx = 1XX555 Status Read from Plane B
xxx = 2XX555 Status Read from Plane C
xxx = 3XX555 Status Read from Plane D

For the AT49BN3204T:

xxx = 1FX555 Status Read from Plane A
xxx = 0XX555 Status Read from Plane B
xxx = 17X555 Status Read from Plane C
xxx = 00X555 Status Read from Plane D

For the AT49BN6408T:

xxx = 38X555 Status Read from Plane A
xxx = 2XX555 Status Read from Plane B
xxx = 1XX555 Status Read from Plane C
xxx = 00X555 Status Read from Plane D

For the AT49BN6416T/BV641T:

xxx = 3XX555 Status Read from Plane A
xxx = 2XX555 Status Read from Plane B
xxx = 1XX555 Status Read from Plane C
xxx = 0XX555 Status Read from Plane D

If a read status has been entered for a plane, any read from this plane will be a status read while any read of another plane will be a memory read, either random or burst. Program or erase operations cannot be performed while one of the planes is in the read status mode.

Table 5. Common Flash Interface Definition for AT49BN/BV64xx(T)/3204(T)

| Address | AT49BN3204(T) | AT49BN/BV64xx(T) | Comments |
|---------|---------------|------------------|--|
| 10h | 0051h | 0051h | “Q” |
| 11h | 0052h | 0052h | “R” |
| 12h | 0059h | 0059h | “Y” |
| 13h | 0002h | 0002h | |
| 14h | 0000h | 0000h | |
| 15h | 0041h | 0041h | |
| 16h | 0000h | 0000h | |
| 17h | 0000h | 0000h | |
| 18h | 0000h | 0000h | |
| 19h | 0000h | 0000h | |
| 1Ah | 0000h | 0000h | |
| 1Bh | 0027h | 0027h | VCC min write/erase |
| 1Ch | 0031h | 0031h | VCC max write/erase |
| 1Dh | 00B5h | 00B5h | VPP min voltage |
| 1Eh | 00C5h | 00C5h | VPP max voltage |
| 1Fh | 0004h | 0004h | Typ word write – 16 μ s |
| 20h | 0000h | 0000h | |
| 21h | 0009h | 0009h | Typ block erase – 500 ms |
| 22h | 000Fh | 0010h | Typ chip erase, 32M bytes – 32,300 ms, 64M bytes – 64,300 ms |
| 23h | 0004h | 0004h | Max word write/typ time |
| 24h | 0000h | 0000h | n/a |
| 25h | 0003h | 0003h | Max block erase/typ block erase |
| 26h | 0003h | 0003h | Max chip erase/ typ chip erase |
| 27h | 0016h | 0017h | Device size |
| 28h | 0001h | 0001h | x16 device |
| 29h | 0000h | 0000h | x16 device |
| 2Ah | 0000h | 0000h | Multiple byte write not supported |
| 2Bh | 0000h | 0000h | Multiple byte write not supported |
| 2Ch | 0002h | 0002h | 2 regions, x = 2 |
| 2Dh | 003Eh | 007Eh | 64K bytes, 32M – Y = 62, 64M – Y = 126 |
| 2Eh | 0000h | 0000h | 64K bytes, 32M – Y = 62, 64M – Y = 126 |
| 2Fh | 0000h | 0000h | 64K bytes, Z = 256 |
| 30h | 0001h | 0001h | 64K bytes, Z = 256 |
| 31h | 0007h | 0007h | 8K bytes, Y = 7 |
| 32h | 0000h | 0000h | 8K bytes, Y = 7 |
| 33h | 0020h | 0020h | 8K bytes, Z = 32 |
| 34h | 0000h | 0000h | 8K bytes, Z = 32 |

Table 5. Common Flash Interface Definition for AT49BN/BV64xx(T)/3204(T) (Continued)

| Address | AT49BN3204(T) | AT49BN/BV64xx(T) | Comments |
|---------------------------------------|--|--|---|
| VENDOR SPECIFIC EXTENDED QUERY | | | |
| 41h | 0050h | 0050h | "P" |
| 42h | 0052h | 0052h | "R" |
| 43h | 0049h | 0049h | "I" |
| 44h | 0031h | 0031h | Major version number, ASCII |
| 45h | 0030h | 0030h | Minor version number, ASCII |
| 46h | 00BFh | 00BFh | Bit 0 – chip erase supported, 0 – no, 1 – yes Bit 1 – erase suspend supported, 0 – no, 1 – yes Bit 2 – program suspend supported, 0 – no, 1 – yes Bit 3 – simultaneous operations supported, 0 – no, 1 – yes Bit 4 – burst mode read supported, 0 – no, 1 – yes Bit 5 – page mode read supported, 0 – no, 1 – yes Bit 6 – queued erase supported, 0 – no, 1 – yes Bit 7 – protection bits supported, 0 – no, 1 – yes |
| 47h | 0000h AT49BN3204T or 0001h AT49BN3204 | 0000h AT49BN/BV64xxT or 0001h AT49BN/BV64xx | Bit 8 – top ("0") or bottom ("1") boot block device undefined bits are "0" |
| 48h | 0007h | 0007h | Bit 0 – 4 word linear burst with wrap around, 0 – no, 1 – yes Bit 1 – 8 word linear burst with wrap around, 0 – no, 1 – yes Bit 2 – continuous burst undefined bits are "0" |
| 49h | 0003h | 0003h | Bit 0 – 4 word page, 0 – no, 1 – yes Bit 1 – 8 word page, 0 – no, 1 – yes Undefined bits are "0" |
| 4Ah | 0080h | 0080h | Location of protection register lock byte, the section's first byte |
| 4Bh | 0003h | 0003h | # of bytes in the factory prog section of prot register – 2*n |
| 4Ch | 0003h | 0003h | # of bytes in the user prog section of prot register – 2*n |

AT49BV641(T) Ordering Information

| t _{ACC} (ns) | I _{CC} (mA) | | Ordering Code | Package | Operation Range |
|--------------------------|----------------------|---------|-----------------|---------|------------------------------|
| | Active | Standby | | | |
| 70 | 30 | 0.01 | AT49BV641-70TI | 48T | Industrial (-40° to 85°C) |
| 85 | 30 | 0.01 | AT49BV641-85TI | 48T | Industrial (-40° to 85°C) |
| 70 | 30 | 0.01 | AT49BV641T-70TI | 48T | Industrial (-40° to 85°C) |
| 85 | 30 | 0.01 | AT49BV641T-85TI | 48T | Industrial (-40° to 85°C) |

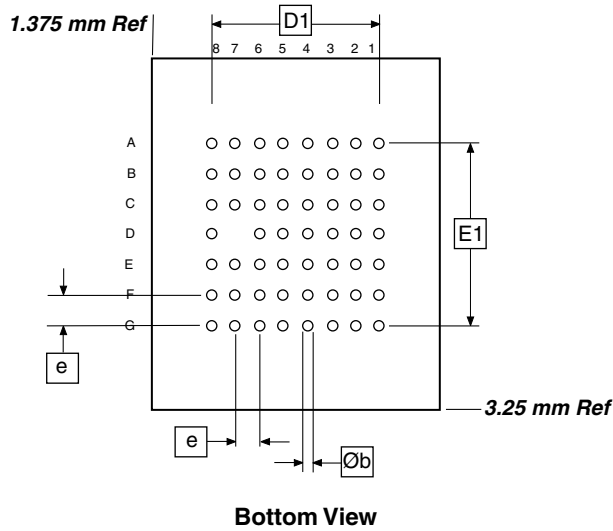
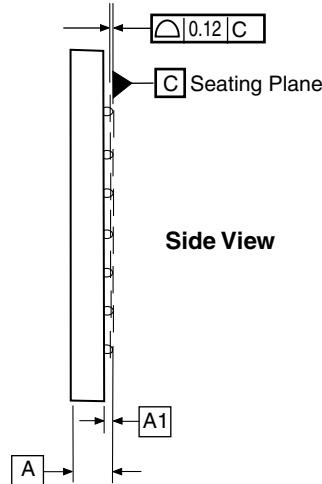
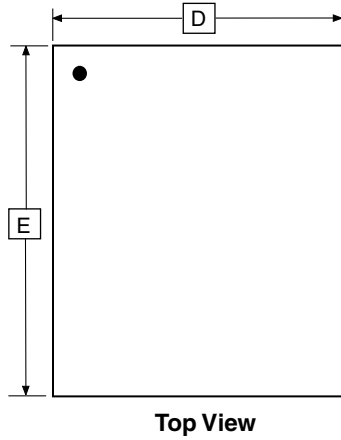
AT49BN6408(T)/6416(T) Ordering Information

| t _{ACC} (ns) | I _{CC} (mA) | | Ordering Code | Package | Operation Range |
|--------------------------|----------------------|---------|------------------|---------|------------------------------|
| | Active | Standby | | | |
| 70 | 30 | 0.01 | AT49BV6408-70CI | 55C1 | Industrial (-40° to 85°C) |
| 85 | 30 | 0.01 | AT49BV6408-85CI | 55C1 | Industrial (-40° to 85°C) |
| 70 | 30 | 0.01 | AT49BV6408T-70CI | 55C1 | Industrial (-40° to 85°C) |
| 85 | 30 | 0.01 | AT49BV6408T-85CI | 55C1 | Industrial (-40° to 85°C) |
| 70 | 30 | 0.01 | AT49BV6416-70CI | 55C1 | Industrial (-40° to 85°C) |
| 85 | 30 | 0.01 | AT49BV6416-85CI | 55C1 | Industrial (-40° to 85°C) |
| 70 | 30 | 0.01 | AT49BV6416T-70CI | 55C1 | Industrial (-40° to 85°C) |
| 85 | 30 | 0.01 | AT49BV6416T-85CI | 55C1 | Industrial (-40° to 85°C) |

| Package Type | |
|--------------|---|
| 55C1 | 55-ball, Plastic Chip-size Ball Grid Array Package (CBGA) |
| 48T | 48-lead, Plastic Thin Small Outline Package (TSOP) |

Packaging Information – AT49BN6408(T)/6416(T)

55C1 – CBGA



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-------|-------|------|
| A | – | – | 1.00 | |
| A1 | 0.23 | – | – | |
| D | 7.90 | 8.00 | 8.10 | |
| D1 | 5.25 TYP | | | |
| E | 10.90 | 11.00 | 11.10 | |
| E1 | 4.50 TYP | | | |
| e | 0.75 TYP | | | |
| Øb | 0.35 TYP | | | |

3/20/02



2325 Orchard Parkway
San Jose, CA 95131

TITLE

55C1, 55-ball (8 x 7 Array), 8 x 11 x 1.0 mm Body, 0.75 mm Ball Pitch
Ceramic Ball Grid Array Package (CBGA)

DRAWING NO.

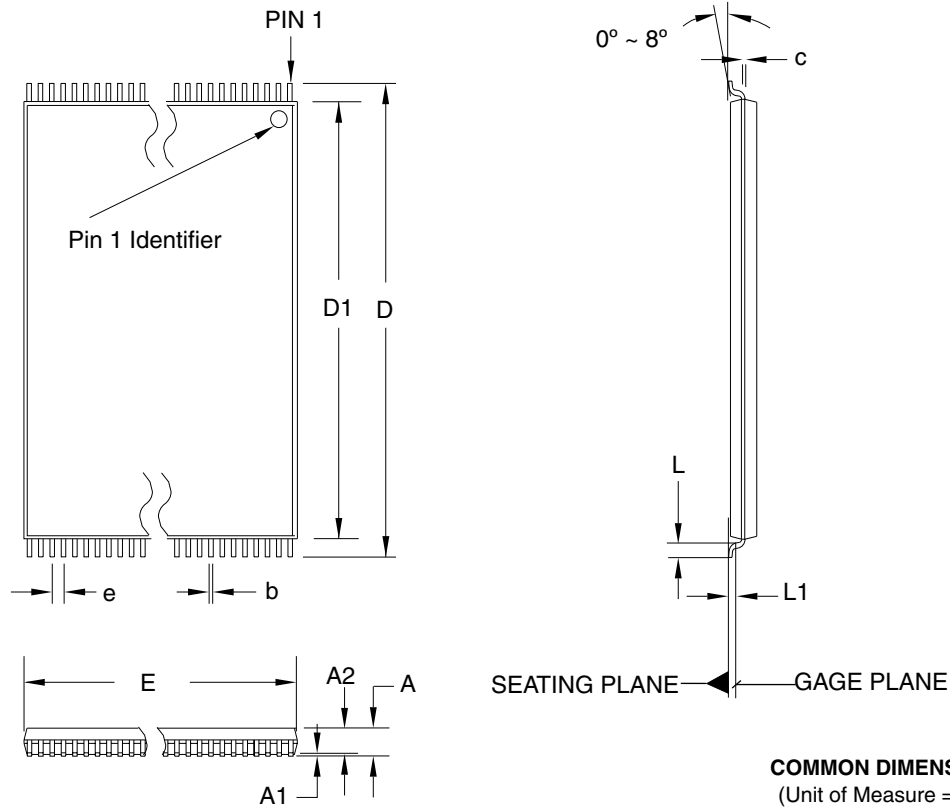
55C1

REV.

A

Packaging Information – AT49BV641(T)

48T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------------|-------|-------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 19.80 | 20.00 | 20.20 | |
| D1 | 18.30 | 18.40 | 18.50 | Note 2 |
| E | 11.90 | 12.00 | 12.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation DD.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

48T, 48-lead (12 x 20 mm Package) Plastic Thin Small Outline
Package, Type I (TSOP)

DRAWING NO.

48T

REV.

B





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