# Application Note 53

## Implementing an RC5051 DC-DC Converter on Pentium® II Motherboards

## Introduction

This document describes how to implement a switching voltage regulator using an RC5051 high speed controller, a power inductor, a Schottky diode, appropriate capacitors, and external power MOSFETs. This regulator forms a step down DC-DC converter that can deliver up to 14.5A of continuous load current at voltages ranging from 1.3V to 3.5V. A specific application circuit, design considerations, component selection, PCB layout guidelines, and performance evaluations are covered in detail.

In the past 10 years, microprocessors have evolved at such a rate that a modern chip can rival the computing power of a mainframe computer. Such evolution has been possible because of the increasing numbers of transistors that processors integrate. Pentium CPUs, for example, integrate well over 5 million transistors on a single piece of silicon.

To integrate so many transistors on a piece of silicon, their physical geometry has been reduced to the sub-micron level. As a result of each geometry reduction, the corresponding operational voltage for each transistor has also been reduced. This changing CPU voltage demands the design of a programmable power supply–a design that is not completely re-engineered with every change in CPU voltage.

The voltage range of the CPU has shown a downwards trend for the past 5 years: from 3.3V for the Pentium, to 3.1V for the Pentium Pro, to 2.8V for the Klamath, and to 2.0V for the Deschutes processors. With this trend in mind, Fairchild Semiconductor has designed the RC5051 controller. This controller integrates the necessary programmability to address the changing power supply requirements of lower voltage CPUs.

Previous generations of DC-DC converter controllers were designed with fixed output voltages adjustable only by means of a set of external resistors. In a high volume production environment (such as with personal computers), however, a CPU voltage change would require a CPU board redesign to accommodate the new voltage requirement. The 5-bit DAC in the RC5051 reads the voltage ID code that is programmed into modern processors and provides the appropriate CPU voltage. In this manner, the PC board does not have to be re-designed each time the CPU voltage changes. The CPU can thus automatically configure its own required supply voltage.

## Intel Pentium II Processor Power Requirements

Refer to Intel's AP-587 Application Note, Slot 1 Processor Power Distribution Guidelines, May 1997 (order number 243332-001), as a basic reference.

### Input Voltages

Available inputs are +12V ±5% and +5V ±5%. Either one or both of these inputs can be used by the DC-DC converter. The input voltage requirements for Fairchild's RC5051 DC-DC converter are listed in Table 1. See below for detailed information on how to apply these.

**Table 1. Input Voltage Requirements**

| Part # | Vcc for IC | MOSFET Drain |
|---|---|---|
| RC5051 | +5V ±5% | +5V ±5% or 12V ±5% |

### Pentium II DC Power Requirements

Refer to Table 2, Intel Pentium II Processor Power Specifications. For standard motherboard designs , the on-board DC-DC converter must supply a minimum of 14.2A at 2.8V for Klamath or 2.0V for Deschutes. For a Deschutes Flexible Motherboard design, the on-board DC-DC converter must supply 18.9A.

### DC Voltage Regulation

As indicated in Table 2, the voltage level supplied to the CPU must be within ±3% of its nominal setting. Voltage regulation limits must include:

- Output load ranges specified in Table 2
- Output ripple/noise
- DC output initial voltage set point
- Temperature and warm up drift (Ambient +0°C to +70°C at full load with a maximum rate of change of 5°C per 10 minutes but no more than 10°C per hour)
- Output load transient with:
- Slew rate >30A/µs at converter pins Range: 0.3A - $I_{CCP}$ Max (as defined in Table 2).

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**Table 2. Intel Pentium II® Processor Power Specifications**

| CPU Model, Features | Voltage Specification, $V_{CC\ CORE}$ (VDC) | Maximum Current, $I_{CC\ CORE}$ (A) |
|---|---|---|
| Klamath<br>233MHz<br>266MHz<br>300MHz | 2.8V +100mV/-60mV | <br>11.8<br>12.7<br>14.2 |
| Deschutes<br>266MHz<br>300MHz<br>333MHz<br>350MHz<br>400MHz<br>450MHz<br>500MHz | <br>2.0V +100mV/-60mV<br>2.0V +100mV/-60mV<br>2.0V +100mV/-60mV<br>2.0V +/-60mV<br>2.0V +/-60mV<br>2.0V +/-60mV<br>2.0V +/-60mV | <br>8.5<br>9.6<br>10.6<br>11.1<br>12.1<br>14.2<br>16.0 |
| Deschutes Flexible Motherboard | 2.0V +/-60mV | 18.9 |

**NOTES:**
1. Maximum power values are measured at typical $V_{CCP}$ to take into account the thermal time constant of the CPU package.
2. Flexible motherboard specifications are recommendations only. Actual specifications are subject to change.

## Output Ripple and Noise

Ripple and noise are defined as periodic or random signals over the frequency band of 0–20MHz at the output pins. Output ripple and noise must be consistent with voltage requirements throughout the full load range and under all specified input voltage conditions.

## Efficiency

The efficiency of the DC-DC converter must be greater than 80% at maximum output current and greater than 40% at low current draw.

## Processor Voltage Identification

There are five Voltage Identification Pins, VID4-VID0, on the Pentium II processor package which can be used to support automatic selection of the power supply voltage. These pins are internally unconnected or are shorted to ground ($V_{SS}$ ). The logic status of the VID pins defines the voltage required by the processor. In order to address future low voltage microprocessors, the RC5051 includes a VID4 input bit to extend the output voltage range as low as 1.3V. The output voltage programming codes are presented in Table 3. A ‘1’ refers to an open pin and a ‘0’ refers to a short to ground.

**Table 3. Output Voltage Programming Codes**

| VID4 | VID3 | VID2 | VID1 | VID0 | $V_{OUT}$ to CPU |
|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1.30V |
| 0 | 1 | 1 | 1 | 0 | 1.35V |
| 0 | 1 | 1 | 0 | 1 | 1.40V |
| 0 | 1 | 1 | 0 | 0 | 1.45V |
| 0 | 1 | 0 | 1 | 1 | 1.50V |
| 0 | 1 | 0 | 1 | 0 | 1.55V |
| 0 | 1 | 0 | 0 | 1 | 1.60V |

**Table 3. Output Voltage Programming Codes** (continued)

| VID4 | VID3 | VID2 | VID1 | VID0 | $V_{OUT}$ to CPU |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1.65V |
| 0 | 0 | 1 | 1 | 1 | 1.70V |
| 0 | 0 | 1 | 1 | 0 | 1.75V |
| 0 | 0 | 1 | 0 | 1 | 1.80V |
| 0 | 0 | 1 | 0 | 0 | 1.85V |
| 0 | 0 | 0 | 1 | 1 | 1.90V |
| 0 | 0 | 0 | 1 | 0 | 1.95V |
| 0 | 0 | 0 | 0 | 1 | 2.00V |
| 0 | 0 | 0 | 0 | 0 | 2.05V |
| 1 | 1 | 1 | 1 | 1 | No CPU |
| 1 | 1 | 1 | 1 | 0 | 2.1V |
| 1 | 1 | 1 | 0 | 1 | 2.2V |
| 1 | 1 | 1 | 0 | 0 | 2.3V |
| 1 | 1 | 0 | 1 | 1 | 2.4V |
| 1 | 1 | 0 | 1 | 0 | 2.5V |
| 1 | 1 | 0 | 0 | 1 | 2.6V |
| 1 | 1 | 0 | 0 | 0 | 2.7V |
| 1 | 0 | 1 | 1 | 1 | 2.8V |
| 1 | 0 | 1 | 1 | 0 | 2.9V |
| 1 | 0 | 1 | 0 | 1 | 3.0V |
| 1 | 0 | 1 | 0 | 0 | 3.1V |
| 1 | 0 | 0 | 1 | 1 | 3.2V |
| 1 | 0 | 0 | 1 | 0 | 3.3V |
| 1 | 0 | 0 | 0 | 1 | 3.4V |
| 1 | 0 | 0 | 0 | 0 | 3.5V |

Note:
1. 0 = processor pin is tied to GND
   1 = processor pin is open.

### I/O Controls

In addition to the Voltage Identification, there are several signals that control the DC-DC converter or provide feedback from the DC-DC converter to the CPU. They are Power-Good (PWRGD), and Output Enable (OUTEN). These signals will be discussed later.

## RC5051 Description

### Simple Step-Down Converter

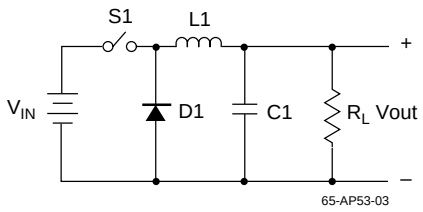



**Figure 1. Simple Buck DC-DC Converter**

For the purpose of understanding a buck converter, Figure 1 illustrates a step-down DC-DC converter with no feedback control. The operation of the basic step-down converter is the basis for the design equations for the RC5051. Referring to Figure 1, the basic operation begins by closing the switch S1. When S1 is closed, the input voltage $V_{IN}$ is applied to inductor L1. The current flowing in this inductor increases, and the increase is given by the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})T_{ON}}{L1}$$

where $T_{ON}$ is the time S1 is closed (the duty cycle is $T_{ON} / T_S$, with $T_S$ the switching period). When S1 opens, the diode D1 conducts the inductor current and the output current is delivered to the load; the inductor current decrease is given by:

$$\Delta I_L = \frac{V_{OUT}(T_S - T_{ON})}{L1}$$

where $(T_S - T_{ON})$ is the time during which S1 is open.

By solving these two equations, we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_{OUT} = V_{IN}\frac{T_{ON}}{T_S}$$

In order to obtain a more accurate approximation for $V_{OUT}$, we must also include the forward voltage $V_D$ across diode D1 and the voltage across the switch , $V_{SW}$. After taking into account these factors, the new relationship becomes:

$$V_{OUT} = (V_{IN} + V_D - V_{SW})\frac{T_{ON}}{T_S} - V_D$$

where $V_{SW}$ = is the voltage across the MOSFET in the on state, $I_L * R_{DS,ON}$.

### The RC5051 Controller

The RC5051 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, this device can be configured to deliver more than 14.5A of output current. The RC5051 utilizes both current-mode and voltage-mode PWM control to create an integrated step-down voltage regulator.

### Main Control Loop

Refer to the RC5051 Block Diagram illustrated in Figure 2. The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital control block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The voltage control path amplifies the difference between the VFB signal and the voltage reference and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the point at which the current limit comparator disables the output drive signals to the external power MOSFETs.

The digital control block takes the comparator inputs and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These pins control the external power MOSFETs. The digital section utilizes high speed Schottky transistor logic, allowing the RC5051 to operate at clock speeds as high as 1MHz.

### High Current Output Drivers

The RC5051 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. Each driver is capable of delivering 1A of current in less than 100ns. Each driver's power and ground are separated from the chip's power and ground for additional switching noise immunity.

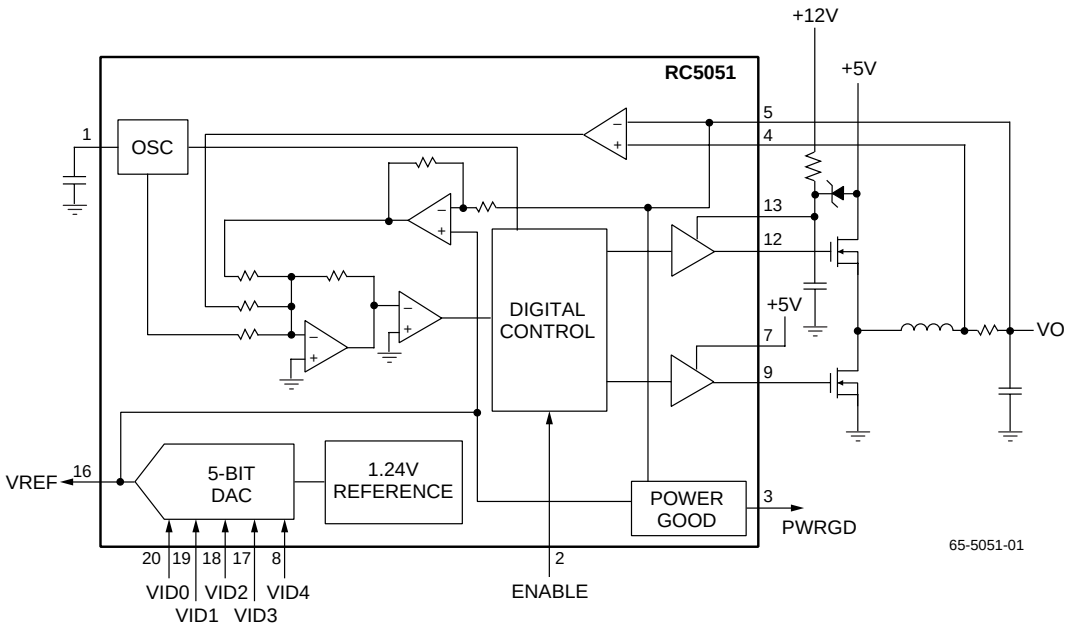



**Figure 2. RC5051 Block Diagram**

The HIDRV driver has a power supply, VCCQP, supplied from a 12V source as illustrated in Figure 2. The resulting voltage is sufficient to provide the gate to source voltage to the external MOSFET that is required to achieve a low $R_{DS,ON}$. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage, and its $V_{CCP}$ power pin can be tied to VCC.

## Internal Voltage Reference

The reference included in the RC5051 is a precision band-gap voltage reference. The internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Added to the reference input is the resulting output from an integrated 5-bit DAC–provided in accordance with the Pentium II specification guidelines. These guidelines require the DC-DC converter output to be directly programmable via a 5-bit voltage identification (VID) code. This code scales the reference voltage from 2.0V (no CPU) to 3.5V in 100mV increments, and between 1.3V and 2.05V in 50mV increments. For guaranteed stable operation under all operating conditions, 0.1µF of decoupling capacitance should be connected to the VREF pin. No load should be imposed on this pin.

## Power Good (PWRGD)

The RC5051 Power Good function is designed in accordance with the Pentium II DC-DC converter specification to provide a constant voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU when the power supply voltage differs more than ±12% from nominal. The Power Good flag provides no other control function to the RC5051.

## Output Enable (OUTEN)

The DC-DC converter accepts an open collector signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

## Over-Voltage Protection

The RC5051 constantly monitors the output voltage for protection against over voltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an over-voltage condition is assumed and the chip disables the output drive signal to the external MOSFETs.

## Over-current Protection

A current sense methodology is implemented to disable the output drive signal to the MOSFETs when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When the voltage developed across the sense resistor exceeds the comparator threshold voltage, the chip reduces the output drive signal to the MOSFETs.

The DC-DC converter returns to normal operation after the fault has been removed, for either an over-voltage or an over-current condition.

## Oscillator

The RC5051 oscillator section uses a fixed current capacitor charging configuration. An external capacitor ($C_{EXT}$) is used to preset the oscillator frequency between 80KHz and 1MHz. This scheme allows maximum flexibility in choosing external components.

In general, a higher operating frequency decreases the peak ripple current flowing in the output inductor, thus allowing the use of a smaller inductor value. operation at higher frequencies also decreases the amount of energy storage that must be provided by the bulk output capacitors during load transients.

Unfortunately, the efficiency losses due to switching of the MOSFETs increase as the operating frequency is increased. Thus, efficiency is optimized at lower operating frequencies.

An operating frequency of 300 kHz was chosen in this Application Note to optimize efficiency while maintaining excellent regulation and transient performance under all operating conditions.

## Design Considerations and Component Selection

Figure 3 illustrates a synchronous application using the RC5051.

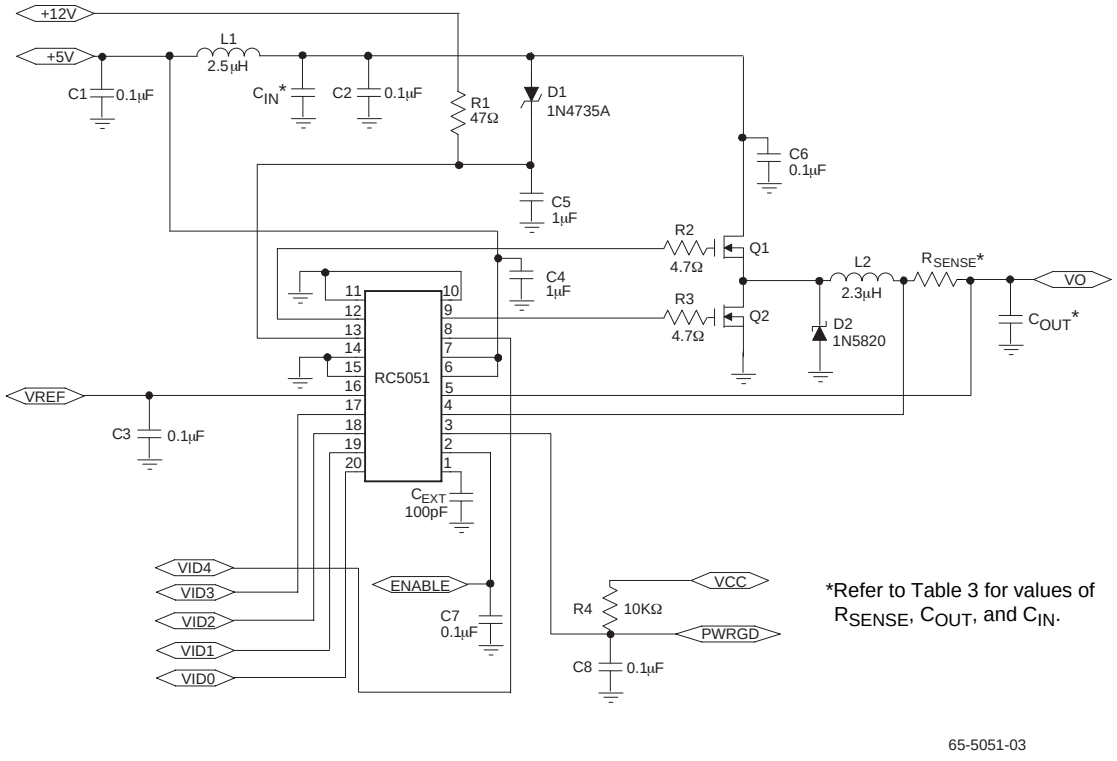



**Figure 3. Synchronous DC-DC Converter Application Schematic Using the RC5051**

**Table 4. RC5051 Application Bill of Materials for Intel Pentium II Processors**

| Reference | Manufacturer's Part # | Quantity | Description | Requirements/Comments |
|---|---|---|---|---|
| C1-3, C6-8 | | 6 | 100nF, 50V Capacitor | |
| C4-5 | | 2 | 1μF 16V Capacitor | |
| $C_{ext}$ | | 1 | 100pF Capacitor | 5%, C0G |
| $C_{IN}$ | Sanyo 10MV1200GX | * | 1200μF, 10V electrolytic | $I_{RMS}$ = 2A *See Table 5 |
| $C_{OUT}$ | Sanyo 6MV1500GX | * | 1500μF, 6.3V electrolytic | ESR < 44mΩ *See Table 5 |
| D1 | Motorola 1N4735A | 1 | 6.2V Zener Diode | 5% |
| D2 | Motorola IN5820 | 1 | 3A Schottky Diode | |
| L1 | | 1 | 2.5μH Inductor | DCR < 6mΩ[1] |
| L2 | Elytone YT-6542 | 1 | 1.3μH Inductor | DCR < 3mΩ |
| Q1-2 | Fairchild FDP6030L or FDB6030L | 2 | N-channel MOSFET | $R_{DS, ON}$ = 20mW @ $V_{GS}$ = 4.5V[2] |
| R1 | | 1 | 47Ω | 1/10W |
| R2-3 | | 2 | 4.7Ω | 1/10W |
| $R_{SENSE}$ | Fairchild RC10-XX | 1 | CuNi Alloy Wire Resistor | *See Table 5 |
| U1 | Fairchild RC5051M | 1 | DC/DC Controller | |

**Notes:**

1. Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel dI/dt requirements. If used, it must be sized to avoid saturation at maximum input current. L1 may be omitted if desired.
2. For 14.2A designs using the FDP6030L MOSFETs, heatsinks with thermal resistance $\Theta_{SA}$ <20°C/W should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletin AB-8.

**Table 5. Recommended Values for CPU-based Applications**

| Application | Output Current | $C_{IN}$ | $C_{OUT}$ | $C_{OUT}$ Maximum ESR | $R_{SENSE}$ |
|---|---|---|---|---|---|
| 300MHz AMD K6 Motherboard | 13A | 3 x 1200μF, 10V Sanyo 10MV1200GX | 7 x 1500μF, 6.3V Sanyo 6MV1500GX | 6.1mΩ | 5.8mΩ |
| 300MHz Intel Pentium II Klamath Motherboard | 14.2A | 3 x 1200μF, 10V Sanyo 10MV1200GX | 7 x 1500μF, 6.3V Sanyo 6MV1500GX | 6.8mΩ | 5.2mΩ |
| 300MHz Intel Pentium II Deschutes Motherboard | 12.6A | 3 x 1200μF, 10V Sanyo 10MV1200GX | 7 x 1500μF, 6.3V Sanyo 6MV1500GX | 5.3mΩ | 5.8mΩ |

# MOSFET Selection Cosiderations

## MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 40\ m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} \leq 4.5V$
- Power package with low Thermal Resistance
- Drain current rating of 20A minimum
- Drain-Source voltage > 15V.

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. It determines the power dissipation within the MOSFET and, therefore, significantly affects the efficiency of the DC-DC converter. Table 6 is a selection table for MOSFETs.

### Table 6. MOSFET Selection Table

| Manufacturer and Part # | Conditions | | $R_{DS,ON}$ (mΩ) | | Package | Thermal Resistance (°C/W) |
|---|---|---|---|---|---|---|
| | | | Typ. | Max. | | |
| Fairchild FDP6030L | $V_{GS}$ = 4.5V, $I_D$ = 21A | $T_J$ = 25°C | 15 | 20 | TO-220 | $\Theta_{JA}$ = 62.5 |
| Fairchild FDB6030L | $V_{GS}$ = 4.5V, $I_D$ = 21A | $T_J$ = 25°C | 15 | 20 | $D^2$-PAK | $\Theta_{JA}$ = 62.5 |
| Fairchild FDP603AL | $V_{GS}$ = 4.5V, $I_D$ = 10A | $T_J$ = 25°C | 30 | 36 | TO-220 | $\Theta_{JA}$ = 62.5 |
| Fairchild FDB603AL | $V_{GS}$ = 4.5V, $I_D$ = 10A | $T_J$ = 25°C | 30 | 36 | $D^2$-PAK | $\Theta_{JA}$ = 62.5 |
| Fairchild FDP7030L | $V_{GS}$ = 5V, $I_D$ = 40A | $T_J$ = 25°C | 9 | 10 | TO-220 | $\Theta_{JA}$ = 62.5 |
| Fairchild FDB7030L | $V_{GS}$ = 5V, $I_D$ = 40A | $T_J$ = 25°C | 9 | 10 | $D^2$-PAK | $\Theta_{JA}$ = 62.5 |
| IR IRL2203N | $V_{GS}$ = 4.5V, $I_D$ = 50A | $T_J$ = 25°C | | 10 | TO-220 | $\Theta_{JA}$ = 62 |
| IR IRL2203S | $V_{GS}$ = 4.5V, $I_D$ = 50A | $T_J$ = 25°C | | 10 | $D^2$-PAK0 | $\Theta_{JA}$ = 40 |

**Two MOSFETs in parallel.**

If output current is high, We recommend two MOSFETs used in parallel instead of one single MOSFET. The following significant advantages are realized using two MOSFETs in parallel:

- **Significant reduction of Power dissipation**.
  Example: RC5051 with Maximum output current of 14A at 2.8V with one MOSFET on the high side:

  $P_{MOSFET} = (I^2 R_{DS,ON})(\text{Duty Cycle}) =$
  $(14A)^2 (0.050\Omega)(2.8V / 5V) = 5.5W$

  With two MOSFETs in parallel:

  $P_{MOSFET} = (I^2 R_{DS,ON})(\text{Duty Cycle}) =$
  $(14A/2)^2 (0.037\Omega) (2.8V / 5V) = 1.0W/FET$

  ***Note:** $R_{DS,ON}$ increases with temperature. Assume $R_{DS,ON}$ = 25mΩ at 25°C. $R_{DS,ON}$ can easily increase to 50mΩ at high temperature when using a single MOSFET. When using two MOSFETs in parallel, the temperature effects should not cause the $R_{DS,ON}$ to rise as much.

- **Smaller heat sink required.**
  With power dissipation down to around one watt, considerably less heat sink is required.

- **Reliability.**
  With thermal management under control, this DC-DC converter is able to deliver load currents up to 14.5A with no performance or reliability concerns.

- **MOSFET Gate Bias.**
  As already discussed, the low-side MOSFET on the RC5051 needs only 5V for its gate drive supply. The high-side MOSFET can be biased by one of two methods: Charge Pump or 12V Gate Bias.

- **Method 1. Charge pump (or Bootstrap) method.**
  Figure 4 displays the use of a charge pump to provide gate bias to the high-side MOSFET with the RC5051. Capacitor CP is the charge pump deployed to boost the voltage of the RC5051 output driver. When the MOSFET switches off, the source of the MOSFET is at approximately 0V. VCCQP is charged through the Schottky diode D1 to approximately 4.5V. Thus, the capacitor CP is charged to approximately 4.5V. When the MOSFET turns on, the source of the MOSFET voltage is equal to 5V. The capacitor voltage follows, and hence provides a voltage at VCCQP equal to approximately 10V. The Schottky diode D1 is required to provide the charge path when the MOSFET is off, and reverses bias when the VCCQP goes to 10V. The charge pump capacitor, CP, needs to be a high Q, high frequency capacitor. A 1µF ceramic capacitor is recommended here.

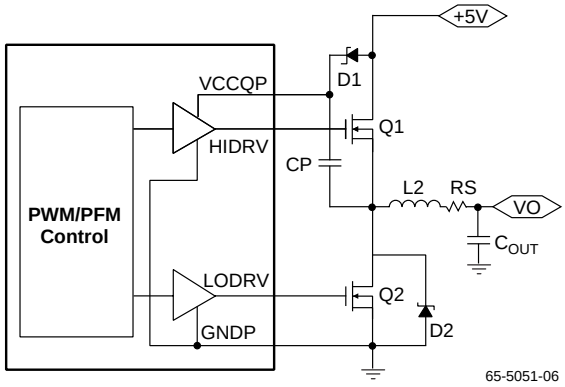



**Figure 4. Charge Pump Configuration**

- **Method 2. 12V Gate Bias.**
  Figure 5 illustrates how a 12V source can be used to bias the VCCQP. A 47Ω resistor is used to limit the transient current into the VCCQP pin and a 1µF capacitor filter is used to filter the VCCQP supply. This method provides a higher gate bias voltage ($V_{GS}$) to the MOSFET than the charge-pump method does, and therefore reduces the $R_{DS,ON}$ of the MOSFET and thus reduces the power loss due to the MOSFET. Figure 6 shows how $R_{DS,ON}$ reduces dramatically with $V_{GS}$ increases. A 6.2V Zener diode (D1) is placed from VCCQP to 5V to clamp the voltage at VCCQP to a maximum of 12V and ensure that the absolute maximum voltage of the IC will not be exceeded.

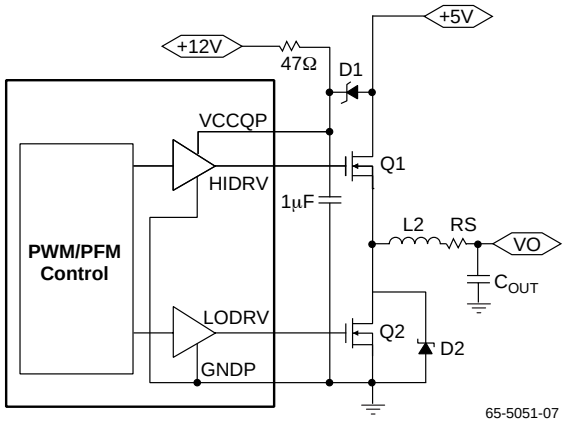



**Figure 5. 12V Gate Bias Configuration**

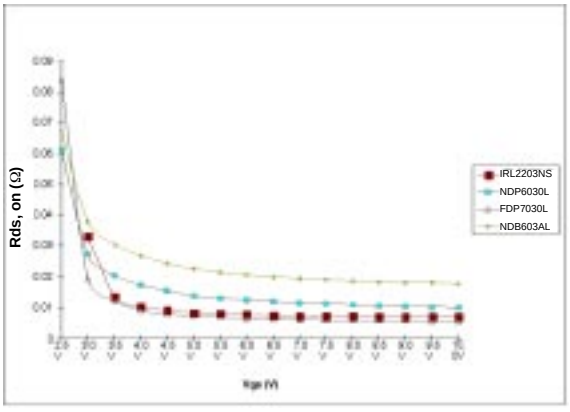



**Figure 6. $R_{DS,ON}$ vs. $V_{GS}$ for Selected MOSFETs**

## Converter Efficiency

Losses due to parasitic resistance in the switches, coil, and sense resistor dominate at high load-current level. The major loss mechanisms under heavy loads, in typical order of importance, are:

- MOSFET $I^2R$ losses
- Transition losses
- Sense Resistor losses
- Input Capacitor losses
- Coil Losses
- Losses due to the operating supply current of the IC.
- Diode-conduction losses
- Gate-charge losses

### Formulae for Calculation of Converter Efficiency

$$\text{Efficiency} = \frac{P_{OUT}}{p_{IN}} = \frac{V_{OUT}I_{OUT}}{V_{OUT}I_{OUT} + P_{LOSS}}$$

$$P_{LOSS} = P_{RDS} + (P_{RISE} + P_{FALL}) + P_{INDUCTOR} + P_{SENSE} + P_{GATE} + P_{DIODE} + P_{CAPS} + P_{IC}$$

$$P_{RDS} = I_{OUT}^2 R_{DS,ON} DC \text{ for the high-side MOSFET}$$

$$P_{RDS} = I_{OUT}^2 R_{DS,ON}(1 - DC) \text{ for the low-side MOSFET}$$

$$P_{RISE} + P_{FALL} = \frac{V_{IN}I_{OUT}t_{RISE}F_S}{2} + \frac{V_{IN}I_{OUT}t_{FALL}F_S}{2} \text{ for the high-side MOSFET}$$

$$P_{RISE} + P_{FALL} = \frac{V_f I_{OUT}t_{RISE}F_S}{2} + \frac{V_f I_{OUT}t_{FALL}F_S}{2} \text{ for the low-side MOSFET}$$

$$P_{INDUCTOR} = I_{OUT}^2 R_{INDUCTOR}$$

$$P_{SENSE} = I_{OUT}^2 R_{SENSE}$$

$$P_{GATE} = CV^2F_S \text{ for each MOSFET}$$

$$P_{DIODE} = I_{OUT}V_F T_{DT} F_S \text{ , with } T_{DT} \text{ the deadtime}$$

$$P_{CAPS} = ESR \times I_{OUT}^2 \times DC \times (1 - DC)$$

$$P_{IC} = 25mA * V_{CC}$$

### Example Efficiency Calculation

As an example, the efficiency of a synchronous 14A converter based on the RC5051 will be calculated. The converter produces 2.8V output from a 5V input, switches at 300kHz, has MOSFETs with a 4nF gate capacitance, $R_{DS,on}$ = 10mΩ for both MOSFETS and a rise and fall time of 50nsec. The inductor has a winding resistance of 3mΩ, and the sense resistor used is 5.2mΩ. The schottky paralleled with the synchronous rectifier has a forward voltage of 400mV at 14A. The input capacitors have a total ESR of 15mΩ.

$$P_{RDS} = (14A)^2 10m\Omega = 1.96W$$

$$P_{RISE} + P_{FALL} = \frac{5V \times 14A(50nsec + 50nsec)300kHz}{2} = 1.05W$$

$$P_{RISE} + P_{FALL} = \frac{400mV \times 14A(50nsec + 50nsec)300kHz}{2} = 84mW$$

$$P_{INDUCTOR} = (14A)^2 3m\Omega = 590mW$$

$$P_{SENSE} = (14A)^2 5.2m\Omega = 1.02W$$

$$P_{GATE} = 4nF(5V)^2 300kHz \times 2 = 60mW$$

$$P_{DIODE} = 14A \times 400mV \times 50nsec \times 300kHz = 84mW$$

$$P_{CAPS} = 15m\Omega \times (14A)^2 \times 0.56 \times (1 - 0.56) = 724mW$$

$$P_{IC} = 25mA \times 5V \times 125mW$$

$$P_{LOSS} = 1.96W + 1.05W + 0.084W + 0.59W + 1.02W + 0.06W + 0.084W + 0.724W + 0.125W = 5.70W$$

$$\text{Efficiency} = \frac{2.8V \times 14A}{2.8V \times 14A + 5.70W} = 87\%$$

When using these formulae, special care must be taken regarding the MOSFETs' transition times: the rise and fall refer to the MOSFETs' drain-source voltage, NOT the gate-source. Using the datasheet values (rather than measured values) can also result in serious overestimation of the losses, since the transition is being driven by an inductive source, not a resistor.

## Selecting the Inductor

The inductor is one of the most critical components to be selected for a DC-DC converter application. The critical parameters of the inductor are its inductance (L), maximum DC current ($I_O$), and DC coil resistance ($R_l$).

The inductor's inductance helps determine two key parameters of a converter, its ripple current and its transient response. On the one hand, making the inductance large reduces the ripple current, and thus the output ripple voltage. On the other hand, a large inductance provides a slow response to load transients. For Pentium II supplies, the transient response is paramount, and thus the inductance is typically chosen to be in the 1-5µH range.

Most inductors' inductance also depends on current, that is, increasing the current through the inductor decreases the inductance. It is thus vital to specify the DC current when procuring an inductor. The one type of inductor which does not change inductance with current is the rod-core inductor, but this type may have significant EMI (noise) problems. For further information, refer to Applications Bulletin AB-12.

The resistance of the winding of the inductor is also important, as it is directly responsible for much of the losses in the inductor. Minimizing the resistance will help improve the converter's efficiency.

## Implementing Over-current Protection

Intel currently requires all power supply manufacturers to provide continuous protection against short circuit conditions that may damage the CPU. To address this requirement, Fairchild Semiconductor has implemented a current sense methodology to limit the power delivered to the load in the event of over-current. The voltage drop created by the output current across a sense resistor is presented to one terminal of an internal comparator with hysteresis. The other comparator terminal has the threshold voltage, nominally of 120mV. Table 7 states the limits for the comparator threshold of the Switching Regulator.

### Table 7. RC5051 Over-current Comparator Threshold Voltage

| | Short Circuit Comparator $V_{threshold}$ (mV) |
|---|---|
| Typical | 120 |
| Minimum | 100 |
| Maximum | 140 |

When designing the external current sense circuitry, pay careful attention to the output limitations during normal operation and during a fault condition. If the over-current protection threshold current is set too low, the DC-DC converter may not be able to continuously deliver the maximum CPU load current. If the threshold level is too high, the output driver may not be disabled at a safe limit and the resulting power dissipation within the MOSFETs may rise to destructive levels. The following is the design equation used to set the over-current threshold limit:

$$I_{PK} = I_{LOAD,\,MAX} + \frac{I_{RIPPLE}}{2}$$

Where $I_{pk}$ is defined as in Figure 7, and $I_{load,\,max}$ = maximum output load current. Figure 7 illustrates the inductor current waveform for the RC5051 DC-DC converter at maximum load.

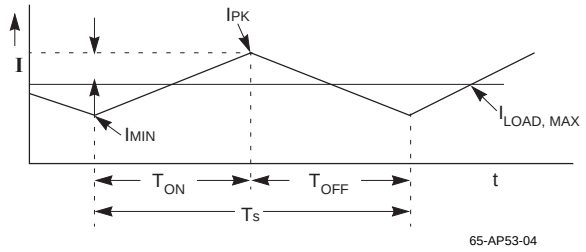



**Figure 7. Typical DC-DC Converter Inductor Current Waveform**

The calculation of the ripple current is as follows:

$$\frac{I_{RIPPLE}}{2} = \frac{V_{IN} - V_{OUT}}{2L} T_S \frac{V_{OUT}}{V_{IN}}$$

where:

$V_{IN}$ = input voltage to converter,

$T_S$ = the switching period of the converter = $1/f_S$, and

$f_S$ = switching frequency.

As an example, for an input voltage of 5V, output voltage of 2.8V @ 14A, L equal to 1.3µH and a switching frequency of 285KHz (using $C_{EXT}$ = 100pF), the peak inductor current can be calculated as :

$$I_{PK} = 14A + \frac{5V - 2.8V}{2 \times 1.3\mu H} \times \frac{1}{285kHz} \times \frac{2.8V}{5V} = 15.7A$$

Therefore, the over-current detection threshold must be at least 16A. The next step is to determine the value of the sense resistor. Including sense resistor tolerance, the sense resistor value can be determined as

$$R_{SENSE} = \frac{V_{th,min}}{I_{SC}(1 + TF)}$$

Where TF = Tolerance Factor for the sense resistor. Table 8 describes tolerance, size, power capability, temperature coefficient and cost of various type of sense resistors.

**Table 8. Comparison of Sense Resistors**

| Description | Motherboard Trace Resistor | Discrete Iron Alloy Resistor (IRC) | Discrete Metal Strip Surface Mount Resistor (Dale) | Discrete MnCu Alloy Wire Resistor | Discrete CuNi Alloy Wire Resistor (Copel) |
|---|---|---|---|---|---|
| Tolerance Factor (TF) | ±20% | ±5% (±1% available) | ±1% | ±10% | ±10% |
| Size (L x W x H) | 2" x 0.2" x 0.001" (1 oz Cu trace) | 0.45" x 0.065" x 0.200" | 0.25" x 0.125" x 0.025" | 0.200" x 0.04" x 0.160" | 0.200" x 0.04" x 0.100" |
| Power capability | >50A/in | 1 watt (3W and 5W available) | 1 watt (2W available) | >1 watt | >1 watt |
| Temperature Coefficient | +3900 ppm | +390 ppm | ±75 ppm | ±50 ppm | ±20 ppm |
| Cost @10,000 piece | Low---included in motherboard | $0.31 | $0.47 | $0.09 | $0.09 |

Continuing with the example, based on the Tolerance Factor in the above table, for an embedded PC trace resistor and for $I_{SC}$ set 1A greater than $Ip_k$:

$$R_{SENSE} = \frac{100mV}{(15.7A + 1A)(1 + 0.20)} = 5.0m\Omega$$

For a discrete Cuni resistor**:**

$$R_{SENSE} = \frac{100mV}{(15.7A + 1A)(1 + 0.10)} = 5.7m\Omega$$

For user convenience, Table 9 lists the recommended values for sense resistors for various load currents using embedded trace resistors and discrete resistors and assuming $(I_{pk} - I_{min}) / 2 = 10\% I_{OUT}$ and $I_{SC}$ set 1A greater than $I_{pk}$

**Table 9. $R_{sense}$ for Various Load Currents**

| $I_{Load,max}$ (A) | $R_{SENSE}$ PC Trace Resistor (mΩ) | $R_{SENSE}$ Discrete Resistor (mΩ) |
|---|---|---|
| 6.9 | 9.7 | 10.6 |
| 7.8 | 8.7 | 9.5 |
| 8.5 | 8.1 | 8.8 |
| 8.7 | 7.9 | 8.6 |
| 9.6 | 7.2 | 7.9 |
| 10.6 | 6.6 | 7.2 |
| 11.1 | 6.3 | 6.9 |
| 12.6 | 5.6 | 6.1 |
| 14.2 | 5.0 | 5.5 |
| 17.2 | 4.2 | 4.6 |
| 18.5 | 3.9 | 4.3 |
| 18.9 | 3.8 | 4.2 |

## Comment on Discrete Sense Resistors

Discrete Iron Alloy resistors come in a variety of tolerances and power ratings, and are ideal for precision implementation, minimizing stress on the MOSFETs. MnCu Alloy wire resistors or CuNi Alloy wire resistors are ideal for low cost implementations.

### Designing an Embedded Sense Resistor (PC Trace Resistor)

Embedded PC trace resistors have the advantage of near zero cost implementation. However, the value of the PC trace resistance has large variations. To start with, traces on the outside layers have far more variation than those on inside layers; for this reason, embedded resistors should always be designed on inside layers. Embedded resistors have 3 error sources: the sheet resistivity of the layer, the tolerance of the width and length of the trace, and the temperature variation of the copper. Only two of the error sources must be considered for laying out embedded sense resistors.

- **Sheet resistivity.**
  For 1 ounce copper, the thickness is nominally 1.3mils, and the toleranace is typically ±.1 mil. Therefore error due to sheet resistivity is 0.1 mil / 1.3mil = +/-8%
- **Tolerance of width and length.**
  The width and length of traces also have tolerances; typical numbers might be ±3/4 mil. A typical width to obtain a 5.2mΩ resistor might be 300mils, and so the length would have to be:

$$L = \frac{t \times w \times R}{\rho} = \frac{1.3mil \times 300mil \times 5.2m\Omega}{6.77 \times 10^{-4}\Omega\text{–mil}} = 2996mils$$

or 3 inches. The tolerance is thus negligible.

- **Thermal Consideration.**
  Due to $I^2R$ power losses the temperature of the resistor will increase, leading to a higher resistance value. In addition, ambient temperature variation will add to the change in resistor value:

  $$R = R_{20C} \times 1.00393^{T-20}$$

  where: $R_{20C}$ is the resistance at 20°C, T is the trace's temperature, and R is the actual resistance. For example, for temperature T = 50°C, the %R change = 12%. Table 10 is the summary of the tolerance for the Embedded PC Trace Resistor.

## Table 10. Summary PC Trace Resistor Tolerance

| | |
|---|---|
| Tolerance due to Sheet Resistivity variation | 8% |
| Tolerance due to temperature variation | 12% |
| Total Tolerance for PC Trace Resistor | 20% |

### Design Rules for Using an Embedded Resistor

The basic equation for the resistance of an embedded resistor is:

$$R = \rho \times \frac{L}{W \times t}$$

where:

ρ = Resistivity(μΩ-mil),
L = Length(mils),
W = Width(mils), and
t = Thickness(mils).

For 1oz copper, t = 1.3 mils, ρ = 677μΩ-mil,
1 L/1 W = 1 Square ( □ ).

For example, you can layout a 5.20mΩ embedded sense resistor using the example above

L/W = 300mils

$$L = \frac{RWt}{\rho} = \frac{0.0052 \times 300 \times 1.3}{677} = 3000\text{mils}$$

L/W = 10 □

Refer to Figure 8.

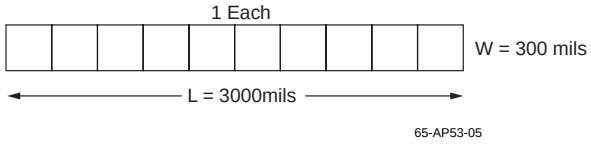



**Figure 8. 5.20mΩ Sense Resistor (10 □)**

You can also implement the sense resistor in the following manner. Each corner square is counted as 0.6 square since current flowing through the corner square does not flow uniformly and it is concentrated towards the inside edge, as shown in Figure 9.

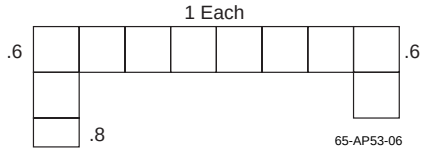



**Figure 9. 5.30mΩ Sense Resistor (10 □)**

### A Design Example Combining an Embedded Resistor and a Discrete Resistor

For low cost implementation, the embedded PC trace resistor is most desirable. However, its wide tolerance (20%) can present a problem. In addition, requirements for the CPU change frequently, and, thus, the maximum load current may be subject to change. Combining embedded resistors with discrete resistors may be a desirable option. Figure 10 shows a design that provides flexibility with a solution to address wide tolerances. In this design, you have the option to choose an embedded or a discrete sense resistor. To use the discrete sense resistor, populate R21 with a shorting bar (zero Ohm resistor) for proper Kelvin connection and add the MnCu sense resistor. To use the embedded sense resistor, on the other hand, populate R22 with a shorting bar for Kelvin connection. The embedded sense resistor allows the user to choose a plus or a minus delta resistance tap to offset any large sheet resistivity change. In this design, the center tap yields 6mΩ, the left tap yields 6.8mΩ, and the right tap yields 5.3mΩ.

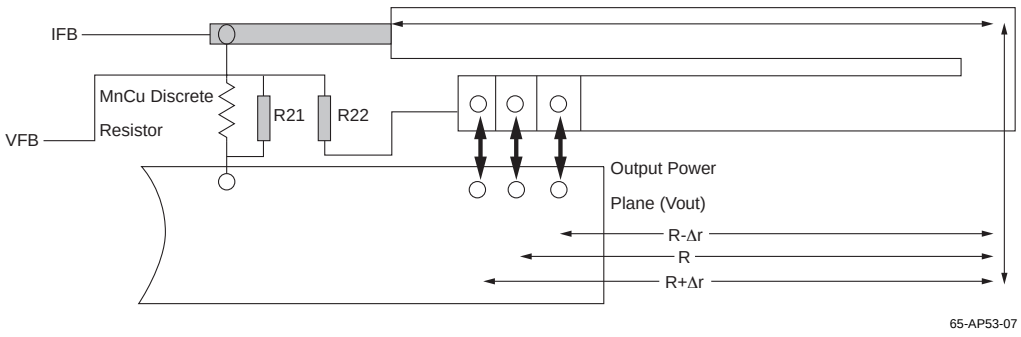



**Figure 10. Short Circuit Sense Resistor Design Using a PC Trace Resistor and an Optional Discrete Sense Resistor**

## RC5051 over-current Characteristics

The RC5051 over-current characteristic includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of an over-current. Figure 11 shows the typical characteristic of the DC-DC converter circuit with a 6mΩ sense resistor. The converter exhibits a normal load regulation characteristic until the voltage across the resistor exceeds the internal over-current threshold of 120mV. At this point, the internal comparator trips and signals the controller to reduce the duty cycle of the high-side MOSFET. This causes a drastic reduction in output voltage as the load regulation collapses into the over-current control mode. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe range for the DC-DC converter.

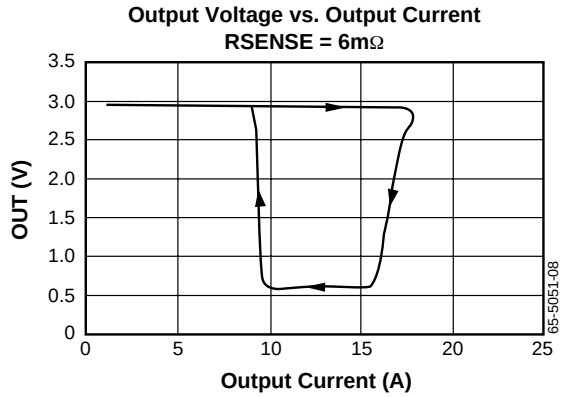



**Figure 11. RC5051 Over-current Characteristic**

## Power Dissipation Consideration During an Over-current Condition

The RC5051 controller responds to an output over-current by drastically reducing the duty cycle of the gate drive signal to the high-side MOSFET. In doing this, the high-side MOSFET is protected from stress and from eventual failure. Figure 12A shows the gate drive signal of a typical RC5051 operating in continuous mode with a load current of 10A. The duty cycle is set by the ratio of the input voltage to the output voltage. If the input voltage is 5V, and the output voltage is 2.8V, the ratio of Vout/ Vin is 56% (64% measured). Figure 12B shows the result of a RC5051 going into its over-current mode with a duty cycle of approximately 47%. Calculating the power in each MOSFET at each condition on the graph (Figure 11) shows how the protection works. The power dissipated in the high-side MOSFET at normal operation for a load current of 14.2A, is given by:

$$P_D = I^2 \times R_{DS,ON} \times DC = (14.2)^2 \times .01 \times .64 = 1.29W$$

ignoring switching losses.

The power dissipated in the MOSFET at an over-current condition of 20A, is given by:

$$P_D = (20)^2 \times .01 \times .47 = 1.88W$$

again ignoring switching losses.

These calculations show that the high-side MOSFET is not being over-stressed during an over-current condition.

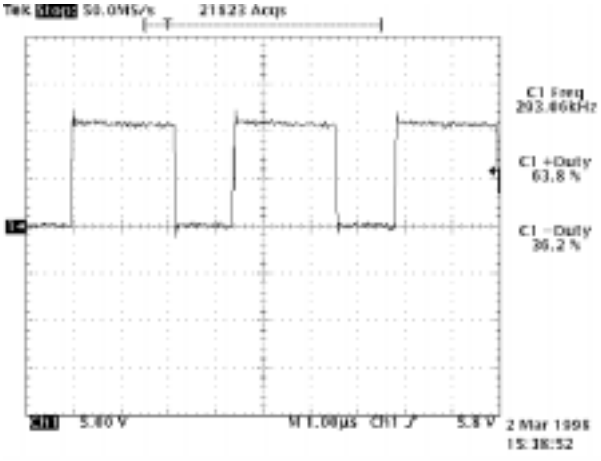



**Figure 12A. HIDRV Output Waveform for Normal Operation Condition with $V_{out}$ = 2.8V@10A**

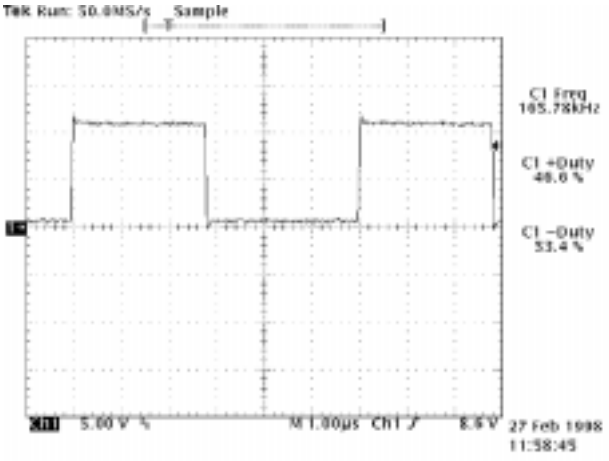



**Figure 12B. HIDRV Output Waveform for Over-current Condition**

Power dissipation in the low-side MOSFET during an over-current condition must also be considered. The low-side MOSFET dissipates power while the high-side MOSFET is off. The power dissipated in the low-side MOSFET during normal operation, is given by:

$$= I^2 \times R_{RDS,ON} \times (1 - DC) = (14.2)^2 \times .01 \times .36 = 0.73$$

During an over-current , the duty cycle reduces to around 47%. The power dissipated in the low-side MOSFET during short circuit condition, is given by:

$$P_D = (20)^2 \times .01 \times .53 = 2.1W$$

Thus, for the low-side MOSFET, the thermal dissipation during over-current is greatly magnified. This requires that the thermal dissipation of the low-side MOSFET be properly managed by an appropriate heat sink. To protect the low-side MOSFET from being destroyed in the event of an over-cur-

rent , you should limit the junction temperature to less than 130°C. You can find the required thermal resistance using the equation for maximum junction temperature:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\Theta JA}}$$

Assuming that the ambient temperature is 50°C,

$$R_{\Theta JA} = \frac{T_{J(max)} - T_A}{P_D} = \frac{130 - 50}{2.1} = 38°C/W$$

Thus, you need to provide a heat sink that gives the low-side MOSFET a thermal resistance of 38°C/W or lower to protect the device during an indefinite short.

In summary, with proper heat sink, the low-side MOSFET is not over-stressed during an over-current condition.

## Schottky Diode Selection

The application circuit diagram of Figure 3 shows a Schottky diode, D2. D2 is used as a flyback diode to provide a current path for the inductor current during the dead-time when both the high-side and low-side MOSFETs are briefly both turned off. Table 11 shows the characteristics of several Schottky diodes. Note that MBRB2515L has a very low forward voltage drop even at high current. Although it is not necessary to use a high-current diode for this application, selecting a higher current schottky will provide improved efficiency at slightly higher cost.

### Table 11. Schottky Diode Selection Table

| Manufacturer Model # | Conditions | Forward Voltage $V_F$ |
|---|---|---|
| Motorola 1N5817 | $I_F$ = 1A; $T_j$ = 25°C | <.45v |
| Motorola 1N5820 | $I_F$ = 3A; $T_j$ = 25°C | <.475v |
| Motorola MBR2015CTL | $I_F$ = 20A; $T_j$ = 25°C<br>$I_F$ = 20A;$T_j$ = 150°C | < 0.58v<br>< 0.48v |
| Motorola MBRB2515L | $I_F$ = 19A; $T_j$ = 70°C | < 0.28v |

## Output Filter Capacitors

Correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple, and, most importantly, load transient response. Because the control loop response of the controller is not instantaneous, the initial load transient must be supplied entirely by the output capacitors. The initial voltage deviation is determined by the total ESR of the capacitors used and the parasitic resistance of the output traces. For a detailed analysis of capacitor requirements in a high-end microprocessor system, please refer to Application Bulletin 14.

## Input Filter

The DC-DC converter may include an input inductor between the system +5V supply and the converter input as described below. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is typical, as illustrated in Figure 13; details on selection of an input inductor may be found in Applications Bulletin AB-16.

The number of input capacitors required for a converter is determined by the capacitors' ripple current rating. The ripple current is given by:

$$I_{rms} = I_{OUT}\sqrt{DC - DC^2}$$

Thus, for example, a Deschutes processor running at 2.0V out from 5.0V in has a DC = 2.0/5.0 = .4; if it pulls 14.2A, its $I_{rms}$ = 7A.

Table 12 shows some typical input capacitors' current ratings; the current rating increases as temperature decreases. Although exceeding these ratings will not cause capacitor damage, it will reduce their life, and thus the converter's MTBF.

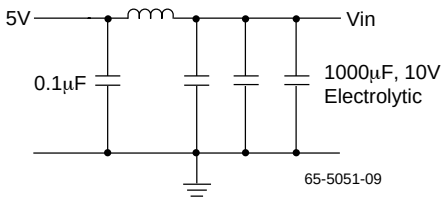



**Figure 13. Typical Input Filter**

### Table 12. Input Capacitor Selection Guide

| Manufacturer | Part # | $I_{rms}$ |
|---|---|---|
| Sanyo | 10MV1200GX | 2.0A @ 65°C |
| United Chemicon | LXZ10VB122M10X20 | 1.2A @ 105°C |
| Panasonic | EEUFA10122 | 1.2A @ 105°C |

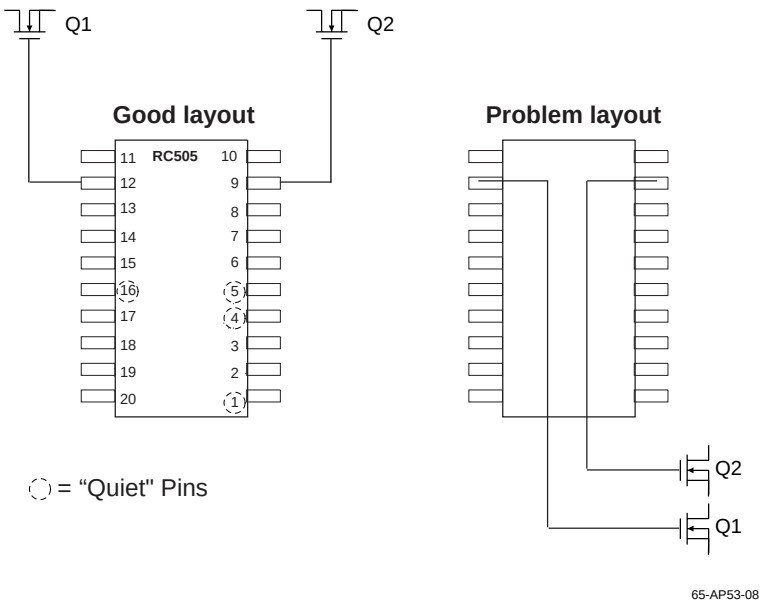



**Figure 14. Placement of the MOSFETs**

# PCB Layout Guidelines and Considerations

## PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5051 is critical. Place the MOSFETs (Q1 & Q2) so that the trace length from the RC5051 HIDRV and LODRV pins to the FET gates is minimized. A long lead length on this pin would cause high amounts of ringing due to the inductance of the trace and the large gate capacitance of the FET. This noise radiates all throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.

  Figure 14 shows an example of good placement for the MOSFETs in relation to the RC5051. In addition, this figure shows an example of problematic placement for the MOSFETs.

  In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5051. That is, traces that connect to pins 9, 12 and 13 (LODRV, HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1, 2, 4 and 5, and pin 16.

- Place the 0.1µF decoupling capacitors as close to the RC5051 pins as possible. Extra lead length degrades their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps to provide isolation between pins.
- Surround the CEXT timing capacitor with a ground trace. Be sure to place a ground or power plane under the capacitor for further noise isolation to provide additional shielding to the oscillator pin 1 from the noise on the PCB. In addition, place this capacitor as close to the RC5051 pin 1 as possible.
- Place the MOSFETs, inductor and Schottky as close together as possible for the same reasons as on the first bullet above. Place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a 0.1µF decoupling capacitor right on the drain of each MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU allows the parasitic resistance of the board traces to degrade the DC-DC converter’s performance under load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- The traces that run from the RC5051 IFB (pin 4) and VFB (pin 5) pins should be run next to each other and Kelvin connected to the sense resistor. Running these lines together prevents some of the common mode noise that is presented to the RC5051 feedback input. Try, as much as possible, to run the noisy switching signals (LODRV, HIDRV & VCCQP) on one layer, but use the inner layers for power and ground only. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VFB and IFB.

### Example of a PC Motherboard Layout and Gerber File.

This section shows a reference design for motherboard implementation of the RC5051 along with the Layout Gerber File and Silk Screen. The actual PCAD Gerber File can be obtained from Fairchild Semiconductor local Sales Office .

## Guidelines for Debugging and Performance Evaluations

### Debugging Your First Design Implementation

1. Note the setting of the VID pins to know what voltage is to be expected.
2. Do not connect any load to the circuit. While monitoring the output voltage, apply power to the circuit with current limiting at the power source. This ensures that no catastrophic shorts are present.
3. If proper voltage is not achieved go to “Procedures” below.
4. When you have proper voltage, increase the current limiting of the power source to 16A.
5. Apply load in 1A increments. An active load (HP6060B or equivalent) is suggested.
6. In case of poor regulation refer to “Procedures” below.

### Procedures

1. If there is no voltage at the output and the circuit is not drawing current look for opens in the connections, check the circuitry versus schematic, and check the power supply pins of the RC5051 to make sure that voltage(s) are applied.
2. If there is no voltage at the output and the circuit is drawing excessive current (>100mA) with no load, check for possible shorts. Determine the path of the excessive current and which device is drawing it–this current may be drawn by peripheral components.
3. If the output voltage comes close to the expected value, check the VID inputs at the device pins. The part is factory set to respond properly to the VID inputs.
4. Shut down at too low a current can be caused by an inappropriate value of the sense resistor. See the “Sense Resistor” section.
5. Poor load regulation can be due to many causes. Check the voltages and signals at the critical pins.
6. The VREF pin should be at the voltage set by the VID pins. If the power supply pins and the VID pins are correct the VREF should have the correct voltage.
7. Next check the oscillator pin. You should see a saw tooth wave at the frequency set by the external capacitor.
8. When the VREF and CEXT pins are checked and correct and the output voltage is incorrect, look at the waveform at VCCQP. This pin should be +12V (in the +12V application), and should be swinging from slightly below +5V to about +10V (in the charge pump application). If the VCCQP pin is noisy, with ripples/ over-shoots riding on it this may make the converter function incorrectly.
9. Next, look at HIDRV pin. This pin directly drives the gate of the high-side FET. It should provide a gate drive (measured gate to ground) of about 10V when turning the FET on. A careful study of the layout is recommended. Refer to the “PCB Layout Guidelines” section.
10. Past experience shows that the most frequent errors are incorrect components, improper connections, and poor layout.

### Performance Evaluation

This section shows sample evaluation results as a reference guide for evaluating a DC-DC Converter using the RC5051 on a Pentium II motherboard.

### DC Regulation

| $VID_{(2.0V)}$ 43210 | $I_{load}$ (A) | $V_{out}$ (V) |
|---|---|---|
| 2.0V 00001 | 0.5 | 2.019 |
| | 1 | 2.018 |
| | 2 | 2.017 |
| | 3 | 2.016 |
| | 4 | 2.014 |
| | 5 | 2.013 |
| | 6 | 2.012 |
| | 7 | 2.010 |
| | 8 | 2.009 |
| | 9 | 2.007 |
| | 10 | 2.006 |
| | 11 | 2.005 |
| | 12 | 2.004 |
| | 13 | 2.003 |
| | 14 | 2.001 |
| | 14.5 | 2.001 |
| Load Regulation 0.5-14.5A | | 0.90% |

The DC output voltage is measured from minimum to maximum load current. Ideally, the RC5051 should show about 20mV droop between these two limits. Note that the measurement must be taken directly on the leads of the output capacitors, since there may otherwise be parasitic resistances causing additional droop.

### Output voltage load transients due to load current step

| | Test Condition | Measured | Comment |
|---|---|---|---|
| Low to high Current Step (Vout = 2.00V) | 0.5A-14.5A | 96mV | Limit = 130mV PASS Figure 15 |
| High to Low Current Step (Vout = 2.00V) | 14.5A-0.5A | 109mV | Limit = 130mV PASS Figure 16 |

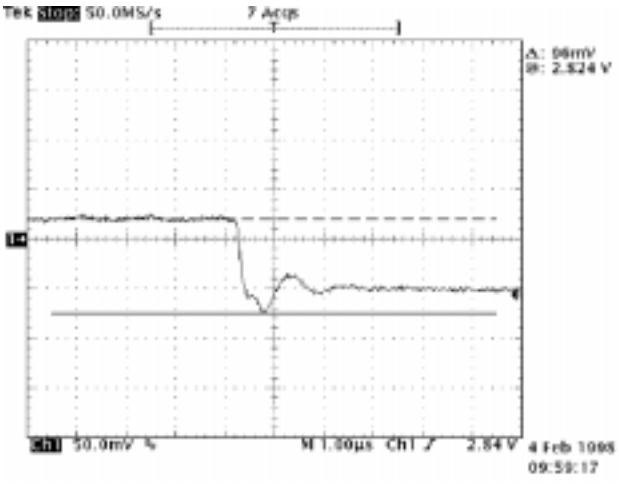



**Figure 15. Low to High Current Transiet Response**

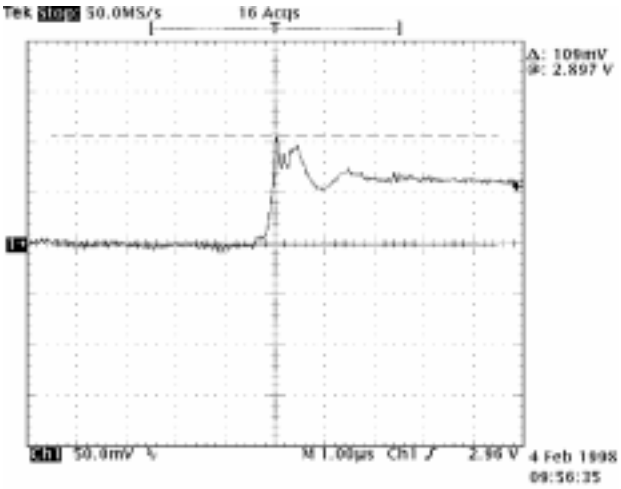



**Figure 16. High to Low Current Transiet Response**

The output voltage transient response to the worst-case step current load is measured using an Intel EMT tool. Again, the measurement must be taken directly on the leads of the output capacitors, since there may otherwise be parasitic resistances and inductances causing additional droop.

### Over-Current Limit

Using an electronic load, the output current should be slowly increased until the converter hits over-current limit. Reaching this limit will be evident because the output voltage quickly drops out of regulation as the current is increased.

### Component Case Temperature

Each of the major components should be measured for excessive temperature, which can be indicative of a problem. At the least, the RC5051, the MOSFETs and the schottky diode should all be measured. The converter should be run at its maximum load current until it reaches thermal stability, at least 20 minutes, before the temperature measurements are taken.

# Notes

# Notes

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