Dual 10-Bit 40MSPS Low-Power ANALOG-TO-DIGITAL CONVERTER with PGA

FEATURES

- 3.3V Single-Supply Operation
- Dual Simultaneous Sample-and-Hold Inputs
- Differential or Single-Ended Analog Inputs
- Programmable Gain Amplifier: 0dB to 18dB
- Separate Serial Control Interface
- Single or Dual Parallel Bus Output
- 60dB SNR at f_{IN} = 10.5MHz
- 73dB SFDR at f_{IN} = 10.5MHz
- Low Power: 275mW
- 300MHz Analog Input Bandwidth
- 3.3V TTL/CMOS-Compatible Digital I/O
- Internal or External Reference
- Adjustable Reference Input Range
- Power-Down (Standby) Mode
- TQFP-48 Package

APPLICATIONS

- Digital Communications (Baseband Sampling)
- Portable Instrumentation
- Video Processing

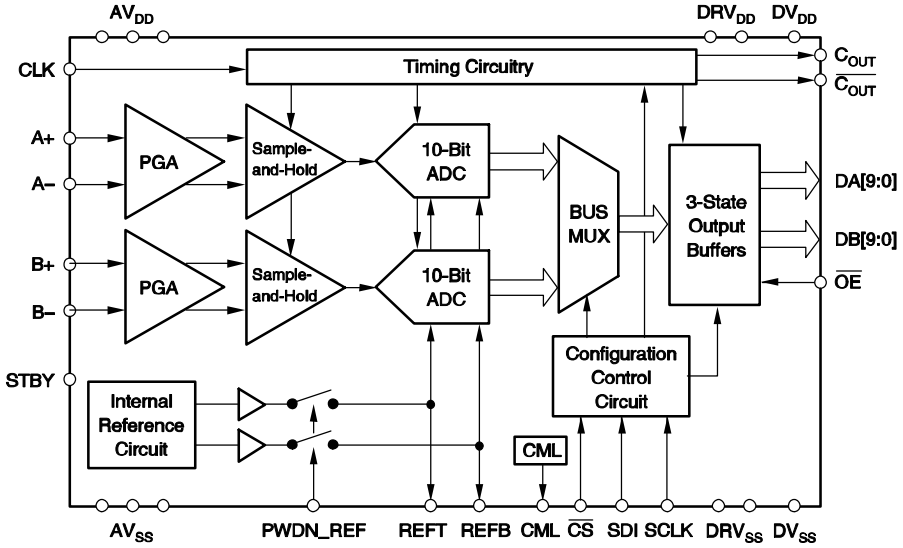
DESCRIPTION

The ADS5204 is a dual 10-bit, 40MSPS Analog-to-Digital Converter (ADC). It simultaneously converts each analog input signal into a 10-bit, binary coded digital word up to a maximum sampling rate of 40MSPS per channel. All digital inputs and outputs are 3.3VTTL/CMOS compatible.

An innovative dual pipeline architecture implemented in a CMOS process and the 3.3V supply results in very low power dissipation. In order to provide maximum flexibility, both top and bottom voltage references can be set from user-supplied voltages. Alternatively, if no external references are available, the on-chip internal references can be used. Both ADCs share a common reference to improve offset and gain matching. If external reference voltage levels are available, the internal references can be powered down independently from the rest of the chip, resulting in even greater power savings.

The ADS5204 also features dual, onboard Programmable Gain Amplifiers (PGAs) that allow a setting of 0dB to 18dB to adjust the gain of each set of inputs in order to match the amplitude of the incoming signal.

The ADS5204 is characterized for operation from –40°C to +85°C and is available in a TQFP-48 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

PRODUCT	PACKAGE–LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5204	TQFP–48	PFB	–40°C to +85°C	AZ5204	ADS5204IPFB	Tray, 250
ADS5204	TQFP–48	PFB	–40°C to +85°C	AZ5204	ADS5204IPFBR	Tape and Reel, 1000

(1) For the most current specifications and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1).

Supply Voltage: AV_{DD} to AGND, DV_{DD} to DGND	–0.5V to 3.6V
Supply Voltage: AV_{DD} to DV_{DD}, AGND to DGND	–0.5V to 0.5V
Digital Input Voltage Range to DGND	–0.5V to DV_{DD} + 0.5V
Analog Input Voltage Range to AGND	–0.5V to AV_{DD} + 0.5V
Digital Output Voltage Applied from Ext. Source to DGND	–0.5V to DV_{DD} + 0.5V
Reference Voltage Input Range to AGND: V_{REFT}, V_{REFB}	–0.5V to AV_{DD} + 0.5V
Operating Free–Air Temperature Range, T_A (ADS5204I)	–40°C to +85°C
Storage Temperature Range, T_{STG}	–65°C to +150°C
Soldering Temperature 1.6mm (1/16 inch) from case for 10 seconds	300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, T_A, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply						
Supply Voltage	AV_{DD}		3.0	3.3	3.6	V
	DV_{DD}					
	DRV_{DD}					
Analog and Reference Inputs						
Reference Input Voltage (top)	V_{REFT}	f_{CLK} = 1MHz to 80MHz	1.9	2.0	2.15	V
Reference Input Voltage (bottom)	V_{REFB}	f_{CLK} = 1MHz to 80MHz	0.95	1.0	1.1	V
Reference Voltage Differential	$V_{REFT} – V_{REFB}$	f_{CLK} = 1MHz to 80MHz	0.95	1.0	1.1	V
Reference Input Resistance	R_{REF}	f_{CLK} = 80MHz		1650		Ω
Reference Input Current	I_{REF}	f_{CLK} = 80MHz		0.62		mA
Analog Input Voltage, Differential	V_{IN}		–1		1	V
Analog Input Voltage, Single–Ended(1)	V_{IN}		CML – 1.0		CML + 1.0	V
Analog Input Capacitance	C_I			8		pF
Clock Input(2)			0		AV_{DD}	V
Analog Outputs						
CML Voltage				$AV_{DD}/2$		V
CML Output Resistance				2.3		kΩ
Digital Inputs						
High-Level Input Voltage	V_{IH}		2.4		DV_{DD}	V
Low-Level Input Voltage	V_{IL}		DGND		0.8	V
Input Capacitance				5		pF
Clock Period	t_c (80MHz)		12.5			ns
Pulse Duration	$t_{w(CLKH)}$, $t_{w(CLKL)}$ (80MHz)	Clock HIGH or LOW	5.25			ns
Clock Period	t_c (40MHz)		25			ns
Pulse Duration	$t_{w(CLKH)}$, $t_{w(CLKL)}$ (40MHz)	Clock HIGH or LOW	11.25			ns

(1) Applies only when the signal reference input connects to CML.
(2) Clock pin is referenced to AV_{DD}/AV_{SS}.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions with f_{CLK} = 80MHz and use of internal voltage references, and PGA Gain = 0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Supply							
I_{DD} Operating Supply Current	AV_{DD}	AV_{DD} = DV_{DD} = DRV_{DD} = 3.3V, C_L = 10pF, V_{IN} = 3.5MHz, –1dBFS			64	72	mA
	DV_{DD}				1.7	2.2	
	DRV_{DD}				18	27	
Power Dissipation	P_D	PWDN_REF = 'L'			275	345	mW
		PWDN_REF = 'H'			240	300	
Standby Power	$P_{D(STBY)}$	STDBY = 'H', CLK Held HIGH or LOW			95	150	µW
Power-Up Time for All References from Standby	t_{PD}				550		ms
Wake Up Time	t_{WU}	External Reference			40		µs
Digital Inputs							
High-Level Input Current on Digital Inputs incl. CLK	I_{IH}	AV_{DD} = DV_{DD} = DRV_{DD} = 3.6V		–1		+1	µA
Low-Level Input Current on Digital Inputs incl. CLK	I_{IL}			–1		+1	µA
Digital Outputs							
High-Level Output Voltage	V_{OH}	AV_{DD} = DV_{DD} = DRV_{DD} = 3.0V at I_{OH} = 50µA, Digital Outputs Forced HIGH		2.8	2.96		V
Low-Level Output Voltage	V_{OL}	AV_{DD} = DV_{DD} = DRV_{DD} = 3.0V at I_{OL} = 50µA, Digital Outputs Forced LOW			0.04	0.2	V
Output Capacitance	C_O				5		pF
High-Impedance State Output Current to High–Level	I_{OZH}	AV_{DD} = DV_{DD} = DRV_{DD} = 3.6V		–1		+1	µA
High-Impedance State Output Current to Low–Level	I_{OZL}			–1		+1	µA
Data Output Rise-and-Fall Time		C_{LOAD} = 10pF, Single-Bus Mode			3		ns
		C_{LOAD} = 10pF, Dual-Bus Mode			5		ns
Reference Outputs							
Reference Top Voltage	V_{REFTO}	Absolute Min/Max Values Valid and Tested for AV_{DD} = 3.3V		1.9	2	2.1	V
Reference Bottom Voltage	V_{REFBO}			0.95	1	1.05	V
Differential Reference Votage	REFT – REFB			0.95	1.0	1.05	V
DC Accuracy							
Integral Nonlinearity, End Point	INL	Internal References(1)	T_A = –40°C to +85°C	–1.5	±0.4	+1.5	LSB
Differential Nonlinearity	DNL	Internal References(2)	T_A = –40°C to +85°C	–0.9	±0.4	+1.0	LSB
Missing Codes		No Missing Codes Assured					
Zero Error(3)		AV_{DD} = DV_{DD} = DRV_{DD} = 3.3V External References (3)			0.12	±1.5	%FS
Full-Scale Error					0.28	±1.5	%FS
Gain Error					0.24	±1.5	%FS

(1) Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full-scale. The point used as zero occurs ½LSB before the first code transition. The full-scale point is defined as a level ½LSB beyond the last code transition. The deviation is measured from the center of each particular code to the best-fit line between these two endpoints.

(2) An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. Therefore this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test, (i.e., (last transition level – first transition level)/(2^n – 2)). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1LSB ensures no missing codes.

(3) Zero error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to ½LSB to the bottom reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024). Full-scale error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5LSB from the top reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

DYNAMIC PERFORMANCE(1)

$T_A = T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD} = DRV_{DD} = 3.3V$, f_{IN} = –1dBFS, Internal Reference, f_{CLK} = 80MHz, f_S = 40MSPS, Differential Input Range = 2Vp–p, and PGA Gain = 0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Effective Number of Bits	ENOB	f_{IN} = 3.5MHz		9.7		Bits
		f_{IN} = 10.5MHz	9.3	9.7		Bits
		f_{IN} = 20MHz		9.6		Bits
Total Harmonic Distortion	THD	f_{IN} = 3.5MHz		–71		dB
		f_{IN} = 10.5MHz		–71	–66	dB
		f_{IN} = 20MHz		–68		dB
Signal-to-Noise Ratio	SNR	f_{IN} = 3.5MHz		60.5		dB
		f_{IN} = 10.5MHz		60.5		dB
		f_{IN} = 20MHz		60		dB
Signal-to-Noise Ratio + Distortion	SINAD	f_{IN} = 3.5MHz		60		dB
		f_{IN} = 10.5MHz	57	60		dB
		f_{IN} = 20MHz		60		dB
Spurious-Free Dynamic Range	SFDR	f_{IN} = 3.5MHz		75		dB
		f_{IN} = 10.5MHz	69	73		dB
		f_{IN} = 20MHz		70.5		dB
Analog Input Bandwidth		See Note (2)		300		MHz
2-Tone Intermodulation Distortion	IMD	f_1 = 9.5MHz, f_2 = 9.9MHz		–68		dBc
A/B Channel Crosstalk				–75		dBc
A/B Channel Offset Mismatch				0.016	1.75	% of FS
A/B Channel Full-Scale Error Mismatch				0.025	1.0	% of FS

(1) These specifications refer to a 25Ω series resistor and 15pF differential capacitor between A/B+ and A/B– inputs; any source impedance will bring the bandwidth down.

(2) Analog input bandwidth is defined as the frequency at which the sampled input signal is 3dB down on unity gain and is limited by the input switch impedance.

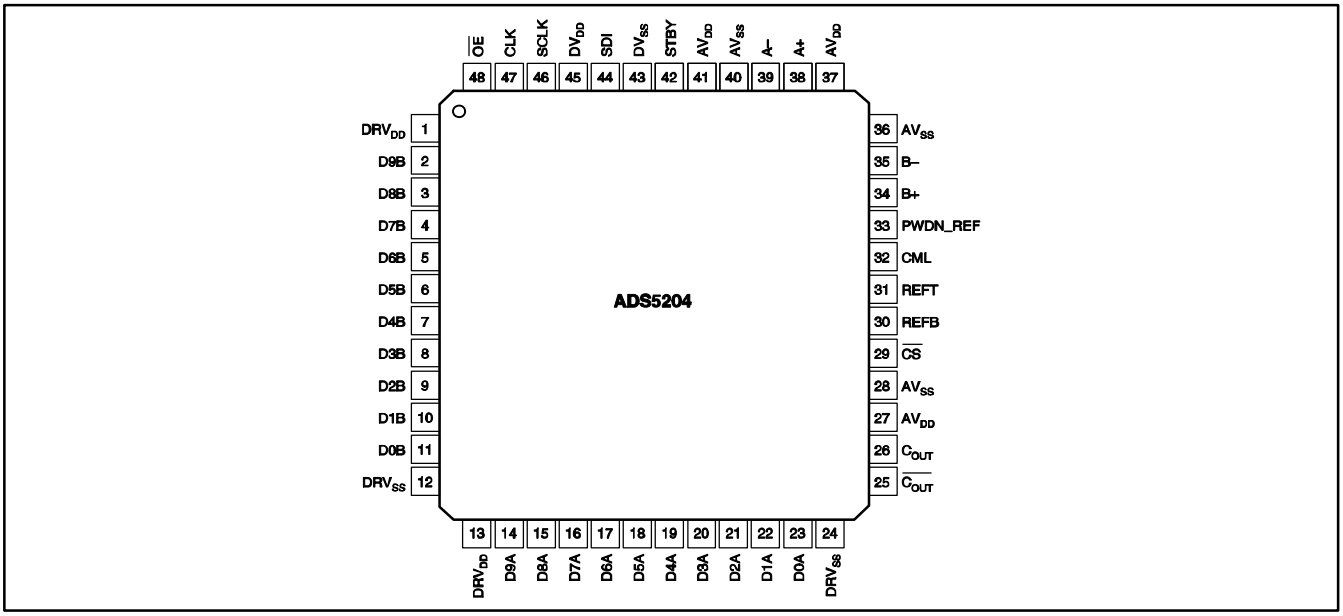
PGA SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Gain Range		0 to 18		dB
Gain Step Size(1)		0.5826		dB
Gain Error(2)	–0.15	±0.025	+0.15	dB
Control Bits Per Channel			5	Bits

(1) Refer to Table 2, PGA Gain Code. Ideal step size: 18.0618dB/31 = 0.5826dB

(2) Deviation from ideal. Refer to Table 2, all gain settings.

PIN CONFIGURATION



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DRV_{DD}	1,13	I	Supply Voltage for Output Drivers
DRV_{SS}	12, 24	I	Digital Ground for Output Drivers
DA 9..0	14-23	O	Data Outputs for Bus A. D9 is MSB. This is the primary bus. Data from both input channels can be output on this bus or data from channel A only. The data outputs are in tri-state during power-down (refer to the Register Configuration table).
DB 9..0	2-11	O	Data Outputs for Bus B. D9 is MSB. This is the second bus. Data is output from the B channel when dual bus output mode is selected. The data outputs are in tri-state during power–down and single–bus modes (refer to Timing Options table).
$\overline{OE}$	48	I	Output Enable. A LOW on this terminal will enable the data output bus, C_{OUT} and $\overline{C_{OUT}}$.
C_{OUT}	26	O	Latch Clock for the Data Outputs. C_{OUT} is in tri–state during power–down.
$\overline{C_{OUT}}$	25	O	Inverted Latch Clock control for the Data Outputs. $\overline{C_{OUT}}$ is in tri–state during power–down.
SDI	44	I	Serial Data I/O
DV_{SS}	43	I	Digital Ground
CLK	47	I	Clock Input. The input is sampled on each rising edge of CLK when using a 40MHz input and alternate rising edges when using an 80MHz input. The clock pin is referenced to AV_{DD} and AV_{SS} to reduce noise coupling from digital logic.
DV_{DD}	45	I	Digital Supply Voltage
AV_{DD}	27,37,41	I	Analog Supply Voltage
$\overline{CS}$	29	I	Serial Data Registers Chip Select
AV_{SS}	28,36,40	I	Analog Ground
B–	35	I	Negative Input for the Analog B Channel
B+	34	I	Positive Input for the Analog B Channel
REFT	31	I/O	Reference Voltage Top. The voltage at this terminal defines the top reference voltage for the ADC. Sufficient filtering should be applied to this input: the use of 0.1µF capacitor between REFT and AV_{SS} is highly recommended. Additionally a 0.1µF capacitor should be connected between REFT and REFB.
REFB	30	I/O	Reference Voltage Bottom. The voltage at this terminal defines the bottom reference voltage for the ADC. Sufficient filtering should be applied to this input: the use of 0.1µF capacitor between REFB and AV_{SS} is recommended. Additionally, a 0.1µF capacitor should be connected between REFT and REFB.
CML	32	O	Common-Mode Level. This voltage is equal to $(AV_{DD} – AV_{SS})/2$. An external capacitor of 0.1µF should be connected between this terminal and AV_{SS} when CML is used as a bias voltage. No capacitor is required if CML is not used.
PDWN_REF	33	I	Power-Down for Internal Reference Voltages. A HIGH on this terminal disables the internal reference circuit.
STBY	42	I	Standby Input. A HIGH on this terminal will power down the device.
A–	39	I	Negative Input for the Analog A Channel
A+	38	I	Positive Input for Analog A Channel
SCLK	46	I	Serial Data Clock. Maximum clock rate is 20MHz.

TIMING REQUIREMENTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Clock Rate	f_{CLK}		1		80	MHz
Conversion Rate			1		40	MSPS
Clock Duty Cycle (40MHz)			45	50	55	%
Clock Duty Cycle (80MHz)			42	50	58	%
Output Delay Time	$t_{d(o)}$	C_L = 10pF		9	14	ns
Mux Setup Time	$t_{s(m)}$		9	10.4		ns
Mux Hold Time	$t_{h(m)}$	C_L = 10pF	1.7	2.1		ns
Output Setup Time	$t_{s(o)}$	C_L = 10pF	9	10.4		ns
Pipeline Delay (latency, channels A and B)	$t_{d(pipe)}$	MODE = 0, SELB = 0		8		CLK Cycles
Pipeline Delay (latency, channels A and B)	$t_{d(pipe)}$	MODE = 1, SELB = 0		4		CLK Cycles
Pipeline Delay (latency, channel A)	$t_{d(pipe)}$	MODE = 0, SELB = 1		8		CLK Cycles
Pipeline Delay (latency, channel B)	$t_{d(pipe)}$	MODE = 0, SELB = 1		9		CLK Cycles
Pipeline Delay (latency, channel A)	$t_{d(pipe)}$	MODE = 1, SELB = 1		8		CLK Cycles
Pipeline Delay (latency, channel B)	$t_{d(pipe)}$	MODE = 1, SELB = 1		9		CLK Cycles
Output Hold Time	$t_{h(o)}$	C_L = 10pF	1.5	2.2		ns
Aperture Delay Time	$t_{d(a)}$			3		ns
Aperture Jitter	$t_{J(a)}$			1.5		ps, rms
Disable Time, $\overline{OE}$ Rising to Hi–Z	t_{dis}			5	8	ns
Enable Time, $\overline{OE}$ Falling to Valid Data	t_{en}			5	8	ns

(1) All internal operations are performed at a 40MHz clock rate.

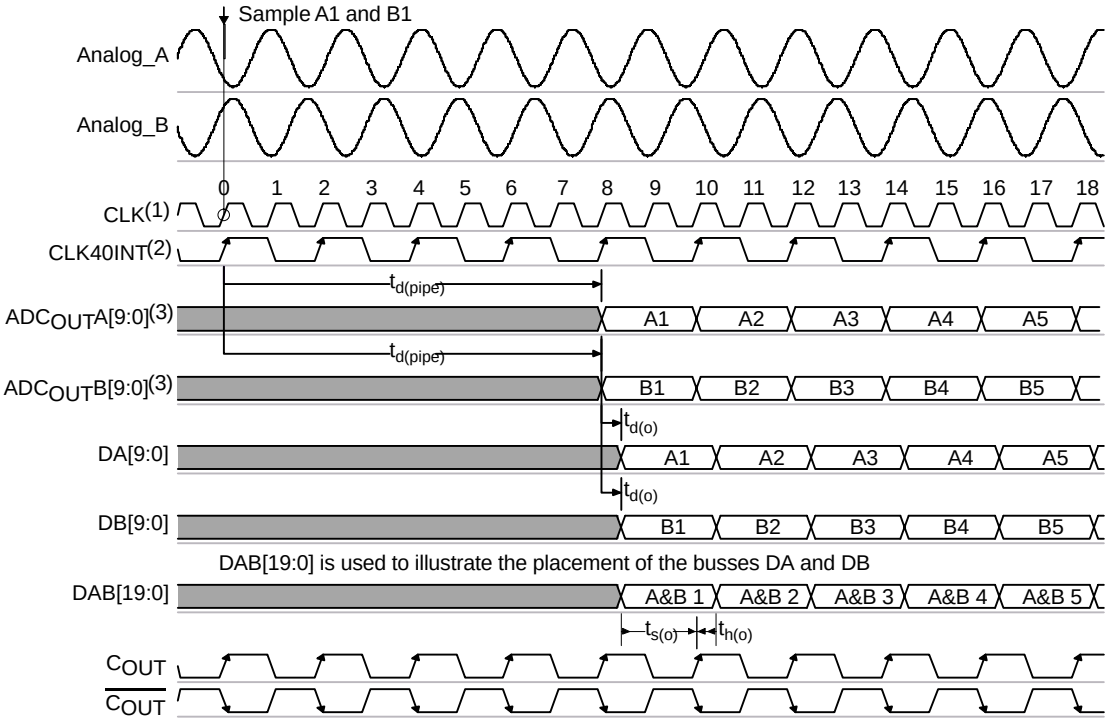
SERIAL INTERFACE TIMING

PARAMETER		MIN	TYP	MAX	UNIT
Maximum Clock Rate	f_{SCLK}	20			MHz
SCLK Pulse Width HIGH	t_{WH}	25			ns
SCLK Pulse Width LOW	t_{WH}	25			ns
Setup Time, $\overline{CS}$ LOW Before First Negative SCLK Edge	$t_{SU(CS\_CK)}$	5			ns
$\overline{CS}$ HIGH Width	$t_{WH(CS)}$	10			ns
Setup Time, 16th Negative SCLK Edge before $\overline{CS}$ Rising Edge	$t_{SU(C16\_CK)}$	5			ns
Setup Time, Data Ready Before SCLK Falling Edge	$t_{SU(D)}$	5			ns
Hold Time, Data Held Valid After SCLK Falling Edge	$t_{SU(H)}$	5			ns

TIMING OPTIONS

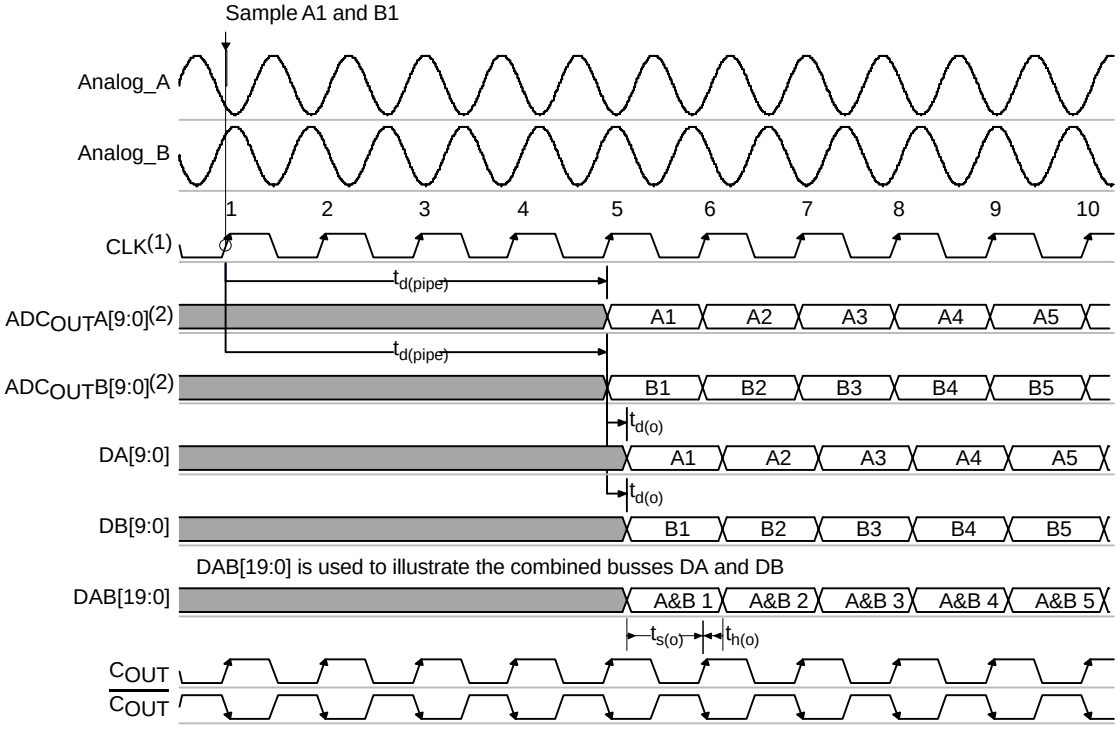
OPERATING MODE	MODE	SELB	TIMING DIAGRAM FIGURE
80MHz Input Clock, Dual-Bus Output, C_{OUT} = 40MHz	0	0	1
40MHz Input Clock, Dual-Bus Output, C_{OUT} = 40MHz	1	0	2
80MHz Input Clock, Single-Bus Output, C_{OUT} = 40MHz	0	1	3
80MHz Input Clock, Single-Bus Output, C_{OUT} = 80MHz	1	1	4

TIMING DIAGRAMS



NOTES: (1) In this option CLK = 80MHz. (2) CLK40INT refers to 40MHz Internal Clock, per channel. (3) Internal signal only.

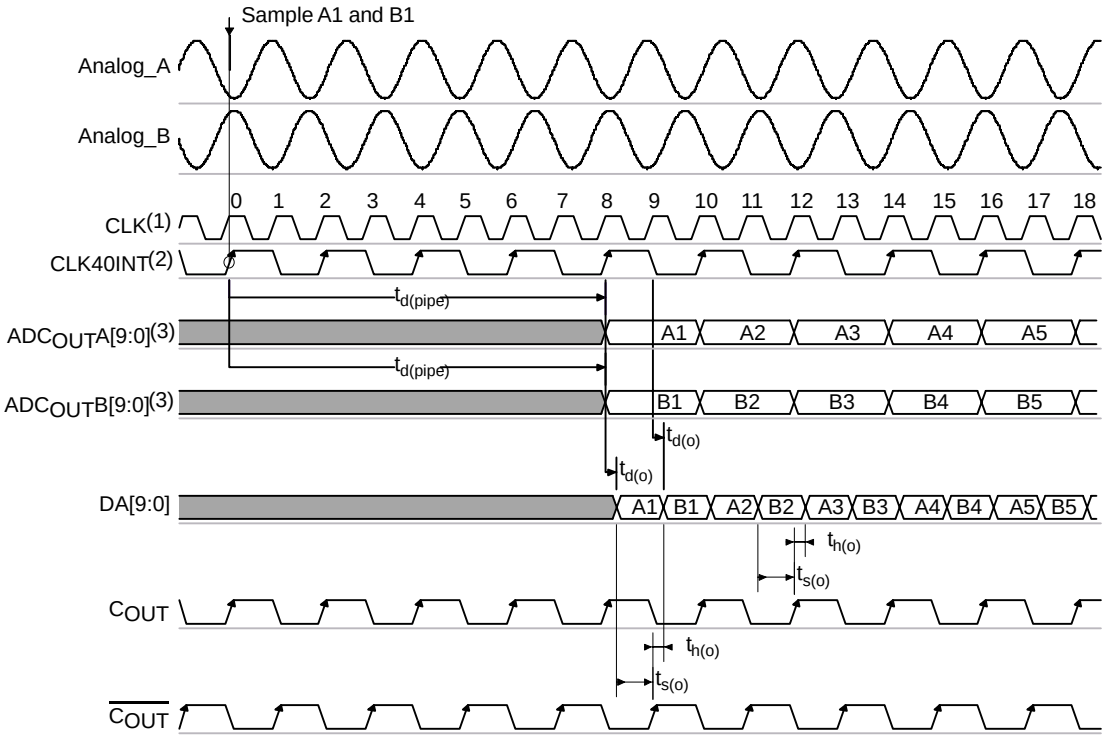
Figure 1. Dual Bus Output—Option 1.



NOTE: (1) In this option CLK = 40MHz, per channel. (2) Internal signal only.

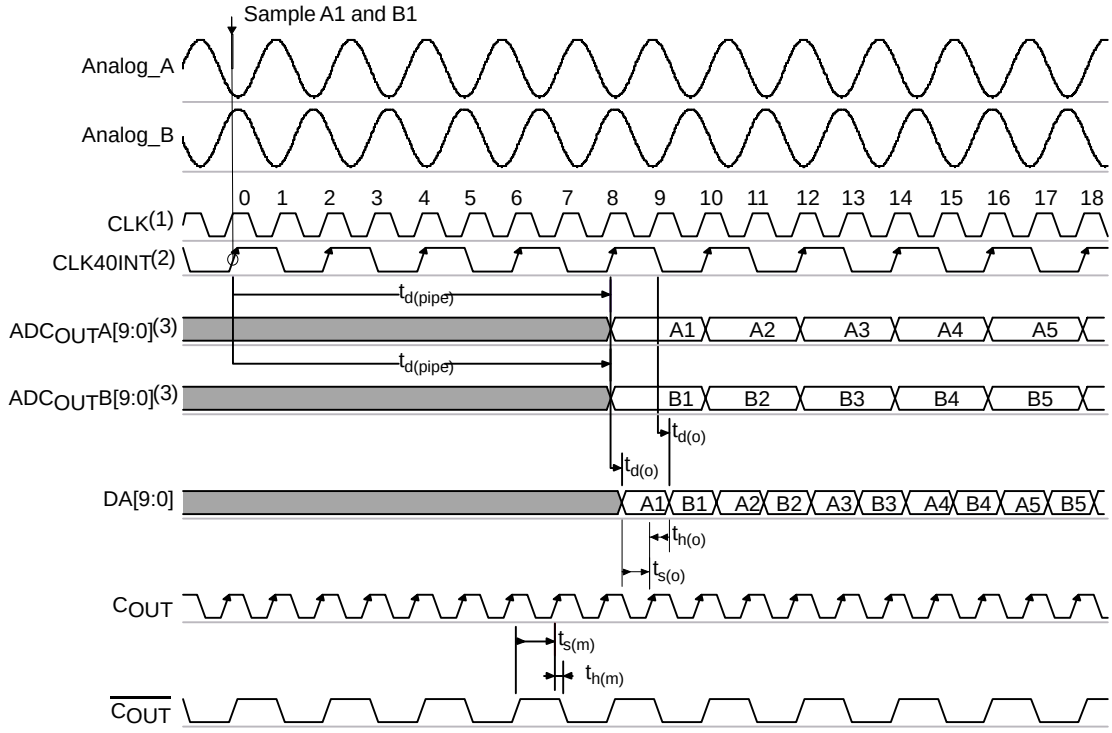
Figure 2. Dual Bus Output—Option 2.

TIMING DIAGRAMS (Cont.)



NOTES: (1) In this option CLK = 80MHz. (2) CLK40INT refers to 40MHz Internal Clock, per channel. (3) Internal signal only.

Figure 3. Single Bus Output—Option 1.



NOTES: (1) In this option CLK = 80MHz. (2) CLK40INT refers to 40MHz Internal Clock, per channel. (3) Internal signal only.

Figure 4. Single Bus Output—Option 2.

TIMING DIAGRAMS (Cont.)

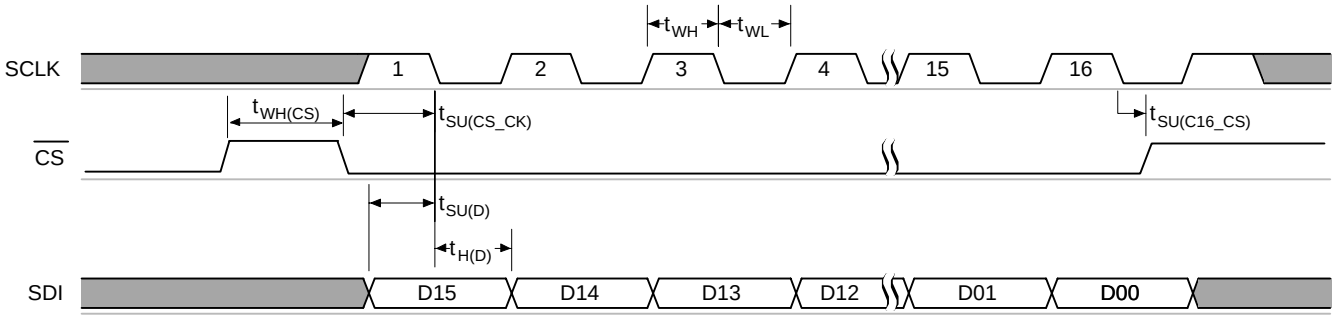


Figure 5. Serial Data Write.

Table 1. Register Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Reserved	TWOS	MODE	SELB	PGA4 B	PGA3 B	PGA2 B	PGA1 B	PGA0 B	PGA4 A	PGA3 A	PGA2 A	PGA1 A	PGA0 A

Always write 0

Default (power-up) condition for this register is all bits = 0. The user register is updated on either the first rising edge of SCLK after the 16th falling edge or $\overline{CS}$ rising, whichever comes first. Raising $\overline{CS}$ before 16 falling SCLK edges have been seen is an incomplete write error and no register update will occur. The PGA gain settings are resynchronized to the internal data conversion clock to avoid data glitches caused by changing gain settings while sampling the inputs.

PGA gain control data is applied to the PGAs on the second falling edge of the ADC sample clock (CLK40INT) after a successful register write. This resynchronization ensures that no analog glitch occurs even when SCLK is asynchronous to CLK.

Note that only the PGA data is resynchronized. The TWOS, MODE, and SELB register bits take effect immediately after a successful register write.

OUTPUT DATA FORMAT

The output data format can either be in Binary Two's Complement ouput mode or in unsigned binary mode, which affects both A and B channels.

TWOS – Binary Two's Complement Mode:

0 – Unsigned Binary

1 – Binary Two's Complement Output.

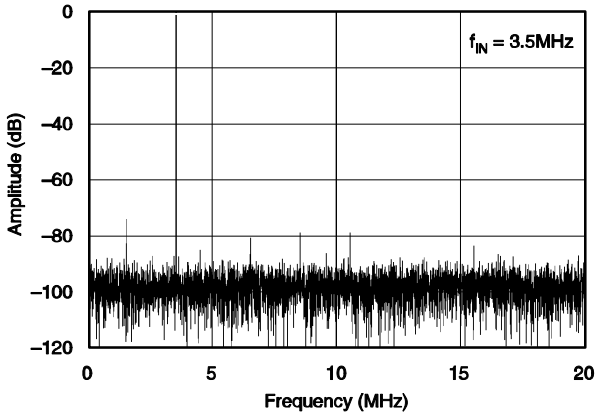
Table 2. PGA DB[0:4], 5–bit PGA gain code for channel A or B.

GAIN (dB)	PGx4	PGx3	PGx2	PGx1	PGx0
0	0	0	0	0	0
0.5606	0	0	0	0	1
1.1599	0	0	0	1	0
1.6643	0	0	0	1	1
2.3806	0	0	1	0	0
2.8703	0	0	1	0	1
3.5218	0	0	1	1	0
4.0824	0	0	1	1	1
4.6817	0	1	0	0	0
5.1630	0	1	0	0	1
5.8451	0	1	0	1	0
6.3903	0	1	0	1	1
6.9807	0	1	1	0	0
7.6040	0	1	1	0	1
8.0497	0	1	1	1	0
8.7712	0	1	1	1	1
9.2831	1	0	0	0	0
9.8272	1	0	0	0	1
10.4078	1	0	0	1	0
11.0301	1	0	0	1	1
11.7005	1	0	1	0	0
12.0412	1	0	1	0	1
12.7970	1	0	1	1	0
13.2208	1	0	1	1	1
14.0944	1	1	0	0	0
14.5400	1	1	0	0	1
15.0666	1	1	0	1	0
15.5630	1	1	0	1	1
16.1623	1	1	1	0	0
16.7229	1	1	1	0	1
17.4181	1	1	1	1	0
18.0618	1	1	1	1	1

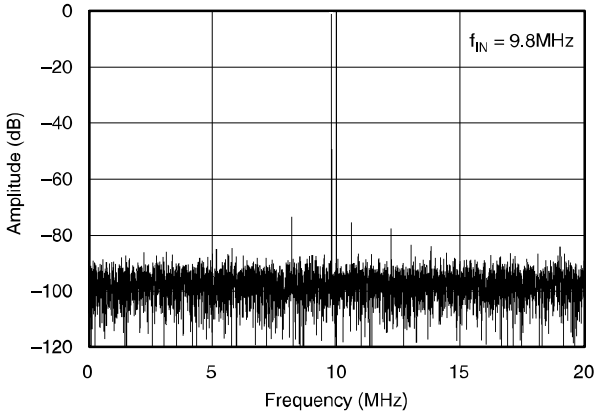
TYPICAL CHARACTERISTICS

At T_A = 25°C, AV_{DD} = DV_{DD} = DRV_{DD} = 3.3V, f_{IN} = –0.5dBFS, Internal Reference, f_{CLK} = 80MHz, f_S = 40MSPS, Differential Input Range = 2Vp-p, 25Ω series resistor, and 15pF differential capacitor at A/B+ and A/B– inputs, unless otherwise noted.

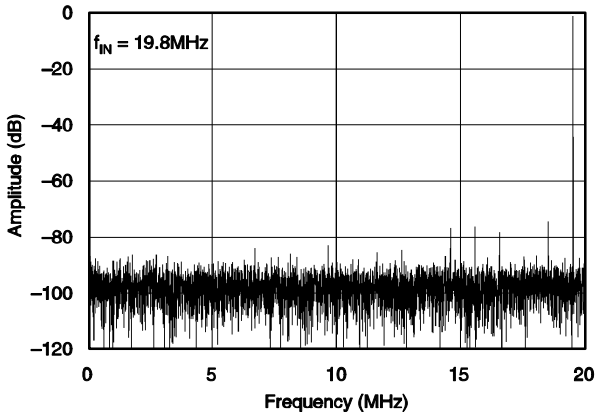
SPECTRAL PERFORMANCE



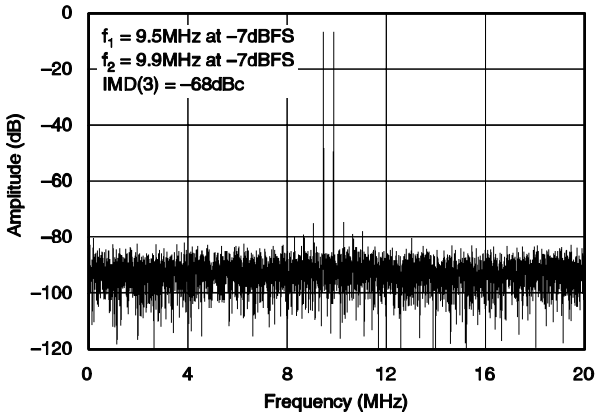
SPECTRAL PERFORMANCE



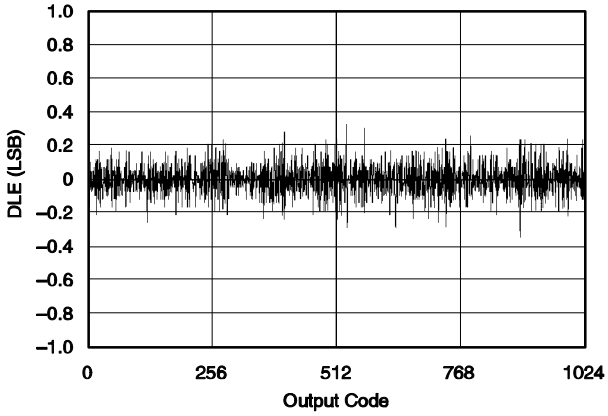
SPECTRAL PERFORMANCE



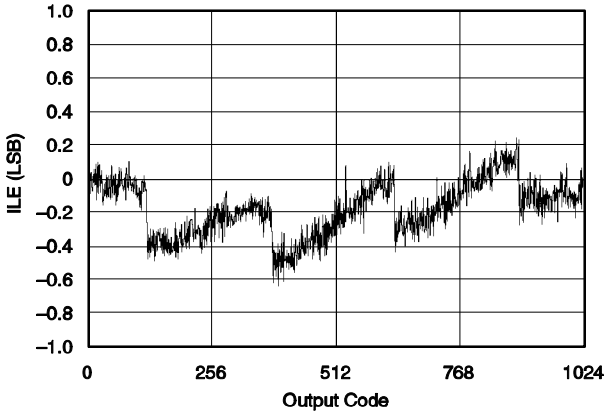
2-TONE INTERMODULATION DISTORTION



DIFFERENTIAL LINEARITY ERROR



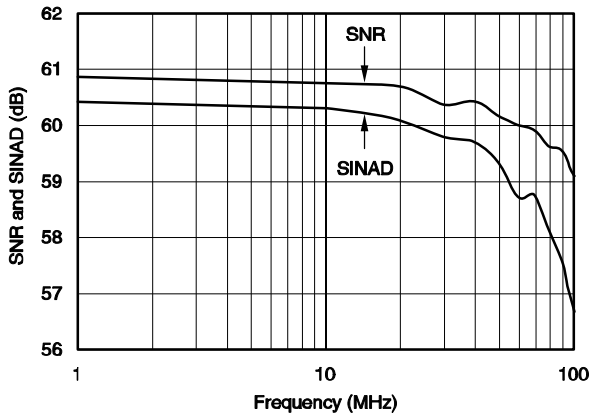
INTEGRAL LINEARITY ERROR



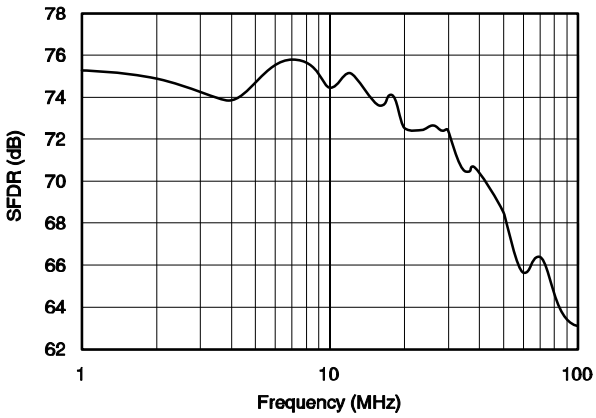
TYPICAL CHARACTERISTICS (Cont.)

At T_A = 25°C, AV_{DD} = DV_{DD} = DRV_{DD} = 3.3V, f_{IN} = –0.5dBFS, Internal Reference, f_{CLK} = 80MHz, f_S = 40MSPS, Differential Input Range = 2Vp-p, 25Ω series resistor, and 15pF differential capacitor at A/B+ and A/B– inputs, unless otherwise noted.

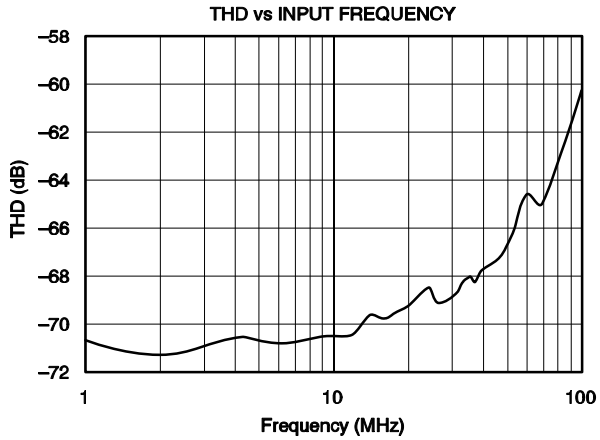
SNR AND SINAD vs INPUT FREQUENCY



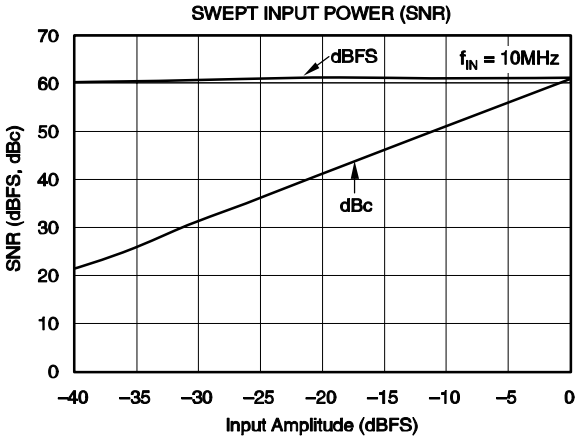
SFDR vs INPUT FREQUENCY



THD vs INPUT FREQUENCY



SWEPT INPUT POWER (SNR)



PRINCIPLE OF OPERATION

The ADS5204 implements a dual high-speed 10-bit, 40MSPS converter in a cost-effective CMOS process. The differential inputs on each channel are sampled simultaneously. Signal inputs are differential and the clock signal is single-ended. The clock signal is either 80MHz or 40MHz, depending on the device configuration set by the user. Powered from 3.3V, the dual-pipeline design architecture ensures low-power operation and 10-bit resolution. The digital inputs are 3.3V TTL/CMOS compatible. Internal voltage references are included for both bottom and top voltages. Alternatively, the user may apply externally generated reference voltages. In doing so, the input range can be modified to suit the application.

The ADC is a 5-stage pipelined ADC with four stages of fully-differential switched capacitor sub-ADC/MDAC pairs and a single sub-ADC in stage five. All stages deliver two bits of the final conversion result. A digital error correction is used to compensate for modest comparator offsets in the sub-ADCs.

SAMPLE-AND-HOLD AMPLIFIER

Figure 6 shows the internal SHA/SHPGA architecture. The circuit is balanced and fully differential for good supply noise rejection. The sampling circuit has been kept as simple as possible to obtain good performance for high-frequency input signals.

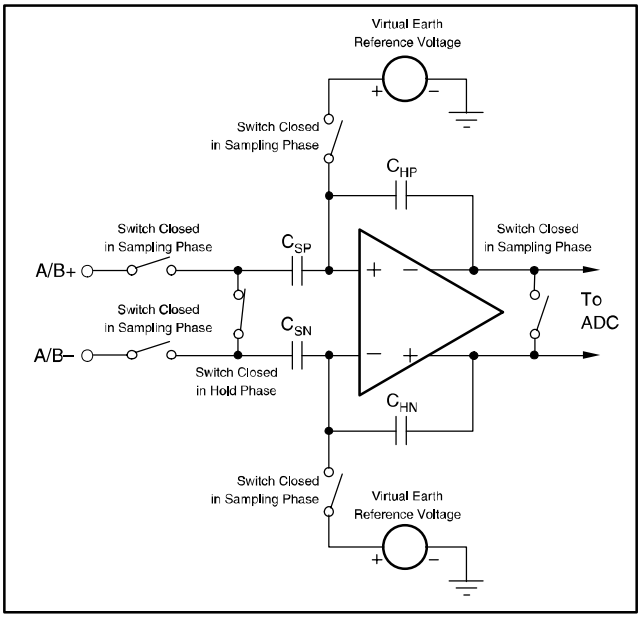


Figure 6. SHA/SHPGA Architecture.

The analog input signal is sampled on capacitors C_{SP} and C_{SN} while the internal device clock is LOW. The sampled voltage is transferred to capacitors C_{HP} and C_{HN} and held on these while the internal device clock is HIGH. The SHA can sample both single-ended and differential input signals.

The load presented to the AIN pin consists of the switched input sampling capacitor C_S (approximately 2pF) and its various stray capacitances. A simplified equivalent circuit for the switched capacitor input is shown in Figure 7. The switched capacitor circuit is modeled as a resistor R_{IN}. f_{CLK} is the clock frequency, which is 40MHz at full speed, and C_S is the sampling capacitor. The use of 25Ω series resistors and a differential 15pF capacitor at the A/B+ and A/B– inputs is recommended to reduce noise.

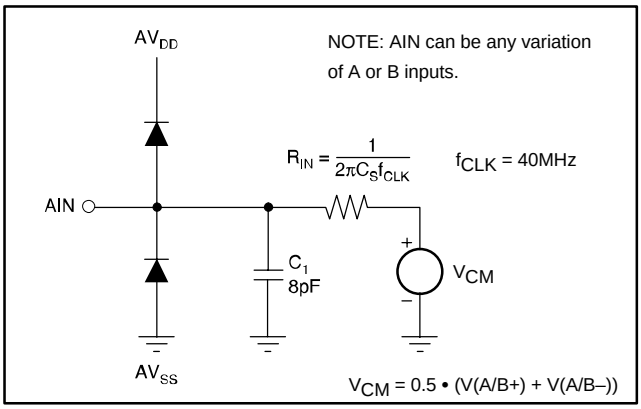


Figure 7. Equivalent Circuit for the Switched Capacitor Input.

ANALOG INPUT, DIFFERENTIAL CONNECTION

The analog input of the ADS5204 is a differential architecture that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection will deliver the best performance from the converter. The analog inputs must not go below AV_{SS} or above AV_{DD}. The inputs can be biased with any common-mode voltage provided that the minimum and maximum input voltages stay within the range AV_{SS} to AV_{DD}. It is recommended to bias the inputs with a common-mode voltage around $AV_{DD}/2$. This can be accomplished easily with the output voltage source CML, which is equal to $AV_{DD}/2$. CML is made available to the user to help simplify circuit design. This output voltage source is not designed to be a reference or to be loaded but makes an excellent DC bias source and stays well within the analog input common-mode voltage range over temperature.

Table 3 lists the digital outputs for the corresponding analog input voltages.

Table 3. Output Format for Differential Configuration

DIFFERENTIAL INPUT	
V_{IN} = (A/B+) – (A/B–), REFT – REFB = 1V, PGA = 0dB	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
V_{IN} = +1V	$3FF_H$
V_{IN} = 0	200_H
V_{IN} = –1V	000_H

DC-COUPLED DIFFERENTIAL ANALOG INPUT CIRCUIT

Driving the analog input differentially can be achieved in various ways. Figure 8 gives an example where a single-ended signal is converted into a differential signal by using a fully differential amplifier such as the THS4141. The input voltage applied to V_{OCM} of the THS4141 shifts the output signal into the desired common–mode level. V_{OCM} can be connected to CML of the ADS5204, the common-mode level is shifted to $AV_{DD}/2$.

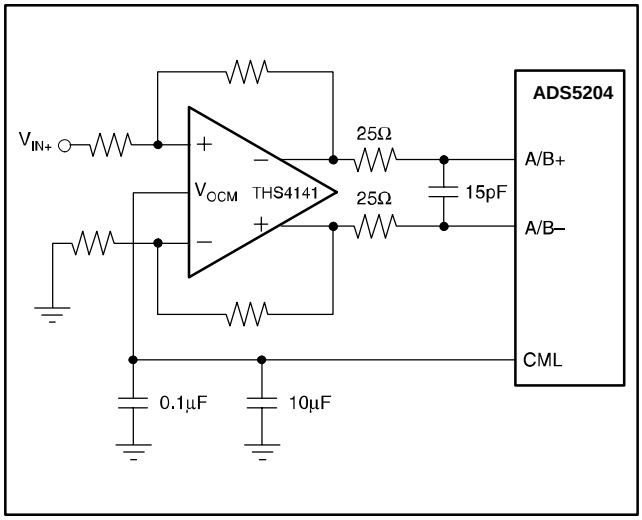


Figure 8. Single–Ended to Differential Conversion Using the THS4141.

AC-COUPLED DIFFERENTIAL ANALOG INPUT CIRCUIT

Driving the analog input differentially can be achieved by using a transformer coupling, as illustrated in Figure 9. The center tap of the transformer is connected to the voltage source CML, which sets the common–mode voltage to $AV_{DD}/2$. No buffer is required at the output of CML since the circuit is balanced and no current is drawn from CML.

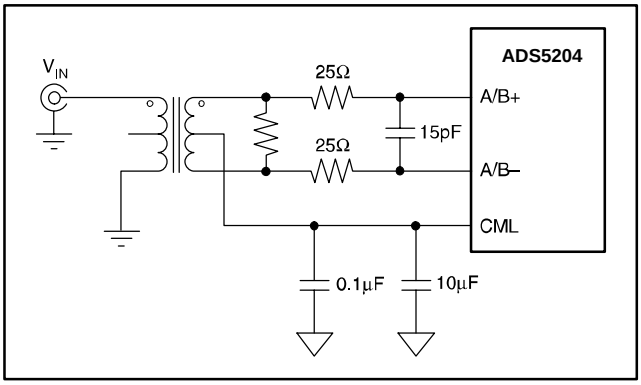


Figure 9. AC-Coupled Differential Input with Transformer.

ANALOG INPUT, SINGLE-ENDED CONFIGURATION

For a single-ended configuration, the input signal is applied to only one of the two inputs. The signal applied to the analog input must not go below AV_{SS} or above AV_{DD}. The inputs can be biased with any common-mode voltage provided that the minimum and maximum input voltage stays within the range AV_{SS} to AV_{DD}. It is recommended to bias the inputs with a common-mode voltage around $AV_{DD}/2$. This can be accomplished easily with the output voltage source CML, which is equal to $AV_{DD}/2$. An example for this is shown in Figure 10.

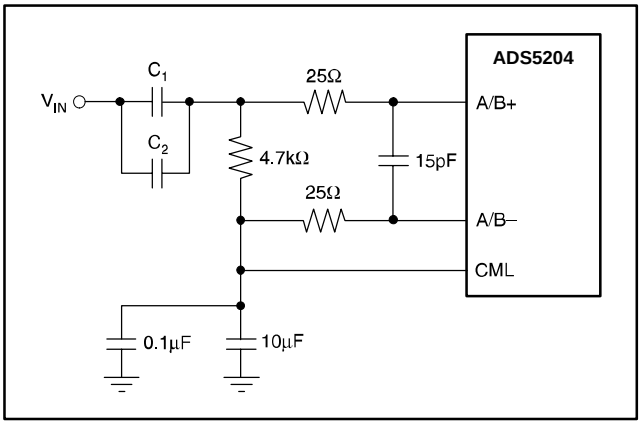


Figure 10. AC-Coupled, Single-Ended Configuration.

The signal amplitude to achieve full-scale is 2Vp-p. The signal, which is applied at A/B+ is centered at the bias voltage. The input A/B– is also centered at the bias voltage. The CML output is connected via a 4.7kΩ resistor to bias the input signal. There is a direct DC–coupling from CML to A/B– while this input is AC–decoupled through the 10µF and 0.1µF capacitors. The decoupling minimizes the coupling of A/B+ into the A/B– path.

Table 4 lists the digital outputs for the corresponding analog input voltages.

Table 4. Output Format for Single-Ended Configuration.

SINGLE–ENDED INPUT, REFT – REFB = 1V, PGA = 0dB	
ANALOG INPUT VOLTAGE	**DIGITAL OUTPUT CODE**
$V(A/B+) = V_{CML} + 1V$	$3FF_H$
$V(A/B+) = V_{CML}$	200_H
$V(A/B+) = V_{CML} – 1V$	000_H

REFERENCE TERMINALS

The ADS5204's input range is determined by the voltages on its REFB and REFT pins. The ADS5204 has an internal voltage reference generator that sets the ADC reference voltages REFB = 1V and REFT = 2V. The internal ADC references must be decoupled to the PCB AV_{SS} plane. The recommended decoupling scheme is shown in Figure 11. The common-mode reference voltages should be 1.5V for best ADC performance.

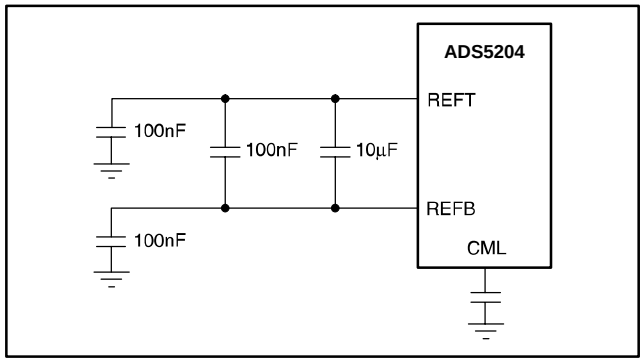


Figure 11. Recommended External Decoupling for the Internal ADC Reference.

External ADC references can also be chosen. The ADS5204 internal references must be disabled by tying PWDN_REF HIGH before applying the external reference sources to the REFT and REFB pins. The common-mode reference voltages should be 1.5V for best ADC performance.

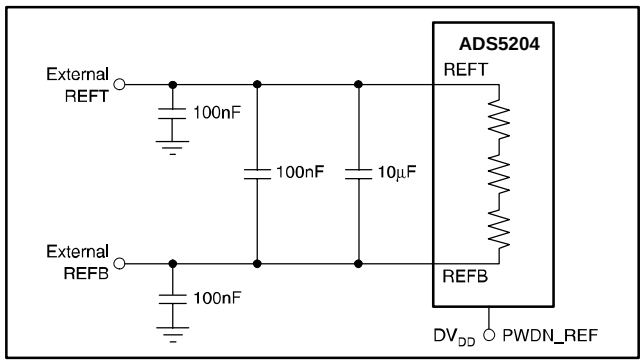


Figure 12. External ADC Reference Configuration.

DIGITAL INPUTS

Digital inputs are CLK, SCLK, SDI, $\overline{CS}$, STDBY, PWDN_REF, and $\overline{OE}$. These inputs don't have a pull-down resistor to ground, therefore, they should not be left floating.

The CLK signal at high frequencies should be considered as an 'analog' input. CLK should be referenced to AV_{DD} and AV_{SS} to reduce noise coupling from the digital logic. Overshoot/undershoot should be minimized by proper termination of the signal close to the ADS5204. An important cause of performance degradation for a high-speed ADC is clock jitter. Clock jitter causes uncertainty in the sampling instant of the ADC, in addition to the inherent uncertainty on the sampling instant caused by the part itself, as specified by its aperture jitter. There is a theoretical relationship between the frequency (f) and resolution (2^N) of a signal that needs to be sampled on one hand, and on the other hand the maximum amount of aperture error dt_{max} that is tolerable. It is given by the following relation:

$$dt_{max} = 1/[\pi\ f\ 2^{(N+1)}]$$

As an example, for a 10-bit converter with a 20MHz input, the jitter needs to be kept less than 7.8ps in order not to have changes in the LSB of the ADC output due to the total aperture error.

DIGITAL OUTPUTS

The output of ADS5204 is an unsigned binary or Binary Two's Complement code. Capacitive loading on the output should be kept as low as possible (a maximum loading of 10pF is recommended) to ensure best performance. Higher output loading causes higher dynamic output currents and can, therefore, increase noise coupling into the part's analog front end. To drive higher loads, the use of an output buffer is recommended.

When clocking output data from ADS5204, it is important to observe its timing relation to C_{OUT}. Please refer to the timing section for detailed information on the pipeline latency in the different modes.

For safest system timing, C_{OUT} and $\overline{C_{OUT}}$ should be used to latch the output data (see Figures 1 to 4). In Figure 4, $\overline{C_{OUT}}$ can be used by the receiving device to identify whether the data presently on the bus is from channel A or B.

LAYOUT, DECOUPLING, AND GROUNDING RULES

Proper grounding and layout of the PCB on which the ADS5204 is populated is essential to achieve the stated performance. It is advised to use separate analog and digital ground planes that are spliced underneath the IC. The ADS5204 has digital and analog pins on opposite sides of the package to make this easier. Since there is no connection internally between analog and digital grounds, they have to be joined on the PCB. It is advised to do this at one point in close proximity to the ADS5204.

As for power supplies, separate analog and digital supply pins are provided on the part (AV_{DD}/DV_{DD}). The supply to the digital output drivers is kept separate as well (DRV_{DD}). Lowering the voltage on this supply to 3.0V instead of the nominal 3.3V improves performance because of the lower switching noise caused by the output buffers.

Due to the high sampling rate and switched-capacitor architecture, the ADS5204 generates transients on the supply and reference lines. Proper decoupling of these lines is, therefore, essential.

SERIAL INTERFACE

A falling edge on $\overline{CS}$ enables the serial interface, allowing the 16-bit control register date to be shifted (MSB first) on subsequent falling edges of SCLK. The data is loaded into the control register on the first rising edge of SCLK after its 16th falling edge or $\overline{CS}$ rising, whichever occurs first. $\overline{CS}$ rising before 16 falling SCLK edges have been counted is an error and the control register will not be updated.

The maximum update rate is:

$$f_{UPDATEMAX} = \frac{f_{SCLK}}{16} = \frac{20MHz}{16} = 1.25MHz$$

NOTES

1. Integral Nonlinearity (INL)—Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full-scale. The point used as zero occurs ½LSB before the first code transition. The full-scale point is defined as a level ½LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.

2. Differential Nonlinearity (DNL)—An ideal ADC exhibits code transitions that are exactly 1LSB apart. DNL is the deviation from this ideal value. Therefore, this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., (last transition level – first transition level)/(2^n – 2)). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1LSB ensures no missing codes.

3. Zero and Full-Scale Error—Zero error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to ½LSB to the bottom reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

Full-scale error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that will switch the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5LSB from the top reference level. The voltage corresponding to 1LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

4. Analog Input Bandwidth—The analog input bandwidth is defined as the max. frequency of a 1dBFS input sine that can be applied to the device for which an extra 3dB attenuation is observed in the reconstructed output signal.

5. Output Timing—Output timing $t_{d(o)}$ is measured from the 1.5V level of the CLK input falling edge to the 10%/90% level of the digital output. The digital output load is not higher than 10pF. Output hold time $t_{h(o)}$ is measured from the 1.5V level of the C_{OUT} input rising edge to the 10%/90% level of the digital output. The digital output is load is not less than 2pF. Aperture delay $t_{d(A)}$ is measured from the 1.5V level of the CLK input to the actual sampling instant.

The $\overline{OE}$ signal is asynchronous. $\overline{OE}$ timing t_{dis} is measured from the $V_{IH(MIN)}$ level of $\overline{OE}$ to the high-impedance state of the output data. The digital output load is not higher than 10pF. $\overline{OE}$ timing t_{en} is measured from the $V_{IL(MAX)}$ level of $\overline{OE}$ to the instant when the output data reaches $V_{OH(min)}$ or $V_{OL(max)}$ output levels. The digital output load is not higher than 10pF.

6. Pipeline Delay (latency)—The number of clock cycles between conversion initiation on an input sample and the corresponding output data being made available from the ADC pipeline. Once the data pipeline is full, new valid output data is provided on every clock cycle. The first valid data is available on the output pins after the latency time plus the output delay time $t_{d(o)}$ through the digital output buffers. Note that a minimum $t_{d(o)}$ is not guaranteed because data can transition before or after a CLK edge. It is possible to use CLK for latching data, but at the risk of the prop delay varying over temperature, causing data to transition one CLK

cycle earlier or later. The recommended method is to use the latch signals C_{OUT} and $\overline{C_{OUT}}$ which are designed to provide reliable setup and hold times with respect to the data out.

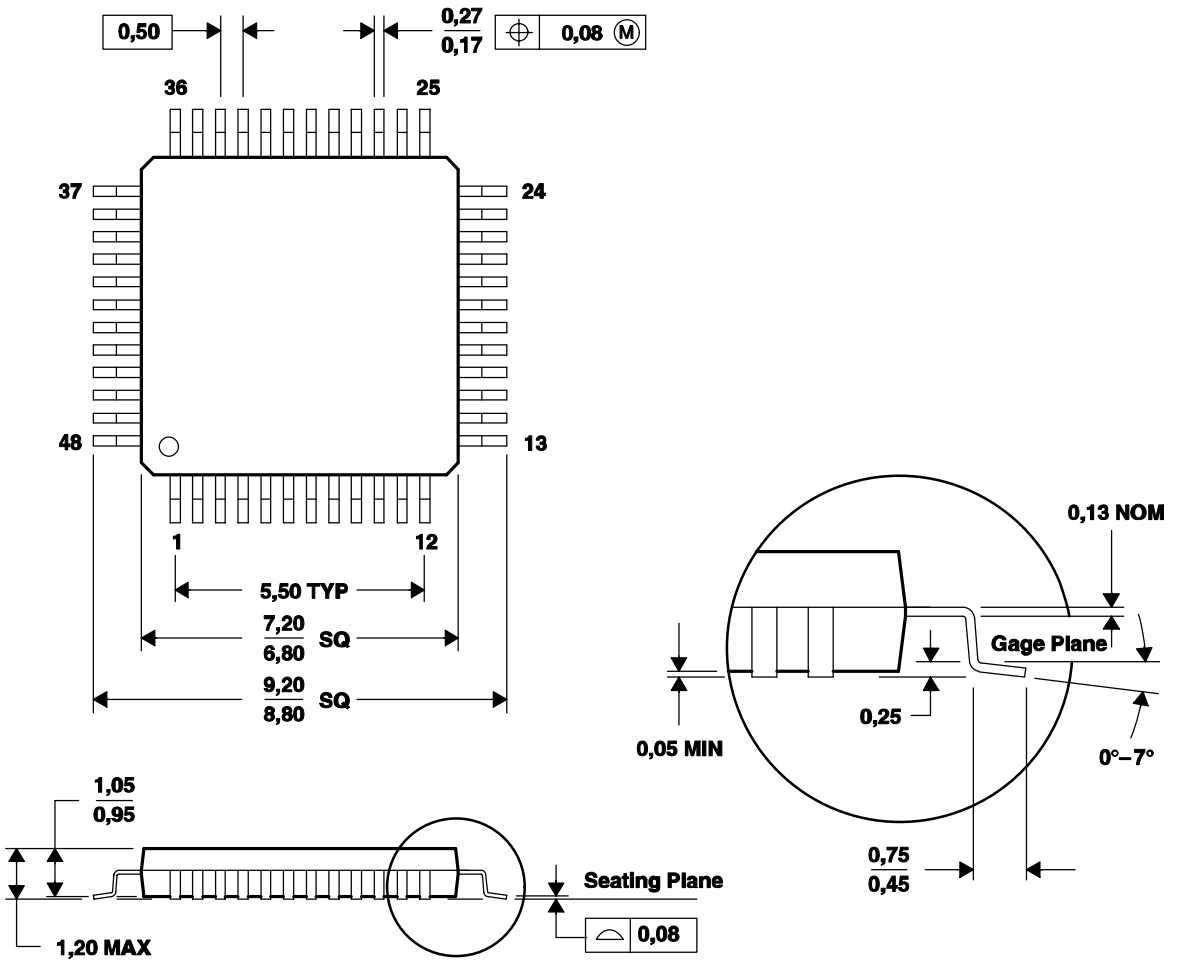
7. Wake-Up Time—Wake-up time is from the power-down state to accurate ADC samples being taken, and is specified for external reference sources applied to the device and an 80MHz clock applied at the time of release of STDBY. Cells that need to power up are the bandgap, bias generator, SHAs, and ADCs.

8. Power-Up Time—Power-up time is from the power-down state to accurate ADC samples being taken with an 80MHz clock applied at the time of release of STDBY. Cells that need to power up are the bandgap, internal reference circuit, bias generator, SHAs, and ADCs.

PACKAGE DRAWING

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265