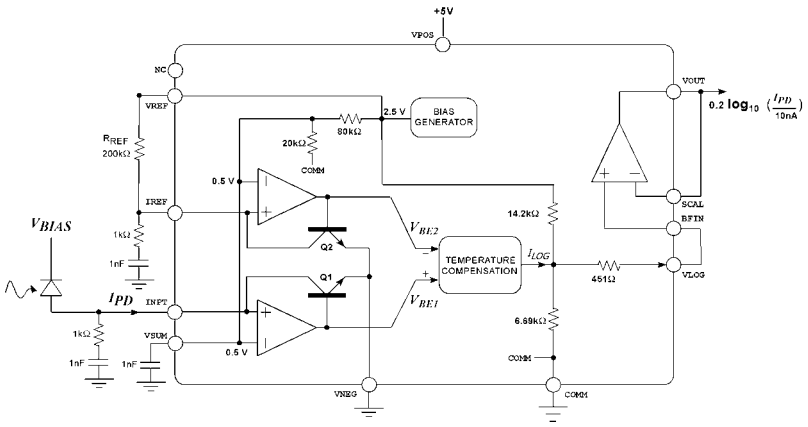
60dB-range (100nA-100μA) Low-Cost Logarithmic Converter

Preliminary Datasheet

ADL5306

FEATURES

Optimized for Fiber-Optic Photodiode Interfacing
Measures Current Over Three Decades
Law Conformance 0.3 dB from 100 nA to 100 μA
Single or Dual Supply Operation (±3 V to ±5.5 V total)
Full Log-Ratio Capabilities
Temperature Stable
Nominal slope of 10 mV/dB (200 mV/decade)
Nominal Intercept of 1 nA (set by external resistor)
Optional Adjustment of Slope and Intercept
Rapid Response Time for a given Current Level
Miniature 16 pin Chip Scale Package (LFCSP 3x3 mm)
Low Power: ~5mA Quiescent Current



APPLICATIONS

Low Cost Optical Power Measurement
Wide Range Baseband Logarithmic Compression
Measurement of Current- and Voltage-Ratios
Optical Absorbance Measurement

PRODUCT DESCRIPTION

The ADL5306 is a low cost micro-miniature logarithmic converter optimized for the determination of optical power in fiber-optic systems. The ADL5306 is a derivative of the popular AD8304 and AD8305 translinear logarithmic converters. The family of devices provide wide measurement dynamic range in a versatile and easily-used form. A single supply voltage of between 3 V and 5.5 V is adequate; dual supplies may optionally be used. The low quiescent current (typically 5 mA) permits use in battery-operated applications.

The input current I_{PD}, of 100 nA to 100 μA, applied to the **INPT** pin is the collector current of an optimally-scaled NPN transistor, which converts this current to a voltage (its V_{BE}) with a precise logarithmic relationship. A second such converter is used to handle the reference current, I_{REF}, applied to pin **IREF**. These input nodes are biased slightly above ground (0.5 V). This is generally acceptable for photodiode applications where the anode does not need to be grounded. Similarly, this bias voltage is easily accounted for in generating I_{REF}. The output of the logarithmic front-end is available at pin **VLOG**.

The basic logarithmic slope at this output is nominally 200 mV/decade (10 mV/dB). Thus, a 60-dB range corresponds to an output change of 600mV. When this voltage (or the buffer output) is applied to an ADC that permits an external reference voltage to be employed, the ADL5306's voltage reference output of 2.5 V at pin **VREF** can be used to improve the scaling accuracy. Suitable ADCs include the AD7810 (serial 10-bit), AD7823 (serial 8-bit) and the AD7813 (parallel, 8/10 bits). Other values of the logarithmic slope can be provided using a simple external resistor network.

The logarithmic intercept (also known as the reference current) is nominally positioned at 1 nA by the use of the externally generated current, I_{REF}, of 100 μA, provided by a 200 kΩ resistor connected between **VREF**, at 2.5 V, and the reference input **IREF**, at 0.5 V. The intercept can be adjusted over a narrow range by varying this resistor. The ADL5306 can also operate in a log-ratio mode, with limited accuracy, where the numerator current applied to **INPT** and the denominator current applied to **IREF**.

A buffer amplifier is provided for driving a substantial load, for use in raising the basic slope of 10 mV/dB to higher values, as a precision comparator (threshold detector), or in implementing low-pass filters. Its rail-to-rail output stage can swing to within 100 mV of the positive and negative supply rails, and its peak current-sourcing capacity is 25 mA.

It is a fundamental aspect of translinear logarithmic converters that the small-signal bandwidth falls as the current level diminishes, and the low-frequency noise-spectral density increases. At the 100 nA level, the bandwidth of the ADL5306 is about 100 kHz, and increases in proportion to I_{PD} up to a maximum value of about 10 MHz. Using the buffer amplifier, the increase in noise level at low currents can be addressed by using it to realize low-pass filters of up to three poles.

The ADL5306 is available in a 16 pin LFCSP package and specified for operation from –40°C to +85°C.

US Patents 4,604,532, 5,519,308 and others pending.

Rev. PrC 03/18/03

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 U.S.A.
Tel: 781/329-4700 **World Wide Web Site: http://www.analog.com**
Fax: 781/326-8703

ADL5306-SPECIFICATIONS

V_P = 5V, V_N = 0, T_A = 25°C, R_{REF} = 200kΩ, unless otherwise noted

Parameters	Conditions	Min	Typ	Max	Units
INPUT INTERFACE	Pin 4, **INPT**, Pin 3, **IREF**				
Specified Current Range, I_{PD}	Flows toward **INPT** pin	100n		100µ	A
Input Current Min/Max Limits	Flows toward **INPT** pin			10m	A
Reference Current, I_{REF}, Range	Flows toward **IREF** pin	100n		100µ	A
Summing Node Voltage	Internally pre-set; may be altered by user	0.46	0.5	0.54	V
Temperature Drift	–40°C < T_A < +85°C		0.015		mV/°C
Input Offset Voltage	V_{IN}-V_{SUM} , V_{IREF}-V_{SUM}	-20		20	mV
LOGARITHMIC OUTPUT	Pin 9, **VLOG**				
Logarithmic Slope		190	200	210	mV/dec
	–40°C < T_A < +85°C	185		215	mV/dec
Logarithmic Intercept[1]		TBD	1	TBD	nA
	–40°C < T_A < +85°C	TBD		TBD	nA
Law Conformance Error	100 nA < I_{PD} < 100 µA		0.1	TBD	dB
Wideband Noise[2]	I_{PD} > 1 µA		0.7		µV/√Hz
Small Signal Bandwidth[2]	I_{PD} > 1 µA		0.7		MHz
Maximum Output Voltage			1.7		V
Minimum Output Voltage	Limited by V_N=0 V		0.01		V
Output Resistance		4.375	5	5.625	kΩ
REFERENCE OUTPUT	Pin 2, **VREF**				
Voltage wrt Ground		2.435	2.5	2.565	V
	–40°C < T_A < +85°C	2.4		2.6	V
Maximum Output Current	Sourcing (grounded load)		20		mA
Incremental Output Resistance	Load current < 10 mA		2		Ω
OUTPUT BUFFER	Pin 10, **BFIN**; pin 11, **SCAL**; pin 12, **VOUT**				
Input Offset Voltage		-20		20	mV
Input Bias Current	Flowing out of pin 10 or 11		0.4		µA
Incremental Input Resistance			35		MΩ
Output Range	R_L = 1 kΩ to ground		V_P –0.1		V
Incremental Output Resistance	Load current < 10 mA		0.5		Ω
Peak Source/Sink Current			50		mA
Small Signal Bandwidth	GAIN = 1		TBD		MHz
Slew Rate	0.2V to 4.8V output swing		15		V/µs
POWER SUPPLY	Pins 8, **VPOS**; pin 6, **VNEG**				
Positive Supply Voltage	($V_P - V_N$) ≤ 11 V	3	5	5.5	V
Quiescent Current			5.4	6.5	mA
Negative Supply Voltage (Optional)	($V_P - V_N$) ≤ 11 V	-5.5	0		V

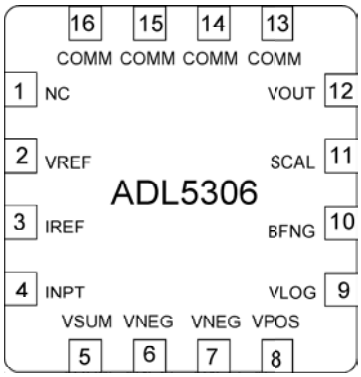
Notes

1) Other values of logarithmic intercept can be achieved by adjustment of R_{REF}
2) Output Noise and Incremental Bandwidth are functions of Input Current, measure using output buffer connected for GAIN = 1.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $V_P - V_N$…..……..……..…...12 V
Input Current ……....20mA
Internal Power Dissipation …. ……..…... TBD
θ_{JA} ……..…..…. 135°C/W
Maximum Junction Temperature …..…….…….....+125°C
Operating Temperature Range ..…….…….-40° C to +85°C
Storage Temperature Range ……....-65° C to +150°C
Lead Temperature Range (Soldering 60 sec) ……... +300°C

***Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**



Pin Function Descriptions

Pin	Name	Function
1	**NC**	N/A
2	**VREF**	Reference output voltage of 2.5 V.
3	**IREF**	Accepts (sinks) reference current, I_{REF}.
4	**INPT**	Accepts (sinks) photodiode current I_{PD}. Usually connected to photodiode anode such that photo-current flows into **INPT**.
5	**VSUM**	Guard Pin. Used to shield the **INPT** current line and for optional adjustment of the **INPT** and **IREF** node potential.
6,7	**VNEG**	Optional Negative Supply, V_N (this pin is usually grounded; for details of usage see APPLICATIONS).
8	**VPOS**	Positive Supply, ($V_P - V_N$) ≤ 11V.
9	**VLOG**	Output of the logarithmic front-end.
10	**BFIN**	Buffer Amplifier non-inverting input.
11	**SCAL**	Buffer Amplifier inverting input.
12	**VOUT**	Buffer Output.
13,14, 15, 16	**COMM**	Analog Ground.

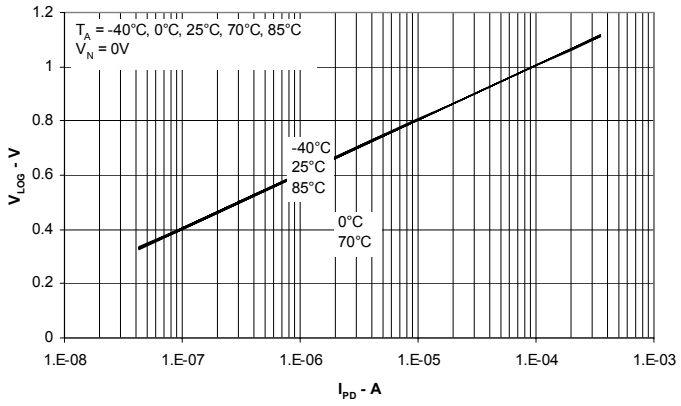
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8305 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy [>250 V HBM] electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

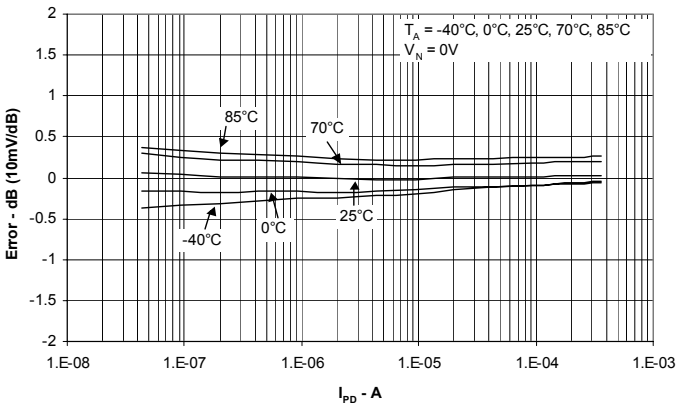
ORDERING GUIDE

Model	Temp. Range	Package Description	Package Option
ADL5306ACP	-40 °C to +85 °C	16-Lead LFCSP	CP-16
ADL5306ACP-REEL7		7" Tape and Reel	
ADL5306-EVAL		Evaluation Board	

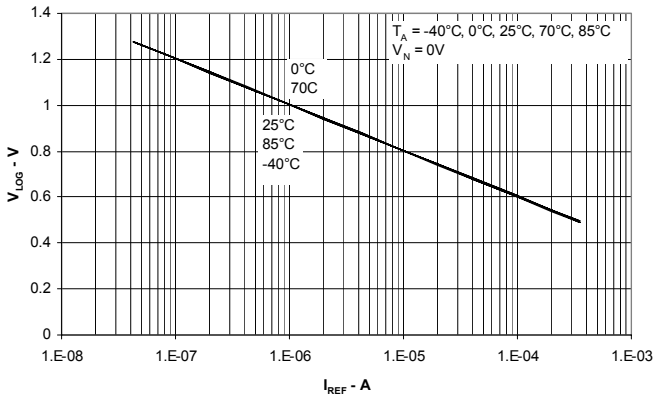
Typical Performance Characteristics (V_P = 5V, V_N = 0V, R_{REF} = 200kΩ, T_A = 25°C, unless noted)



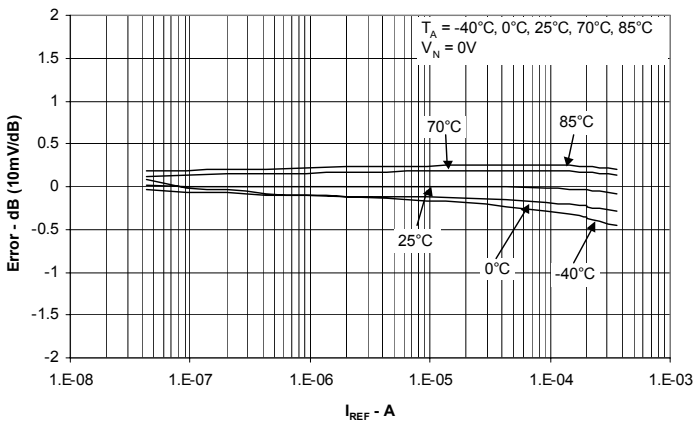
TPC 1. V_{LOG} vs. I_{PD} for Multiple Temperatures



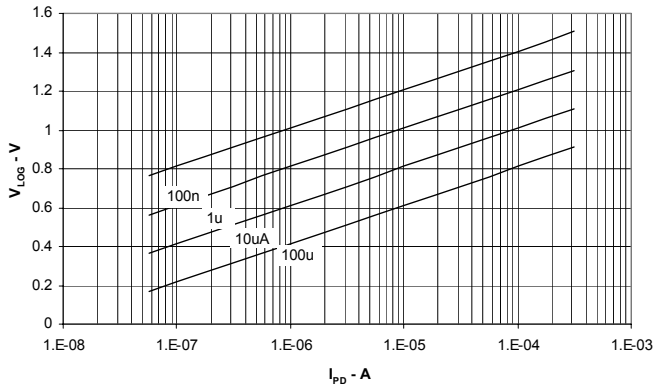
TPC 4. Law Conformance Error vs. I_{PD} (at I_{REF} = 10uA) for Multiple Temperatures, Normalized to 25°C



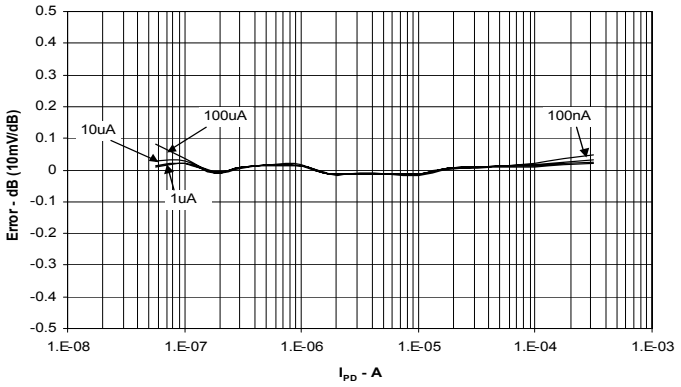
TPC 2. V_{LOG} vs. I_{REF} for Multiple Temperatures



TPC 5. Law Conformance Error vs. I_{REF} (at I_{PD} = 10uA) for Multiple Temperatures, Normalized to 25°C



TPC 3. V_{LOG} vs. I_{PD} for Multiple Values of I_{REF} (Decade Steps from 10 nA to 1 mA)



TPC 6. Law Conformance Error vs. I_{PD} for Multiple Values of I_{REF} (Decade Steps from 10 nA to 1 mA)

GENERAL STRUCTURE

The ADL5306 addresses a wide variety of interfacing conditions to meet the needs of fiber-optic supervisory systems, and will also be useful in many non-optical applications. These notes explain the structure of this unique style of translinear log amp. Figure 1 is a simplified schematic showing the key elements.

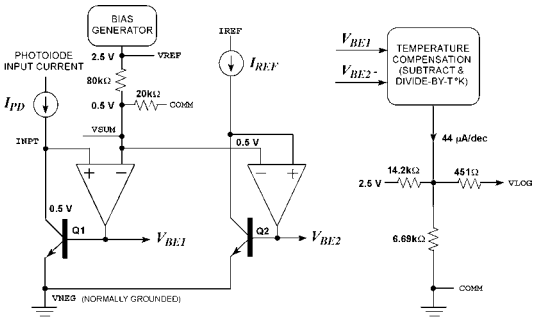


Figure 1: Simplified Schematic

The photodiode current I_{PD} is received at pin **INPT**. The voltage at this node is essentially equal to that on the two adjacent guard pins, **VSUM** and **IREF**, due to the low offset voltage of the JFET op amp. Transistor Q1 converts the input current I_{PD} to a corresponding logarithmic voltage, as shown in Equation (1). A finite positive value of V_{SUM} is needed to bias the collector of Q1, for the usual case of a single supply voltage. This is internally set to 0.5 V, that is, one fifth of the reference voltage of 2.5 V appearing on pin **VREF**. The resistance at the **VSUM** pin is nominally 16 kΩ; this voltage is not intended as a general bias source.

The ADL5306 also supports the use of an optional negative supply voltage, V_N, at pin **VNEG**. When V_N is –0.5 V or more negative, **VSUM** may be connected to ground; thus **INPT** and **IREF** assume this potential. This allows operation as a voltage-input logarithmic converter by the inclusion of a series resistor at either or both inputs. Note that the resistor setting I_{REF} will need to be adjusted to maintain the intercept value. It should also be noted that the collector-emitter voltages of Q1 and Q2 are now the full V_N, and effects due to self-heating will cause errors at large input currents.

The input-dependent V_{BE1} of Q1 is compared with the reference V_{BE2} of a second transistor, Q2, operating at I_{REF} . This is generated externally, to a recommended value of 10 µA. However, other values over a several-decades range can be used with a slight degradation in law conformance (see TPC1).

Theory

The base-emitter voltage of a BJT (bipolar junction transistor) can be expressed by the following equation, which immediately shows its basic logarithmic nature:

$$V_{BE} = \text{kT/q } \ln(I_C/I_S) \qquad (1)$$

where I_C is its collector current, I_S is a scaling current, typically only 10^{-17}A, and kT/q is the thermal voltage, proportional to absolute temperature (PTAT) and is 25.85mV at 300K. The current I_S is never precisely defined, and it exhibits an even stronger temperature dependence, varying by a factor of roughly a billion between -35°C and +85°C. Thus, to make use of the BJT as an accurate logarithmic element, both of these temperature-dependencies must be eliminated.

The difference between the base-emitter voltages of a matched pair of BJTs, one operating at the photodiode current I_{PD} and the second operating at a reference current I_{REF} can be written as

$$\begin{aligned} V_{BE1} - V_{BE2} &= \text{kT/q } \ln(I_{PD}/I_S) - \text{kT/q } \ln(I_{REF}/I_S) \\ &= \ln(10)\ \text{kT/q } \log_{10}(I_{PD}/I_{REF}) \qquad (2) \\ &= 59.5\text{mV } \log_{10}(I_{PD}/I_{REF}) \ \ (\text{T} = 300\text{K}) \end{aligned}$$

The uncertain and temperature-dependent saturation current I_S which appears in Equation (1) has thus been eliminated. To eliminate the temperature variation of kT/q this difference voltage is processed by what is essentially an analog divider. Effectively, it puts a variable under equation (2). The output of this process, which also involves a conversion from voltage-mode to current-mode, is an intermediate, temperature-corrected current:

$$I_{LOG} = I_Y \log_{10}(I_{PD}/I_{REF}) \qquad (3)$$

where I_Y is an accurate, temperature-stable *scaling current* which determines the slope of the function (the change in current per decade). For the ADL5306, I_Y is 44 µA, resulting in a temperature-independent slope of 44 µA/decade, for all values of I_{PD} and I_{REF} . This current is subsequently converted back to a voltage-mode output, V_{LOG}, scaled 200mV/decade.

It is apparent that this output should be zero for $I_{PD} = I_{REF}$, and would need to swing negative for smaller values of input current. To avoid this, I_{REF} would need to be as small as the smallest value of I_{PD}. However, it is impractical to use such a small reference current as 1 nA. Accordingly, an internal offset voltage is added to V_{LOG} to shift it upward by 0.8 V. This has the effect of moving the intercept to the left by 4 decades, from 10 µA to 1 nA:

$$I_{LOG} = I_Y \log_{10}(I_{PD}/I_{INTC}) \qquad (4)$$

where I_{INTC} is the operational value of the intercept current. Since values of $I_{PD} < I_{INTC}$ result in a negative V_{LOG}, a negative supply of sufficient value is required to accommodate this situation (discussed later).

The voltage V_{LOG} is generated by applying I_{LOG} to an internal resistance of 4.55 kΩ, formed by the parallel combination of a 6.69 kΩ resistor to ground and the 14.2 kΩ resistor to the internal 2.5V reference. The output current I_{LOG} generates a voltage at the **VLOG** pin of

$$V_{LOG} = I_{LOG} \times 4.55\ \text{k}\Omega$$
$$= 44\ \mu\text{A} \times 4.55\ \text{k}\Omega \times \log_{10}(I_{PD}/I_{REF})$$
$$= V_Y \log_{10}(I_{PD}/I_{REF}) \quad (5)$$

where V_Y = 200 mV/decade, or 10 mV/dB. Note that any resistive loading on **VLOG** will lower this slope, and also result in an overall scaling uncertainty, due to the variability of the on-chip resistors. Consequently, this practice is not recommended.

V_{LOG} may also swing below ground when dual supplies (V_P and V_N) are used. When V_N = −0.5V or larger, the input pins **INPT** and **IREF** may now be positioned at ground level by simply grounding **VSUM**.

Managing Intercept and Slope

As noted above, this introduces an accurate offset voltage of +0.8V at the **VLOG** pin, equivalent to four decades, resulting in a logarithmic transfer function that can be written as

$$V_{LOG} = V_Y \log_{10}(10^4 \times I_{PD}/I_{REF})$$
$$= V_Y \log_{10}(I_{PD}/I_{INTC}) \quad (6)$$
$$\text{where } I_{INTC} = I_{REF}/10^4.$$

Thus, the effective intercept current I_{INTC} is only one ten-thousandth of I_{REF}, corresponding to 10 nA when using the recommended value of I_{REF} = 100 μA.

The slope can be reduced by attaching a resistor to the **VLOG** pin. This is strongly discouraged, in view of the fact that the on-chip resistors will not ratio correctly to the added resistance. Also, it is rare that one would wish to lower the basic slope of 10 mV/dB, and if this is needed, it should be effected at the low-impedance output of the buffer, which is provided to avoid such miscalibration and also allow higher slopes to be used.

The ADL5306 buffer is essentially an uncommitted op- amp with rail-to-rail output swing, good load-driving capabilities and a unity-gain bandwidth of >20 MHz. In addition to allowing the introduction of gain, using standard feedback networks, and thereby increase the slope voltage, V_Y, the buffer can be used to implement multi-pole low-pass filters, threshold detectors, and a variety of other functions. Further details of these can be found in the Data Sheet for the AD8304.

Response Time and Noise Considerations

The response time and output noise of the ADL5306 are fundamentally a function of the signal current I_{PD}. For small currents the bandwidth is proportional to I_{PD}. The output low-frequency voltage-noise spectral-density is a function of I_{PD} and also increases for small values of I_{REF}. Details of the noise and bandwidth performance of translinear log amps can be found in the AD8304 Data Sheet.

APPLICATIONS

The ADL5306 is easy to use in optical supervisory systems and in similar situations where a wide-ranging current is to be converted to its logarithmic equivalent, that is, represented in decibel terms. Basic connections for measuring a single current input are shown in Figure 2, which also includes various non-essential components, as will be explained.

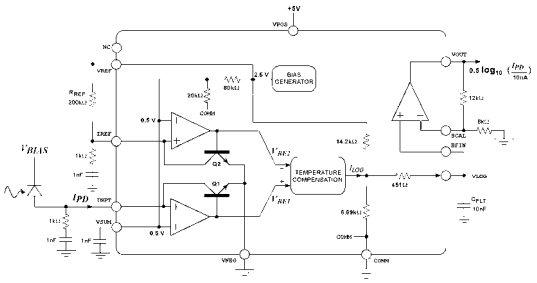


Figure 2: Basic Connections for Fixed Intercept Use

The 2 V difference in voltage between the **VREF** and **INPT** pins in conjunction with the external 200 kΩ resistor R_{REF} provide a reference current I_{REF} of 100 μA into pin **IREF**. The internal reference raises the voltage at **VLOG** by 0.8V, effectively lowering the intercept current I_{INTC} by a factor of 10^4, to position it at 1 nA. Any temperature variation in R_{REF} must be taken into account when estimating the stability of the intercept. Also, the overall noise will increase when using very low values of I_{REF}. In fixed-intercept applications, there is little benefit in using a large reference current, since this only compresses the low-current end of the dynamic range, when operated from a single supply, here shown as 5 V. The capacitor between **VSUM** and ground is recommended to minimize the noise on this node and help to provide a clean reference current.

Since the basic scaling at **VLOG** is 0.2 V/dec, and thus a swing of 4V at the buffer output would correspond to 20 decades, it will often be useful to raise the slope, to make better use of the rail-to-rail voltage range. For illustrative purposes, the circuit in Figure 2 provides an overall slope of 0.5 V/dec (25 mV/dB). Thus, using I_{REF} = 100 μA, V_{LOG} runs from 0.2 V at I_{PD} = 100 nA to 0.8 V at I_{PD} = 100uA while the buffer output runs from 0.5 to 2.0 V, corresponding to a dynamic range of 60 dB (electrical, that is, 30 dB optical power).

The optional capacitor from **VLOG** to ground forms a single-pole low-pass filter in combination with the 4.55-kΩ resistance at this pin. For example, using a C_{FLT} of 10 nF the −3dB corner frequency is 3.2 kHz. Such filtering is useful in minimizing the output noise, particularly when I_{PD} is small. Multi-pole filters are more effective in reducing the total noise; examples are provided in the AD8304 Data Sheet.

The dynamic response of this overall input system is influenced by the external RC networks connected from the two inputs (**INPT**, **IREF**) to ground. These

are required to stabilize the input systems over the full current range. The bandwidth changes with the input current due to the widely varying *pole* frequency. The RC network adds a *zero* to the input system to ensure stability over the full range of input current levels. The network values shown in Figure 2 will usually suffice, but some experimentation may be necessary when the photodiode capacitance is high.

Although the two current inputs are similar, some care is needed to operate the reference input at extremes of current (<100nA) and temperature (<0°C). Modifying the RC network to 4.7nF and 2kΩ will allow operation to -40°C at 10nA. By inspecting the transient response to perturbations in I_{REF} at representative current levels, the capacitor value can be adjusted to provide fast rise and fall times with acceptable settling. To fine tune the network *zero*, the resistor value should be adjusted.

USING A NEGATIVE SUPPLY

Most applications of the ADL5306 will require only a single supply of 3.0 V to 5.5 V. However, to provide further versatility, dual supplies may be employed, as illustrated in Figure 4.

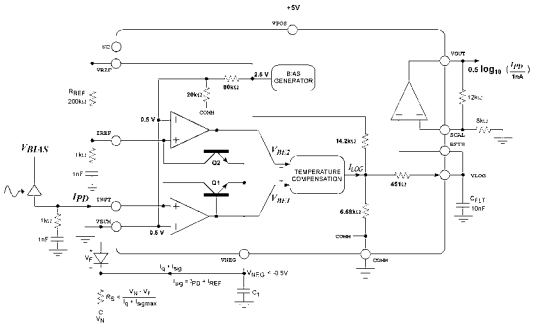
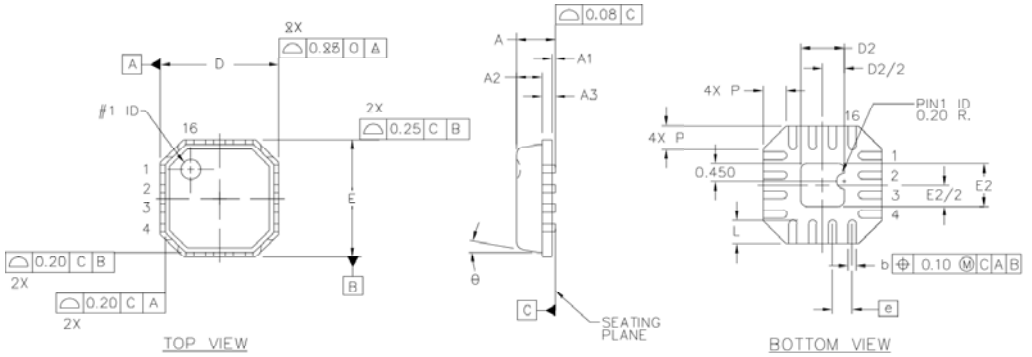


Figure 4: Negative Supply Application

The use of a negative supply, V_N, allows the summing node to be placed at ground level whenever the input transistor (Q1 in Figure 1) has a sufficiently negative bias on its emitter. When $V_N = –0.5$ V, the V_{CE} of Q1 and Q2 will be the same as for the default case when **VSUM** is grounded. This bias need not be accurate, and a poorly defined source can be used. The source does however need to be able to support the quiescent current as well as the **INPT** and **IREF** signal current. For example, it may be convenient to utilize a forward-biased junction voltage of about 0.7V or a Schottky barrier voltage of a little over 0.5 V. With the summing node at ground, the ADL5306 may now be used as a voltage-input log amp, at either the numerator input **INPT** or the denominator input **IREF** by inserting a suitably scaled resistor from the voltage source to the relevant pin. The overall accuracy for small input voltages is limited by the voltage offset at the inputs of the JFET op amps.

The use of a negative supply also allows the output to swing below ground, thereby allowing the intercept to correspond to a midrange value of I_{PD}. However, the voltage V_{LOG} remains referenced to the **ACOM** pin, and while it does not swing negative for default operating conditions, it is free to do so. Thus, adding a resistor from **VLOG** to the negative supply lowers all values of V_{LOG}, which raises the intercept. The disadvantage of this method is that the slope is reduced by the shunting of the external resistor, and the poorly-defined ratio of on-chip and off-chip resistances causes errors in both the slope and the intercept. A more accurate method for repositioning the intercept is described below.

OUTLINE DIMENSIONS



Dim	Min.	Nom.	Max
A	0.80	0.85	1.00
A1	0.00	0.01	0.05
A2		0.65	0.80
A3		0.20 REF	
θ	0°		12°

Dim	Min.	Nom.	Max
D	2.75	3.00	3.25
D1	2.55	2.75	2.95
D2	1.15	1.30	1.45
E	2.75	3.00	3.25
E1	2.55	2.75	2.95
E2	1.15	1.30	1.45
L	0.30	0.40	0.50

Dim	Min.	Nom.	Max
b	0.18	0.23	0.30
e		0.50 BSC	
P	0.24	0.42	0.60