

General Description

The AAT8541 is a low threshold MOSFET designed for the battery, cell phone, and PDA markets. Using AnalogicTech™'s ultra high density MOSFET process and space saving small outline J-lead package, performance superior to that normally found in a TSOP-6 footprint has been squeezed into the footprint of a SC70 package.

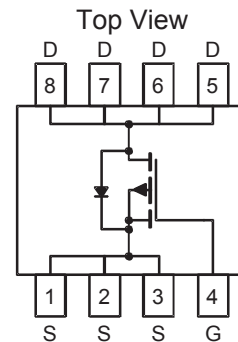
Features

- $V_{DS(MAX)} = -20V$
- $I_{D(MAX)}^1 = -3.0A @ 25^{\circ}C$
- Low $R_{DS(ON)}$:
 - $100\ m\Omega @ V_{GS} = -4.5V$
 - $175\ m\Omega @ V_{GS} = -2.5V$

Applications

- Battery Packs
- Cellular & Cordless Telephones
- Battery-powered portable equipment

SC70JW-8 Package



Absolute Maximum Ratings ($T_A = 25^{\circ}C$ unless otherwise noted)

Symbol	Description	Value	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 12	
I_D	Continuous Drain Current @ $T_J = 150^{\circ}C$ ¹	$T_A = 25^{\circ}C$: ± 3.0 $T_A = 70^{\circ}C$: ± 2.4	A
I_{DM}	Pulsed Drain Current ²	± 12	
I_S	Continuous Source Current (Source-Drain Diode) ¹	-1.1	
P_D	Maximum Power Dissipation ¹	$T_A = 25^{\circ}C$: 1.5 $T_A = 70^{\circ}C$: 0.9	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	

Thermal Characteristics

Symbol	Description	Typ	Max	Units
$R_{\theta JA}$	Junction-to-Ambient steady state ¹	107	130	$^{\circ}C/W$
$R_{\theta JA2}$	Junction-to-Ambient $t < 5$ seconds ¹	68	83	$^{\circ}C/W$
$R_{\theta JF}$	Junction-to-Foot ¹	40	48	$^{\circ}C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Description	Conditions	Min	Typ	Max	Units
DC Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250μA	-20			V
R _{DS(ON)}	Drain-Source ON-Resistance ²	V _{GS} =-4.5V, I _D =-3.0A		80	100	mΩ
		V _{GS} =-2.5V, I _D =-2.3A		140	175	
I _{D(ON)}	On-State Drain Current ²	V _{GS} =-4.5V, V _{DS} =-5V (Pulsed)	-12			A
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250μA	-0.6			V
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±12V, V _{DS} =0V			±100	nA
I _{DSS}	Drain Source Leakage Current	V _{GS} =0V, V _{DS} =-20V			-1	μA
		V _{GS} =0V, V _{DS} =-16V, T _J =70°C ³			-5	
g _{fs}	Forward Transconductance ²	V _{DS} =-5V, I _D =-3.0A		4		S
Dynamic Characteristics ³						
Q _G	Total Gate Charge	V _{DS} =-15V, R _D =5Ω, V _{GS} =-4.5V		4.2		nC
Q _{GS}	Gate-Source Charge	V _{DS} =-15V, R _D =5Ω, V _{GS} =-4.5V		0.7		
Q _{GD}	Gate-Drain Charge	V _{DS} =-15V, R _D =5Ω, V _{GS} =-4.5V		1.7		
t _{D(ON)}	Turn-ON Delay	V _{DS} =-15V, R _D =5Ω, V _{GS} =-4.5V, R _G =6Ω		TBD		ns
t _R	Turn-ON Rise Time	V _{DS} =-15V, R _D =5Ω, V _{GS} =-4.5V, R _G =6Ω		TBD		
t _{D(OFF)}	Turn-OFF Delay	V _{DS} =-15V, R _D =5Ω, V _{GS} =-4.5V, R _G =6Ω		TBD		
t _F	Turn-OFF Fall Time	V _{DS} =-15V, R _D =5Ω, V _{GS} =-4.5V, R _G =6Ω		TBD		
Source-Drain Diode Characteristics						
V _{SD}	Source-Drain Forward Voltage ²	V _{GS} =0, I _S =-3.0A			-1.3	V
I _S	Continuous Diode Current ¹				-1.1	A

Note 1: Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5 second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design, however $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

Note 2: Pulse test: Pulse Width = 300 μs

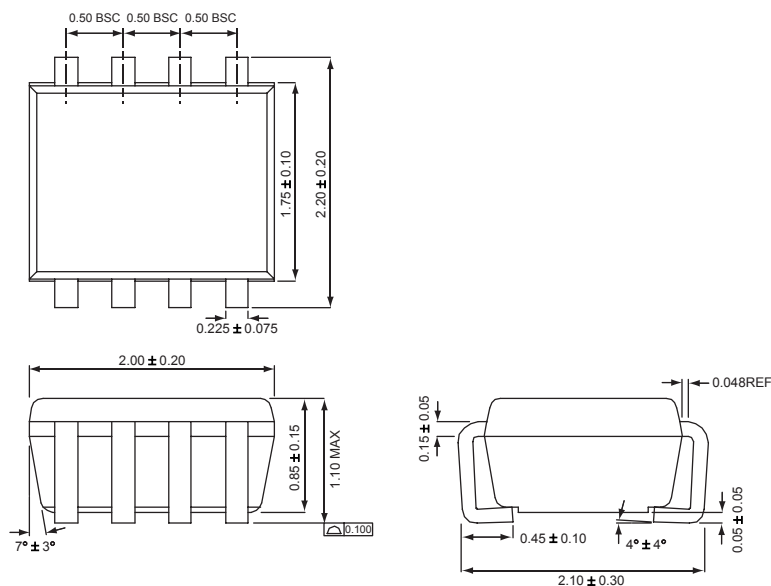
Note 3: Guaranteed by design. Not subject to production testing.

Ordering Information

Package	Marking	Part Number (Tape and Reel)
SC70JW-8		AAT8541IJS-T1

Package Information

SC70JW-8



All dimensions in millimeters.

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