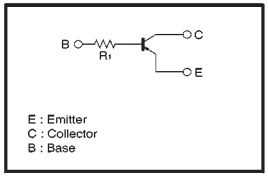
Digital transistors (built-in resistor)

DTA115TE / DTA115TUA / DTA115TKA / DTA115TSA

●**Features**

1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors.
2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input, and parasitic effects are almost completely eliminated.
3) Only the on / off conditions need to be set for operation, making device design easy.
4) Higher mounting densities can be achieved.

●**Circuit schematic**



E : Emitter
C : Collector
B : Base

●**Absolute maximum ratings** (Ta=25℃)

Parameter		Symbol	Limits	Unit
Collector-base voltage		V_{CBO}	−50	V
Collector-emitter voltage		V_{CEO}	−50	V
Emitter-base voltage		V_{EBO}	−5	V
Collector current		I_C	−100	mA
Collector power dissipation	DTA115TE	Pc	150	mW
	DTA115TUA / DTA115TKA		200	
	DTA115TSA		300	
Junction temperature		Tj	150	℃
Storage temperature		Tstg	−55~+150	℃

●**Package, marking, and packaging specifications**

Part No.	DTA115TE	DTA115TUA	DTA115TKA	DTA115TSA
Package	EMT3	UMT3	SMT3	SPT
Marking	99	99	99	—
Packaging code	TL	T106	T146	TP
Basic ordering unit (pieces)	3000	3000	3000	5000

●**Electrical characteristics** (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	−50	—	—	V	I_C=−50 μA
Collector-emitter breakdown voltage	BV_{CEO}	−50	—	—	V	I_C=−1mA
Emitter-base breakdown voltage	BV_{EBO}	−5	—	—	V	I_E=−50 μA
Collector cutoff current	I_{CBO}	—	—	−0.5	μA	V_{CB}=−50V
Emitter cutoff current	I_{EBO}	—	—	−0.5	μA	V_{EB}=−4V
Collector-emitter saturation voltage	$V_{CE(sat)}$	—	—	−0.3	V	I_C/I_B=−1mA/−0.1mA
DC current transfer ratio	h_{FE}	100	250	600	—	I_C=−1mA , V_{CE}=−5V
Input resistance	R_1	70	100	130	kΩ	—
Transition frequency	f_T	—	250	—	MHz	V_{CE}=−10V , I_E=5mA , f=100MHz *

* Transition frequency of the device.

(96-259-A115T)

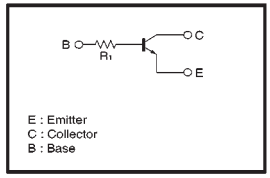
Digital transistors (built-in resistor)

DTC115TUA / DTC115TKA / DTC115TSA

●**Features**

1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors.
2) The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input, and parasitic effects are almost completely eliminated.
3) Only the on / off conditions need to be set for operation, making device design easy.
4) Higher mounting densities can be achieved.

●**Circuit schematic**



E : Emitter
C : Collector
B : Base

●**Absolute maximum ratings** (Ta=25℃)

Parameter		Symbol	Limits	Unit
Collector-base voltage		V_{CBO}	50	V
Collector-emitter voltage		V_{CEO}	50	V
Emitter-base voltage		V_{EBO}	5	V
Collector current		I_C	100	mA
Collector power dissipation	DTC115TUA / DTC115TKA	Pc	200	mW
	DTC115TSA		300	
Junction temperature		Tj	150	℃
Storage temperature		Tstg	−55~+150	℃

●**Package, marking, and packaging specifications**

Part No.	DTC115TUA	DTC115TKA	DTC115TSA
Package	UMT3	SMT3	SPT
Marking	09	09	—
Packaging code	T106	T146	TP
Basic ordering unit (pieces)	3000	3000	5000

●**Electrical characteristics** (Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	50	—	—	V	I_C=50 μA
Collector-emitter breakdown voltage	BV_{CEO}	50	—	—	V	I_C=1mA
Emitter-base breakdown voltage	BV_{EBO}	5	—	—	V	I_E=50 μA
Collector cutoff current	I_{CBO}	—	—	0.5	μA	V_{CB}=50V
Emitter cutoff current	I_{EBO}	—	—	0.5	μA	V_{EB}=4V
Collector-emitter saturation voltage	$V_{CE(sat)}$	—	—	0.3	V	I_C/I_B=1mA/0.1mA
DC current transfer ratio	h_{FE}	100	250	600	—	I_C=1mA , V_{CE}=5V
Input resistance	R_1	70	100	130	kΩ	—
Transition frequency	f_T	—	250	—	MHz	V_{CE}=10V , I_E=−5mA , f=100MHz *

* Transition frequency of the device.

(96-317-C115T)