

20 characters × 2 lines COG module

RCM2072R

The RCM2072R is a reflective TN type liquid crystal module with a built-in controller/driver LSI and a display capacity of 20 characters × 2 lines.

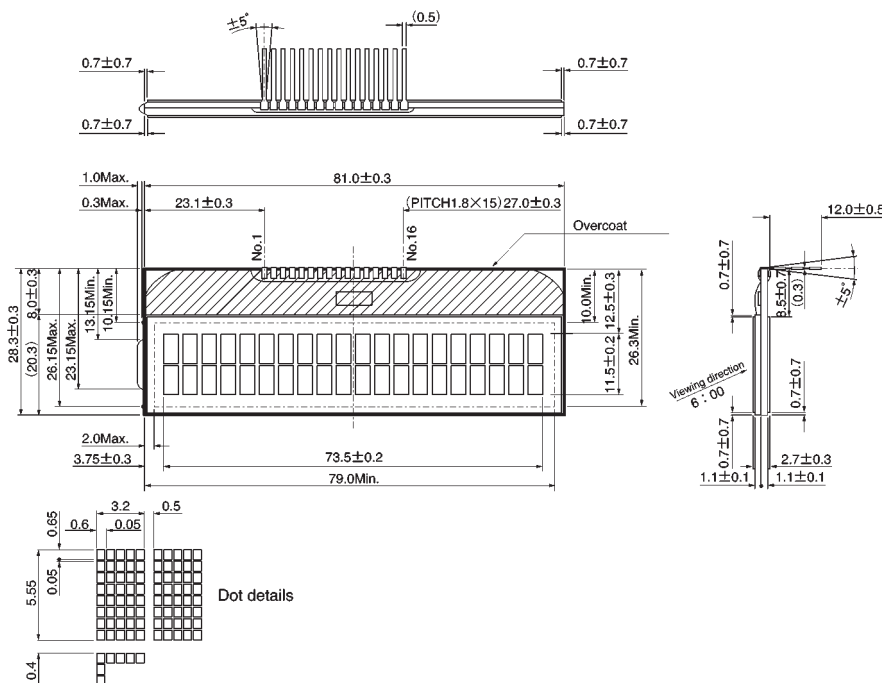
●Applications

Printers, copiers, facsimiles, etc.

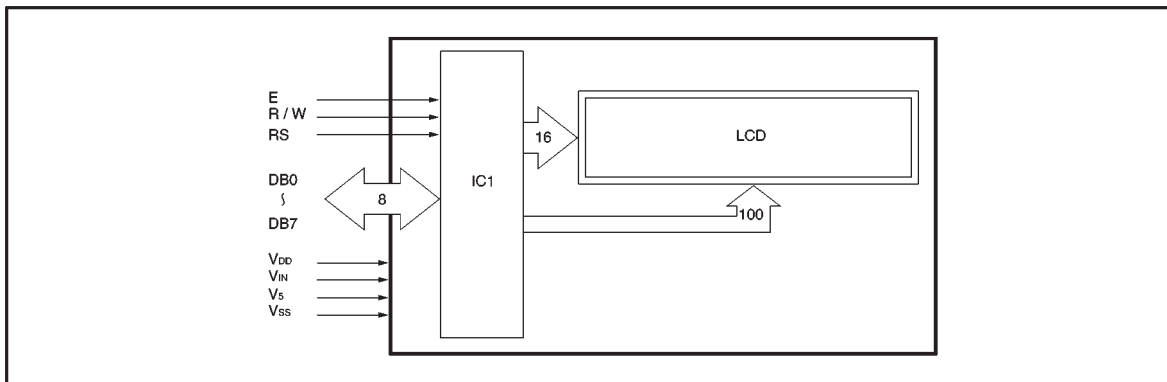
●Features

- 1) Wide viewing angle and high contrast.
- 2) 5 × 7 dot character matrix with cursor.
- 3) Interfaces with 4-bit or 8-bit MPUs.
- 4) Displays up to 237 characters and special symbols
- 5) Custom character patterns are displayed with the character RAM.
- 6) Abundant instruction set including clear display, cursor on/off, and character blinking.
- 7) Compact and lightweight for easy assembly to the host instrument.
- 8) Operable on single 5V power supply.
- 9) Low power consumption.

●External dimensions (Units: mm)



●Block diagram



●Pin assignments

Pin No.	Signal	Pin No.	Signal
1	RS	9	DB5
2	R / W	10	DB6
3	E	11	DB7
4	DB0	12	VSS
5	DB1	13	VDD
6	DB2	14	VIN
7	DB3	15	VS
8	DB4	16	GND

VSS and GND are separate.

VSS is the earth for the IC.

●Power supply example

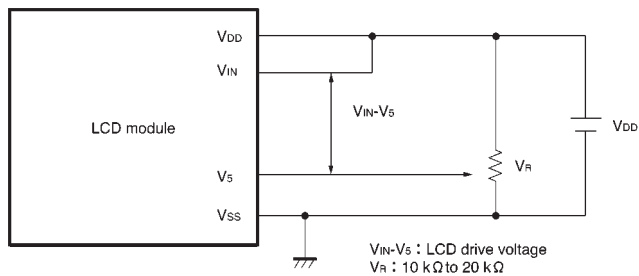


Fig.1

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Logic power supply voltage	V _{DD} -V _{SS}	−0.3	6.0	V
LCD drive voltage	V _{DD} -V _S	−0.3	6.0	V
Input voltage	V _I	−0.3	V _{DD} +0.3	V
Operating temperature	T _{opr}	0	50	°C
Storage temperature	T _{stg}	−20	70	°C

●Electrical characteristics (V_{DD} = 5.0 ± 5%, Ta = 25°C)

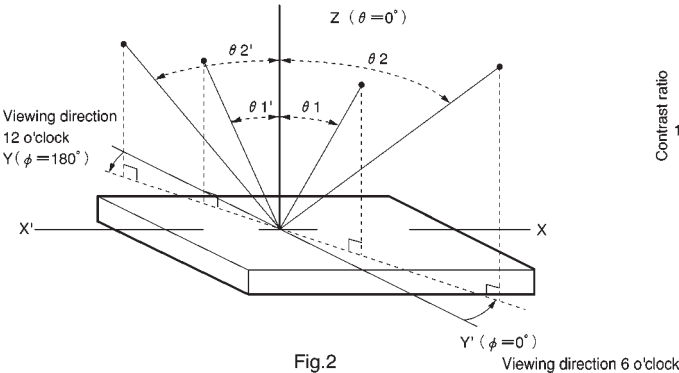
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
High level input voltage	V _{IH}	0.7V _{DD}	—	—	V	—
Low level input voltage	V _{IL}	—	—	0.2V _{DD}	V	—
High level output voltage	V _{OH}	0.75V _{DD}	—	—	V	I _{OH} = −0.1mA
Low level output voltage	V _{OL}	—	—	0.2V _{DD}	V	I _{OL} = 0.1mA
Operating voltage	V _{LCD}	3.0	—	5.0	V	1 / 4Bias
Power supply current	I _{DD}	—	1.5	2.5	mA	V _{DD} = 5.0V

●Optical characteristics (Ta = 25°C)

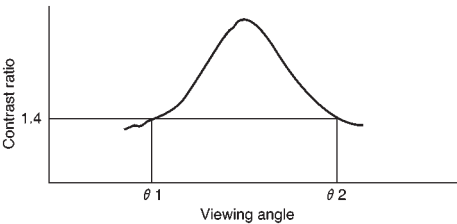
When viewing from below

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Rise time	Tr	—	100	250	ms	$\theta = 10^\circ, \phi = 0^\circ$
Fall time	Td	—	150	250	ms	$\theta = 10^\circ, \phi = 0^\circ$
Contrast ratio	K	—	3	—	—	$\theta = 10^\circ, \phi = 0^\circ$
Viewing angle	$\theta 1$	—	—	10	deg	$K \geq 1.4$
	$\theta 2$	40	—	—	deg	$\phi = 0^\circ$
	ϕ	± 30	—	—	deg	$K \geq 1.4$ $\theta = 20^\circ$

(1) Definition θ and ϕ



(2) Definition of viewing angles



(3) Definition of contrast ratio "K"

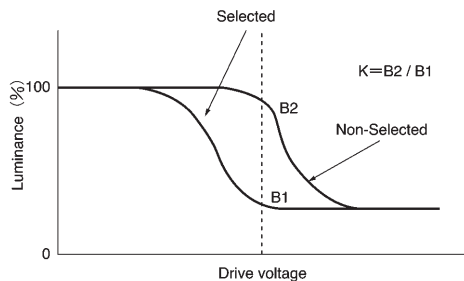


Fig.4

(4) Definition of optical response

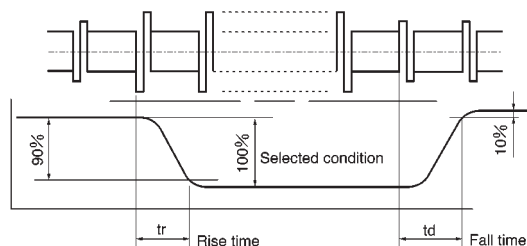


Fig.5

● Pin functions

Symbol	Level	IN / OUT	Function	
V _{SS}	—	—	0V	Earth
V _{DD}	—	—	5.0V	Power supply voltage
V _{IN} V ₅	—	—	3.0~5.0V (V _{DD} -V ₅)	The V ₅ pin is for the liquid crystal contrast adjustment should be kept within the range V _{DD} ≥ V ₅ ≥ V _{SS} .
GND	—	—	Frame GND	
RS	H / L	IN	Register selection signal. 0: Instruction register (writing) Busy flag, address counter (reading) 1: Data register (reading / writing)	
R / W	H / L	IN	Reading (R) and writing (W) selection signal. 0: Writing MPU→LCD module 1: Reading MPU←LCD module	
E	H, H / L	IN	Data reading and writing start signal.	
DB0 } DB3	H / L	IN / OUT	The lower 4 line data buses are 3-state bi-directional. They are not used during 4-bit operation and must be fixed to GND.	
DB4 } DB7	H / L	IN / OUT	The upper 4 line data buses are 3-state bi-directional. DB7 can also be used as a busy flag.	

Note: In order to be able to interface with 4-bit or 8-bit MPUs, the module supports data transfer with two transmissions of 4 bits at a time or one transmission of 8 bits at once.

- (1) When the interface data length is 4 bits, data is transferred between the MPU along DB4 through DB7 buses and DB0 through DB3 buses are not used. Data transferral is completed after two transfers of 4 bit data. First the upper nibble (contents of DB4 through DB7 during 8-bit interfacing) is transferred and then the lower nibble (contents of DB0 through DB3 during 8-bit interfacing) is transferred. Check for busy flag occurs after the second 4-bit data (one instruction) is transferred. At that time, the busy flag and address counter data is also output in two 4-bit increments.
- (2) When the interface data length is 8 bits, the data DB0 through DB7 is transferred along the eight data buses.

●Timing chart
(1) Writing

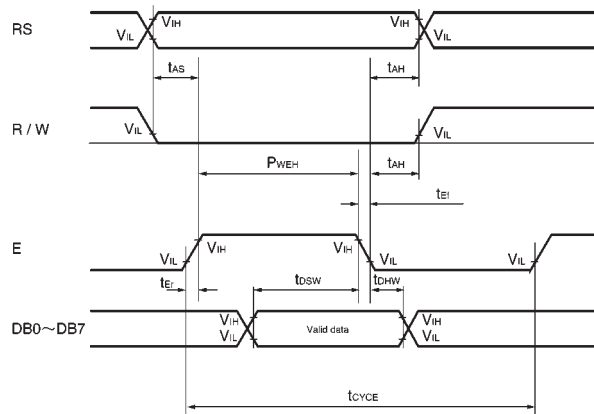


Fig.6

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Enable cycle time	tcyce	500	—	—	ns	Fig.6
Enable pulse time	PWEH	250	—	—	ns	
Enable rise and fall time	tEr / tErf	—	—	20	ns	
Address setup time	tAS	40	—	—	ns	
Address hold time	tAH	10	—	—	ns	
Data setup time	tDSW	60	—	—	ns	
Data hold time	tDHW	10	—	—	ns	

(2) Reading

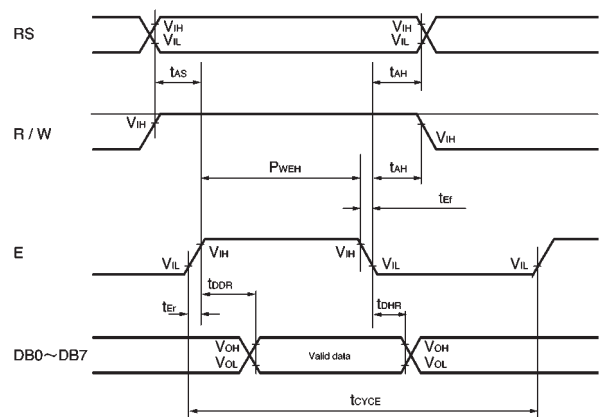


Fig.7

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Enable cycle time	t _{cyce}	500	—	—	ns	Fig.7
Enable pulse time	P _{WEH}	250	—	—	ns	
Enable rise and fall time	t _{Er} / t _{Ef}	—	—	20	ns	
Address setup time	t _{AS}	40	—	—	ns	
Address hold time	t _{AH}	10	—	—	ns	
Data delay time	t _{DDR}	—	—	250	ns	
Data hold time	t _{DHR}	20	—	—	ns	

● Instructions

Instruction	Code										Description	Execution time Max.	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		fosc=250kHz	
Clear display	0	0	0	0	0	0	0	0	0	1	Clears display and sets address 0 of DD RAM to address counter.	1.64ms	
Home cursor	0	0	0	0	0	0	0	0	1	*	Sets address 0 of DD RAM to address counter and returns a shifted display to original position. The contents of DD RAM are unchanged.	1.64ms	
Entry mode set	0	0	0	0	0	0	0	1	I / D	S	Sets the cursor move direction and specifies whether or not to shift display. This operation occurs when reading or writing data.	40 μs	
Display on / off control	0	0	0	0	0	0	1	D	C	B	Turns display on or off (D), turns cursor on or off (C), or blinks the character at the cursor position (B).	40 μs	
Cursor / display shift	0	0	0	0	0	1	S / C	R / L	*	*	Moves cursor or shifts display without changing the DD RAM.	40 μs	
Function set	0	0	0	0	1	DL	N	SD1	SD2	CD	Sets the interface data length (DL), SEG data transfer direction (SD1,SD2), and COM data transfer direction(CD).	40 μs	
CG RAM address set	0	0	0	1	ACG					Sets the CG RAM address. Data received after this is CG RAM data.		40 μs	
DD RAM address set	0	0	1	ADD					Sets the DD RAM address. Data received after this is DD RAM data.		40 μs		
Read busy flag address	0	1	BF	AC					Reads the busy flag signifying internal operations in progress and reads the contents of the address counter.		0 μs		
Write data to CG or DD RAM	1	0	Write Data					Data is written from the DD RAM or CG RAM.			40 μs tADD=6 μs		
Read data from CG or DD RAM	1	1	Read Data					Data is read to DD RAM or CG RAM.			40 μs tADD=6 μs		
	I/D=1: Increment, I/D=0: Decrement S=1: Accompanies display shift S/C=1: Display shift, S/C=0: Cursor movement R/L=1: Right shift , R/L=0: Left shift DL=1: 8 bit, DL=0: 4 bit N=1: 2 lines, N=0: 1 line CD=0: COM1→COM16 CD=1: COM16→COM1 SD1=0,SD2=0: SEG1→SEG50→SEG51→SEG100 SD1=1,SD2=0: SEG1→SEG50→SEG100→SEG51 SD1=0,SD2=1: SEG100→SEG51→SEG50→SEG1 SD1=1,SD2=1: SEG100→SEG51→SEG1→SEG50 BF=1: Internal operation in progress BF=0: Instructions can be received										DD RAM: Display data RAM CG RAM: Character generator RAM ACG: CG RAM address ADD: DD RAM address (corresponds to cursor address) AC: Address counter used for both DD and CG RAM.		Execution times will vary with frequency

(Example) When fosc = 270kHz

$$40\mu\text{s} \times \frac{250}{270} = 37\mu\text{s}$$

● Character code and corresponding character pattern

Upper Lower																
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	*1	A	0	a	P	`	P	Ç	É		—	♪	Σ	a	p	
0001	*2	B	!	1	A	Q	a	q	U	æ	„	7	7	4	a	q
0010	*3	a	"	2	B	R	b	r	e	E	7	イ	ウ	×	e	θ
0011	*4	1	#	3	C	S	c	s	a	ô	„	ウ	7	E	e	„
0100	*5	ô	\$	4	D	T	d	t	a	ö	„	7	7	7	μ	α
0101	*6	U	%	5	E	U	e	u	a	ö	„	7	7	7	7	U
0110	*7	A	&	6	F	V	f	v	a	ö	7	7	7	7	7	Σ
0111	*8	N	'	7	G	W	g	w	9	U	7	7	7	7	9	π
1000	*1	a	(	8	H	X	h	x	e	9	7	7	7	7	7	7
1001	*2	Q	)	9	I	V	i	v	e	ö	7	7	7	7	7	7
1010	*3	z	*	:	J	Z	j	z	e	ö	7	7	7	7	7	7
1011	*4	7	+	;	K	L	k	l	i	ö	7	7	7	7	7	7
1100	*5	7	,	<	L	#	1	1	i	e	7	7	7	7	7	7
1101	*6	1	—	=	M	I	m	/	1	#	7	7	7	7	7	7
1110	*7	Σ	„	>	N	^	n	÷	A	k	3	E	7	7	7	7
1111	*8	Σ	/	?	0	—	o	÷	A	7	7	7	7	7	7	7

●Reset function

When you turn on the power supply, the module automatically returns to its initial (reset) settings. At the initial settings, the busy flag (BF) becomes "1." The busy status last 10 ms from when V_{DD} reaches 4.5V. At the initial settings, following instructions are carried out.

(1) Clear display	
(2) Function set	
8-bit interface data length	(DL = 1)
Two line display	(N = 1)
SEG signal transfer direction SEG1→SEG50→SEG51→SEG100	(SD1 = 0, SD2 = 0)
COM signal transfer direction COM1→COM16	(CD = 0)
(3) Display on/off control	
Display off	(D = 0)
Cursor off	(C = 0)
Blinking off	(B = 0)
(4) Entry mode set	
+1 (increment)	(I/D = 1)
No shift	(S = 0)

* The internal reset circuit may not operate properly due to conditions with the power supply. If this is the case, use the appropriate instruction to reset the settings.

●Operation notes

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| <p>(1) Handling precautions</p> <ul style="list-style-type: none"> • Protect the module from strong shocks as they can cause damage or defective operation. • The polarizing plate on the surface of the module is soft and can easily be scratched. Wipe away dirt and dust using an alcohol-based cleanser. • If the liquid crystal panel is damaged and liquid crystal contacts your clothing or body, wash immediately with soap and water. • If the module is to be used for long periods subjected to direct sunlight, employ a filter to block the ultraviolet rays. • Do not use the module in areas of high temperature or high humidity. Do not use the module in locations exposed to direct sunlight or fluorescent light. • A protective film (polyethylene) is pasted over ROHM liquid crystal modules to protect the panel surfaces. When peeling this film off, be sure to peel as slow as possible in order to minimize the generation of static electricity. | <p>(2) Precautions during operation</p> <ul style="list-style-type: none"> • Do not connect or disconnect the module while the power supply is turned on. • Input the input signal after the module power supply is turned on. When turning it off, turn off the input signal first. Otherwise the IC may be damaged by the latch-up phenomenon. |
|--|--|