



STW13NK100Z

N-CHANNEL 1000V - 0.56Ω - 13.5A TO-247
Zener-Protected SuperMESH™ Power MOSFET

TARGET DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STW13NK100Z	1000 V	< 0.70 Ω	13.5 A	350 W

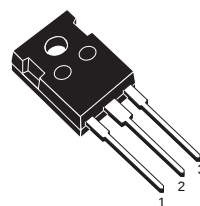
- TYPICAL R_{DS(on)} = 0.56 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

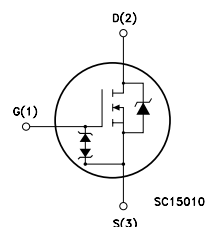
APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES



TO-247

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW13NK100Z	W13NK100Z	TO-247	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	1000	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	1000	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	13.5	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	8.2	A
$I_{DM} (\bullet)$	Drain Current (pulsed)	54	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	350	W
	Derating Factor	2.4	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	TBD	V
$dv/dt (1)$	Peak Diode Recovery voltage slope	TBD	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	$^\circ\text{C}$

($\bullet$) Pulse width limited by safe operating area

(1) $I_{SD} \leq 13.5\text{A}$, $di/dt \leq \text{TBD A}/\mu\text{s}$, $V_{DD} \leq 800\text{V}$, $T_j \leq T_{JMAX}$.

(*) Limited only by maximum temperature allowed

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case Max	0.42	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$ T_I	Thermal Resistance Junction-ambient Max Maximum Lead Temperature For Soldering Purpose	50 300	$^\circ\text{C}/\text{W}$ $^\circ\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j \text{ max}$)	13.5	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50 \text{ V}$)	TBD	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)
 ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	1000			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 150\text{ }\mu A$	3	3.75	4.5	V
$R_{DS(on)} (1)$	Static Drain-source On Resistance	$V_{GS} = 10V$, $I_D = 6.75\text{ A}$		0.56	0.70	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15\text{ V}$, $I_D = 6.75\text{ A}$		71		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1\text{ MHz}$, $V_{GS} = 0$		6300 400 80		pF pF pF
$C_{oss\text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0V$, $V_{DS} = 0V\text{ to }800V$		TBD		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 500\text{ V}$, $I_D = 6.75\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load see, Figure 3)		TBD TBD TBD TBD		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 800V$, $I_D = 13.5\text{ A}$, $V_{GS} = 10V$		220 TBD TBD	297	nC nC nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				13.5 54	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 13.5\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 13.5\text{ A}$, $di/dt = 100A/\mu s$ $V_{DD} = 100\text{ V}$, $T_j = 25^{\circ}C$ (see test circuit, Figure 5)		TBD TBD TBD		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 13.5\text{ A}$, $di/dt = 100A/\mu s$ $V_{DD} = 100\text{ V}$, $T_j = 150^{\circ}C$ (see test circuit, Figure 5)		TBD TBD TBD		ns μC A

 Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

 3. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Fig. 1: Unclamped Inductive Load Test Circuit

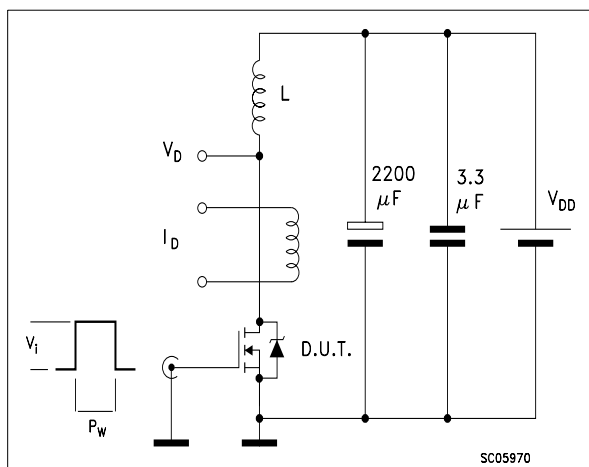


Fig. 2: Unclamped Inductive Waveform

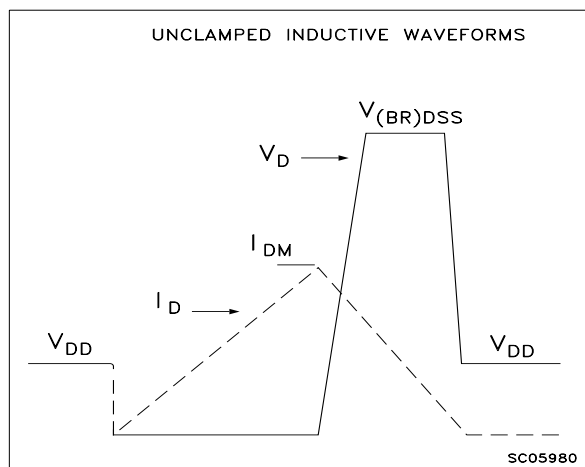


Fig. 3: Switching Times Test Circuit For Resistive Load

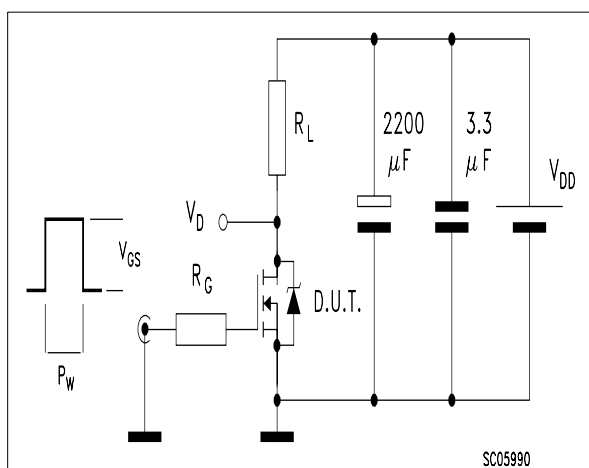


Fig. 4: Gate Charge test Circuit

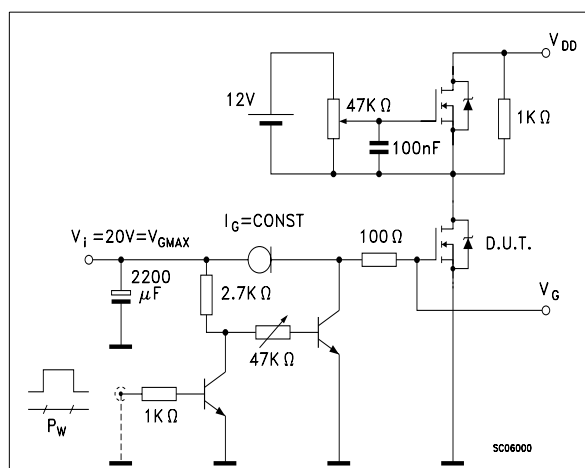
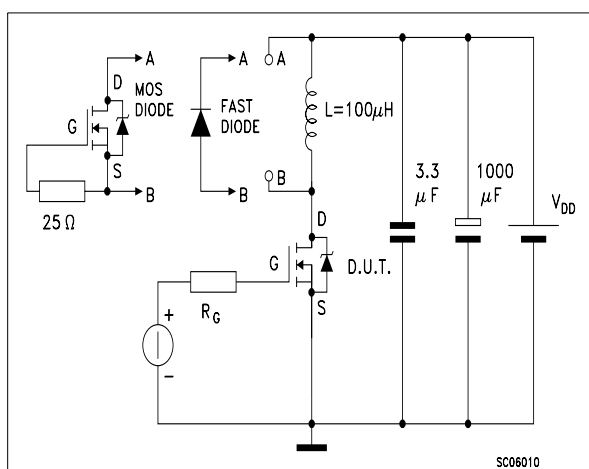
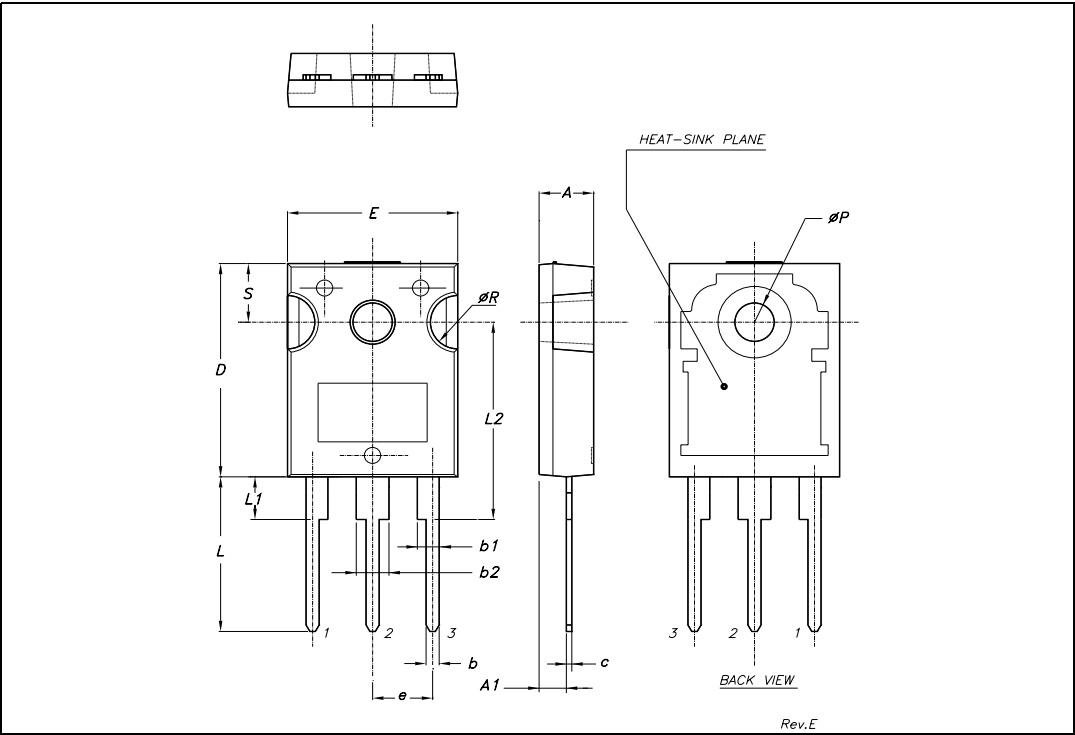


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



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