16-Bit CCD/CIS Analog Signal Processor

Features

- Operating voltage: 3.3V
- Low power consumption at 56mW
- Power-down mode: Under 1μA (clock timing keep low)
- 16-bit 6 MSPS A/D converter
- Guaranteed no missing codes
- Supports CDS/SHA mode
- 1~6 programmable gain
- ±200mV programmable offset
- Input clamp circuitry
- Internal voltage reference
- Multiplexed byte-wide output (8+8 format)
- Programmable 3-wire serial interface
- 3.3V digital I/O compatibility
- 28-pin SSOP package

Applications

Low power flatbed document scanners

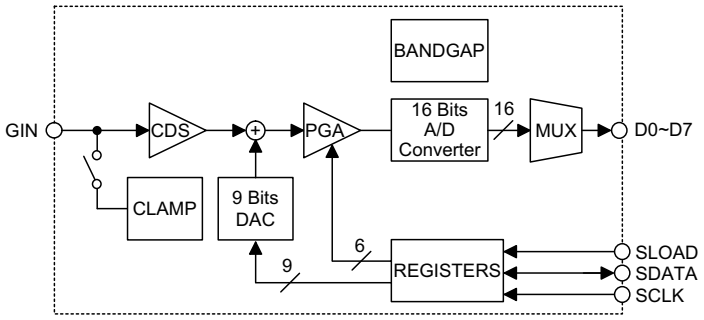
General Description

The HT82V36 is a complete analog signal processor for CCD imaging applications. It features a 1-channel architecture designed to sample and condition the outputs of linear CCD arrays. It consists of an input clamp, Correlated Double Sampler (CDS), offset DAC and Programmable Gain Amplifier (PGA), and a low power 16-bit A/D converter.

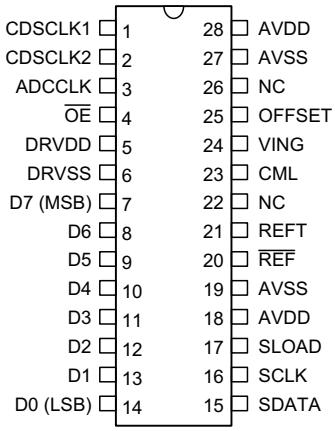
The CDS amplifiers may be disabled for use with sensors such as Contact Image Sensors (CIS) and CMOS active pixel sensors, which do not require CDS.

The 16-bit digital output is multiplexed into an 8-bit output word that is accessed using two read cycles. The internal registers are programmed through a 3-wire serial interface, which provides gain, offset and operating mode adjustments.

Block Diagram

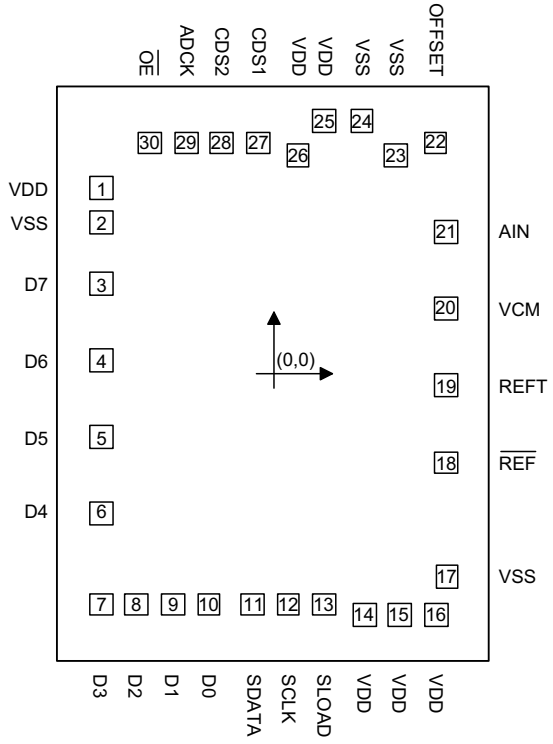


Pin Assignment



HT82V36
– 28 SSOP-A

Pad Assignment



Chip size: 1485×1980 $(\mu m)^2$

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Pad No.	X	Y	Pad No.	X	Y
1	–578.373	631.150	16	544.577	–815.950
2	–578.373	513.900	17	579.577	–684.450
3	–578.373	306.350	18	576.277	–298.800
4	–578.373	46.750	19	576.277	–39.200
5	–578.373	–212.850	20	576.277	220.100
6	–578.373	–472.450	21	576.277	480.000
7	–577.823	–777.150	22	541.677	782.050
8	–457.823	–777.150	23	406.427	737.250
9	–337.223	–777.150	24	294.877	856.700
10	–217.223	–777.150	25	170.577	856.700
11	–71.623	–777.150	26	81.527	737.250
12	48.977	–777.150	27	–51.873	782.050
13	169.577	–777.150	28	–172.473	782.050
14	303.677	–815.950	29	–293.073	782.050
15	419.677	–815.950	30	–413.673	782.050

Pad Description

Pad No.	Pad Name	I/O	Description
1	CDSCLK1	DI	CDS reference clock pulse input
2	CDSCLK2	DI	CDS data clock pulse input
3	ADCCLK	DI	A/D sample clock input for 3-channels mode
4	$\overline{OE}$	DI	Output enable, active low
5	DRVDD	P	Digital driver power
6	DRVSS	P	Digital driver ground
7~14	D7~D0	DO	Digital data output
15	SDATA	DI/DO	Serial data input/output
16	SCLK	DI	Clock input for serial interface
17	SLOAD	DI	Serial interface load pulse
18, 27	AVSS	P	Analog ground
19, 28	AVDD	P	Analog supply
20	$\overline{REF}$	AO	Reference decoupling
21	REFT	AO	Reference decoupling
23	CML	AO	Internal reference output
24	VING	AI	Analog input
25	OFFSET	AO	Clamp bias level decoupling

Absolute Maximum Ratings

Supply Voltage .....–0.3V to 3.6V

Input Voltage .....V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature .....–50°C to 125°C

Operating Temperature .....–25°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Logic Inputs							
V_{IH}	High Level Input Voltage	—	—	$0.8\times V_{DD}$	—	—	V
V_{IL}	Low Level Input Voltage	—	—	—	—	$0.2\times V_{DD}$	V
I_{IH}	High Level Input Current	—	—	—	10	—	μA
I_{IL}	Low Level Input Current	—	—	—	10	—	μA
C_{IN}	Input Capacitance	—	—	—	10	—	pF
Logic Outputs							
V_{OH}	High Level Output Voltage	—	—	V_{DD}-0.5	—	—	V
V_{OL}	Low Level Output Voltage	—	—	—	—	0.5	V
I_{OH}	High Level Output Voltage	—	—	—	1	—	mA
I_{OL}	Low Level Output Voltage	—	—	—	1	—	mA

A.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Maximum Conversion Rate							
t_{MAX}	1-channel Mode with CDS/CIS	—	—	6	—	—	MHz
Accuracy (Entire Signal Path)							
	ADC Resolution	—	—	—	16	—	
	Integral Nonlinear (INL)	—	—	—	±16	—	LSB
	Differential Nonlinear (DNL)	—	—	–1	—	2	LSB
	Offset Error	—	—	–100	TBD	100	mV
	Gain Error	—	—	—	TBD	—	%FSR
Analog Inputs							
R_{FS}	Full-scale Input Range	—	—	1.3	1.4	1.6	Vp-p
V_i	Input Limits	—	—	AVDD-0.3	—	AVDD+0.3	V
C_i	Input Capacitance	—	—	—	TBD	—	pF
I_i	Input Current	—	—	—	TBD	—	μA
Amplifiers							
	PGA Gain at Minimum	—	—	—	1	—	V/V
	PGA Gain at Maximum	—	—	—	5.85	—	V/V
	PGA Gain Resolution	—	—	—	6	—	Bits
	Programmable Offset at Minimum	—	—	—	–200	—	mV
	Programmable Offset at Maximum	—	—	—	200	—	mV
	Offset Resolution	—	—	—	9	—	Bits
Temperature Range							
t_A	Operating	—	—	0	—	70	°C
Power Supplies							
V_{ADD}	AVDD	—	—	3	3.3	3.6	V
V_{DRDD}	DRVDD	—	—	3	3.3	3.6	V
Power Consumption							
P_{tot}	Total Power Consumption	—	—	—	56	—	mW

Timing Specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock Parameters					
t_{ADCLK}	Pixel Rate Clock	166	—	—	ns
t_{ADH}	ADCCLK Pulse High Width	80	—		ns
t_{ADL}	ADCCLK Pulse Low Width	80	—		ns
t_{C1}	CDSCLK1 Pulse Width	20	—	—	ns
t_{C2}	CDS Mode CDSCLK2 Pulse Width	20	—	—	ns
t_{C3}	SHA Mode CDSCLK2 Pulse Width	40	—	—	ns
t_{C2ADF}	CDSCLK2 Falling to ADCCLK Falling	60	—	—	ns
t_{ADFC1}	ADCCLK Falling to CDSCLK1 Rising	2	—	—	ns
t_{ADFC2}	ADCCLK Falling to CDSCLK2 Rising	2	—	—	ns
t_{AD}	Analog Sampling Delay	5	—	—	ns
Serial Interface					
f_{SCLK}	Maximum SCLK Frequency	10	—	—	MHz
t_{LS}	SLOAD to SCLK Setup Time	133	—	—	ns
t_{LH}	SCLK to SLOAD Hold Time	50	—	—	ns
t_{DS}	SDATA to SCLK Rising Setup Time	16	—	—	ns
t_{DH}	SCLK Rising to SDATA Hold Time	15	—	—	ns
t_{RDV}	Falling to SDATA Valid	50	—	—	ns
Data Output					
t_{OD}	Output Delay	—	8	—	ns
	Latency (Pipeline Delay)	—	9	—	Cycles

Functional Description

Integral nonlinear (INL)

Integral nonlinear error refers to the deviation of each individual code from a line drawn from zero scale through positive full scale. The point used as zero scale occurs 1 /2 LSB before the first code transition. Positive full scale is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential nonlinear (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed to 16-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

Offset error

The first ADC code transition should occur at a level 1/2 LSB above the nominal zero scale voltage.

The offset error is the deviation of the actual first code transition level from the ideal level.

Gain error

The last code transition should occur for an analog value 1/2 LSB below the nominal full-scale voltage.

Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

Aperture delay

The aperture delay is the time delay that occurs when a sampling edge is applied to the HT82V36 until the actual sample of the input signal is held. Both CDSCLK1 and CDSCLK2 sample the input signal during the transition from high to low, so the aperture delay is measured from each clock′s falling edge to the instant the actual internal sample is taken.

Internal register descriptions

Register Name	Address			Data Bits								
	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	0	0	0	0	0	1	1	CDS on	Clamp Voltage	Enable Power Down	Output Delay	1byte out
Reserved	0	0	1									
Reserved	0	1	0									
Green PGA	0	1	1	X	0	0	MSB					LSB
Reserved	1	0	0									
Reserved	1	0	1									
Green Offset	1	1	0	MSB								LSB
Reserved	1	1	1									

Internal register map

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	Set to 1	Set to 1	CDS operation	Clamp bias	Power-down	Output delay	1 byte out
				1=CDS mode*	1=2.5V*	1=On	1=On	1=On
				0=CIS mode	0=2V	0=Off (Normal)*	0=Off*	0=Off*

Configuration register settings

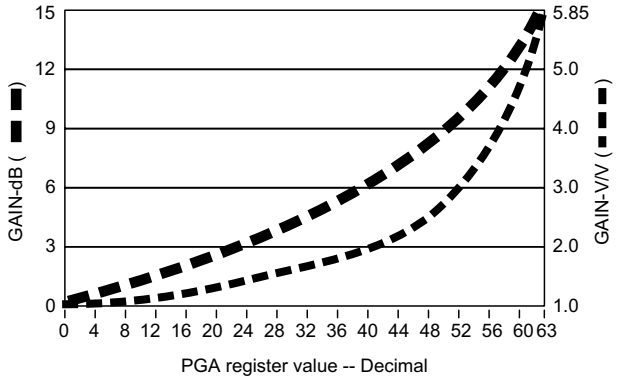
Note: * Power-on default value

PGA gain registers

There are three PGA registers for individually programming the gain in the red, green and blue channels. Bits D8, D7 and D6 in each register must be set low, and bits D5 through D0 control the gain range in 64 increments. See figure for a graph of the PGA gain versus PGA register code. The coding for the PGA registers is straight binary, with an all zero words corresponding to the minimum gain setting (1x) and an all one word corresponding to the maximum gain setting (5.85x).

The HT82V36 uses one Programmable Gain Amplifier (PGA) for each channel. Each PGA has a gain range from 1x (0dB) to 5.85x (15.3dB), adjustable in 64 steps. The Figure shows the PGA gain as a function of the PGA register code. Although the gain curve is approximately linear in dB, the gain in V/V varies in nonlinear proportion with the register code, according to the following the equation: $\text{Gain}=\frac{5.85}{1+4.85\times(\frac{63-G}{63})}$

Where G is the decimal value of the gain register contents, and varies from 0 to 63.



PGA gain transfer function

D8	D7	D6	D5	D4	D3	D2	D1	D0	Gain (V/V)	Gain (dB)
Set to 0	Set to 0	Set to 0	MSB					LSB		
0	0	0	0	0	0	0	0	0*	1.0	0.0
0	0	0	0	0	0	0	0	1	1.013	0.12
					.				.	.
					.				.	.
					.				.	.
0	0	0	1	1	1	1	1	0	5.43	14.7
0	0	0	1	1	1	1	1	1	5.85	15.3

PGA gain register settings

Note: * Power-on default value

Offset registers

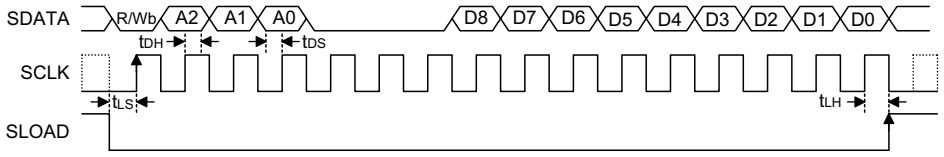
There are three PGA registers for individually programming the offset in the red, green, and blue channels. Bits D8 through D0 control the offset range from −200mV to 200mV in 512 increments.

The coding for the offset registers is sign magnitude, with D8 as the sign bit. The Table shows the offset range as a function of the bits D8 through D0.

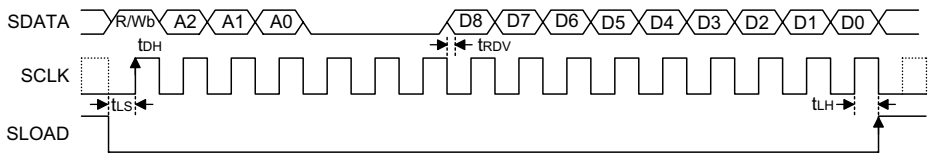
D8	D7	D6	D5	D4	D3	D2	D1	D0	Offset (mV)
MSB								LSB	
0	0	0	0	0	0	0	0	0*	0
0	0	0	0	0	0	0	0	1	0.78
					.				.
					.				.
					.				.
0	1	1	1	1	1	1	1	1	200
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	−0.78
					.				.
					.				.
					.				.
1	1	1	1	1	1	1	1	1	−200

Note: * Power-on default value

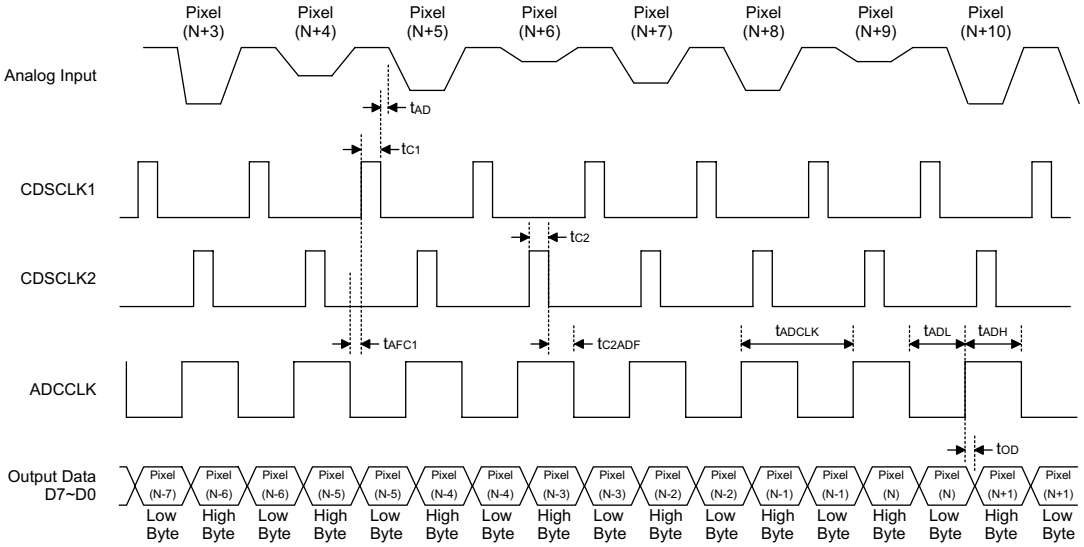
Timing Diagrams



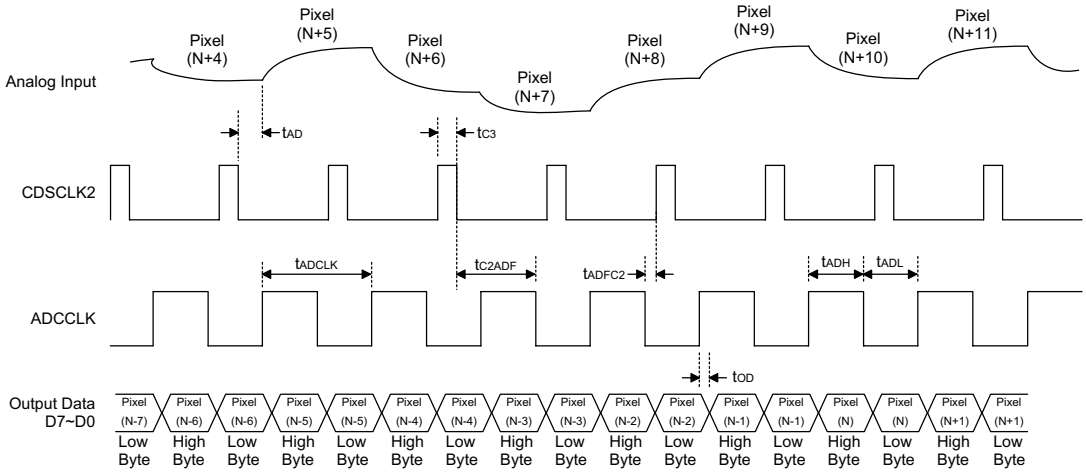
Serial write operation timing



Serial read operation timing

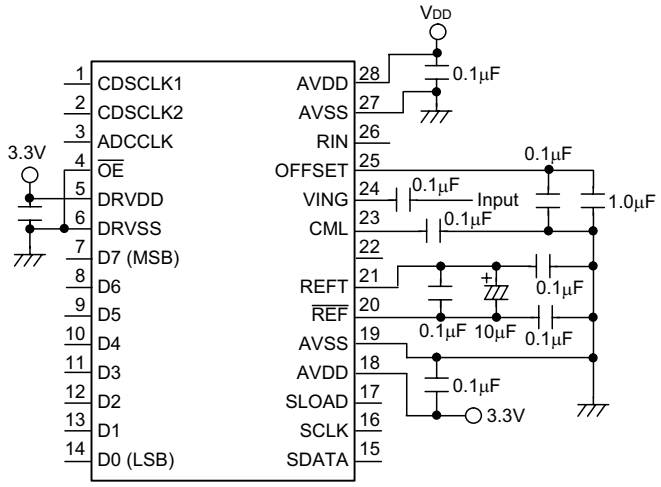


1-channel CDS mode timing



1-channel SHA mode timing

Application Circuits

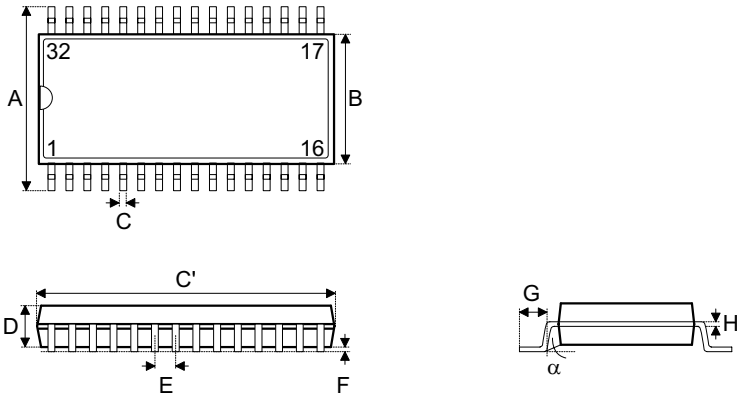


Note: The recommended circuit configuration for 1-channel CDS mode operation is shown below.
The recommended input coupling capacitor value is 0.1μF (see circuit operation section for more details).

A single ground plane is recommended for the HT82V36. A separate power supply may be used for DRVDD, the digital driver supply, but this supply pin should still be decoupled to the same ground plane as the rest of the HT82V36. The loading of the digital outputs should be minimized, either by using short traces to the digital ASIC, or by using external digital buffers. All 0.1μF decoupling capacitors should be located as close as possible to the HT82V36 pins.

Package Information

28-pin SSOP (150mil) outline dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	150	—	157
C	8	—	12
C′	386	—	394
D	54	—	60
E	—	25	—
F	4	—	10
G	22	—	28
H	7	—	10
α	0°	—	8°

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