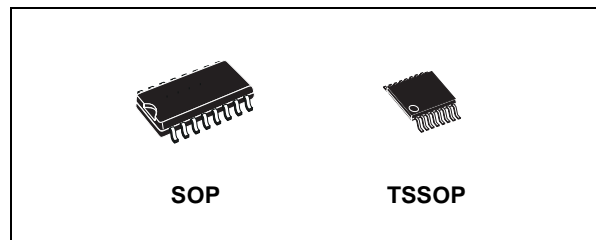




74LVX139

LOW VOLTAGE CMOS DUAL 2 TO 4 DECODER/DEMULTIPLEXER

- HIGH SPEED :
 $t_{PD} = 6.0ns$ (TYP.) at $V_{CC} = 3.3V$
- 5V TOLERANT INPUTS
- INPUT VOLTAGE LEVEL :
 $V_{IL}=0.8V$, $V_{IH}=2V$ at $V_{CC}=3V$
- LOW POWER DISSIPATION:
 $I_{CC} = 2 \mu A$ (MAX.) at $T_A=25^\circ C$
- LOW NOISE:
 $V_{OLP} = 0.3V$ (TYP.) at $V_{CC} = 3.3V$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4mA$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(OPR) = 2V$ to $3.6V$ (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 139
- IMPROVED LATCH-UP IMMUNITY
- POWER DOWN PROTECTION ON INPUTS



ORDER CODES

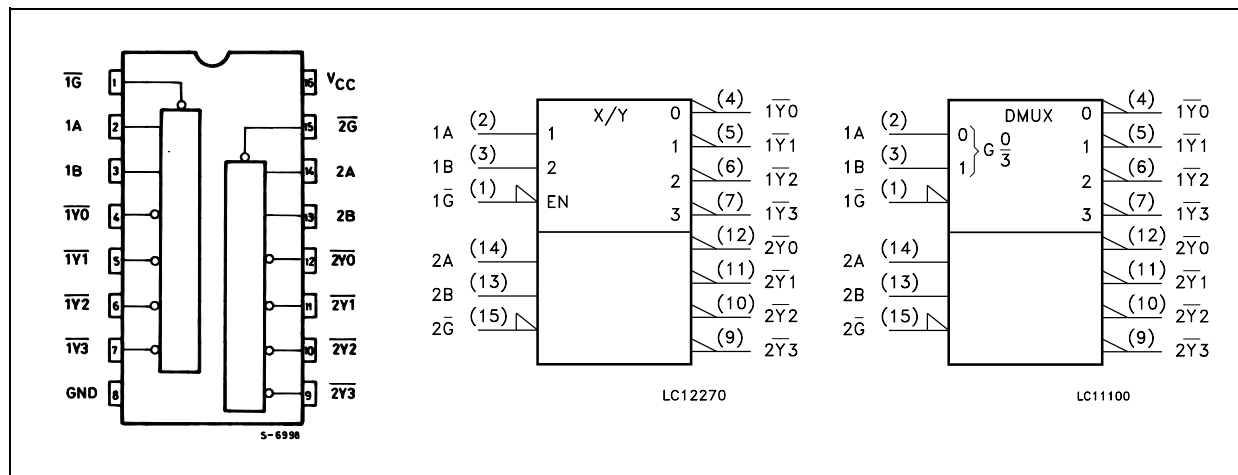
PACKAGE	TUBE	T & R
SOP	74LVX139M	74LVX139MTR
TSSOP		74LVX139TTR

The active low enable input can be used for gating or as a data input for demultiplexing applications. While the enable input is held high, all four outputs are high independently of the other inputs. Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V system. It combines high speed performance with the true CMOS low power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

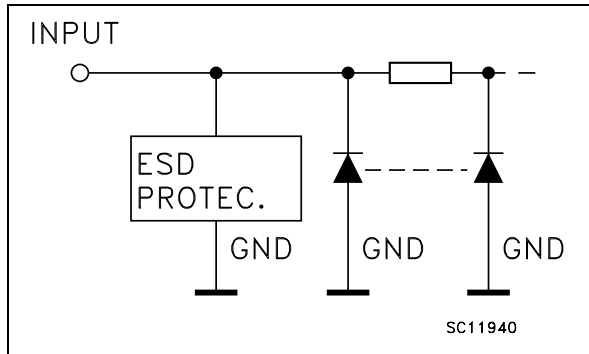
DESCRIPTION

The 74LVX139 is a low voltage CMOS DUAL 2 TO 4 DECODER/DEMULTIPLEXER fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

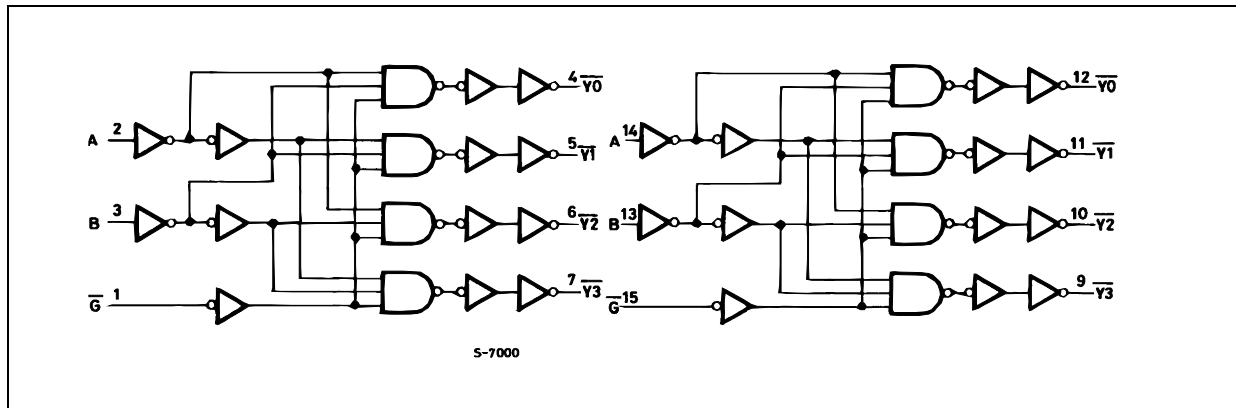
PIN No	SYMBOL	NAME AND FUNCTION
1, 15	$\overline{1G}, \overline{2G}$	Enable Inputs
2, 3	1A, 1B	Address Inputs
4, 5, 6, 7	1Y0 to 1Y3	Outputs
12, 11, 10, 9	2Y0 to 2Y3	Outputs
14, 13	2A, 2B	Address Inputs
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
\overline{nG}	nB	nA	$\overline{nY0}$	$\overline{nY1}$	$\overline{nY2}$	$\overline{nY3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

X : Don't Care
n: 1, 2.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}\text{C}$
T_L	Lead Temperature (10 sec)	300	$^{\circ}\text{C}$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	$^{\circ}\text{C}$
dt/dv	Input Rise and Fall Time (note 2) ($V_{CC} = 3.3\text{V}$)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
				$T_A = 25^{\circ}\text{C}$			-40 to 85 $^{\circ}\text{C}$		-55 to 125 $^{\circ}\text{C}$		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V_{IH}	High Level Input Voltage	2.0								V	
		3.0									
		3.6									
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		V	
		3.0				0.8		0.8			
		3.6				0.8		0.8			
V_{OH}	High Level Output Voltage	2.0	$I_O = -50 \mu\text{A}$	1.9	2.0		1.9		1.9	V	
		3.0	$I_O = -50 \mu\text{A}$	2.9	3.0		2.9		2.9		
		3.0	$I_O = -4 \text{mA}$	2.58			2.48		2.4		
V_{OL}	Low Level Output Voltage	2.0	$I_O = 50 \mu\text{A}$		0.0	0.1		0.1		V	
		3.0	$I_O = 50 \mu\text{A}$		0.0	0.1		0.1			
		3.0	$I_O = 4 \text{mA}$			0.36		0.44			0.55
I_I	Input Leakage Current	3.6	$V_I = 5.5\text{V}$ or GND			± 0.1		± 1		μA	
I_{CC}	Quiescent Supply Current	3.6	$V_I = V_{CC}$ or GND			2		20		μA	

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C _L = 50 pF		0.3	0.5					V
V _{OLV}				-0.5	-0.3						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2							
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time A, B to \bar{Y}	2.7	15		7.5	12.0		14.0		16.0	ns	
		2.7	50		9.4	15.0		17.0		19.0		
		3.3(*)	15		6.0	8.5		10.0		11.5		
		3.3(*)	50		7.6	11.0		12.5		14.5		
t _{PLH} t _{PHL}	Propagation Delay Time G to Y	2.7	15		7.3	12.0		14.0		16.0	ns	
		2.7	50		9.2	15.0		17.0		19.0		
		3.3(*)	15		5.8	8.5		10.0		11.5		
		3.3(*)	50		7.2	11.0		12.5		14.5		
t _{OSLH} t _{OSHL}	Output To Output Skew Time (note 1, 2)	2.7	50		0.5	1.0		1.5		1.5	ns	
		3.3(*)	50		0.5	1.0		1.5		1.5		

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

2) Parameter guaranteed by design

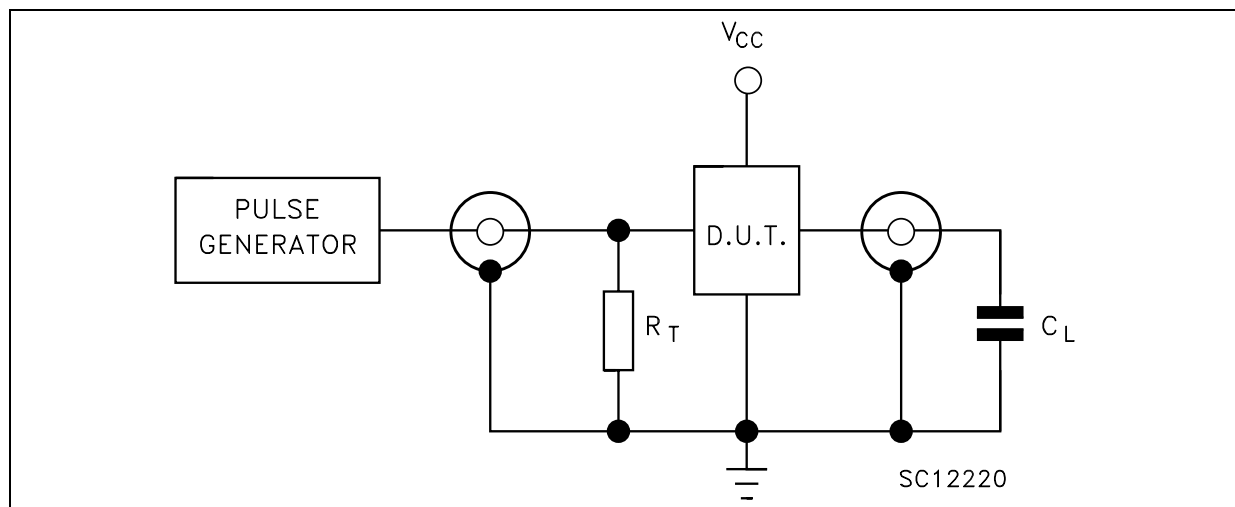
(*) Voltage range is 3.3V ± 0.3V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	3.3			5						pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3	f _{IN} = 10MHz		13						pF

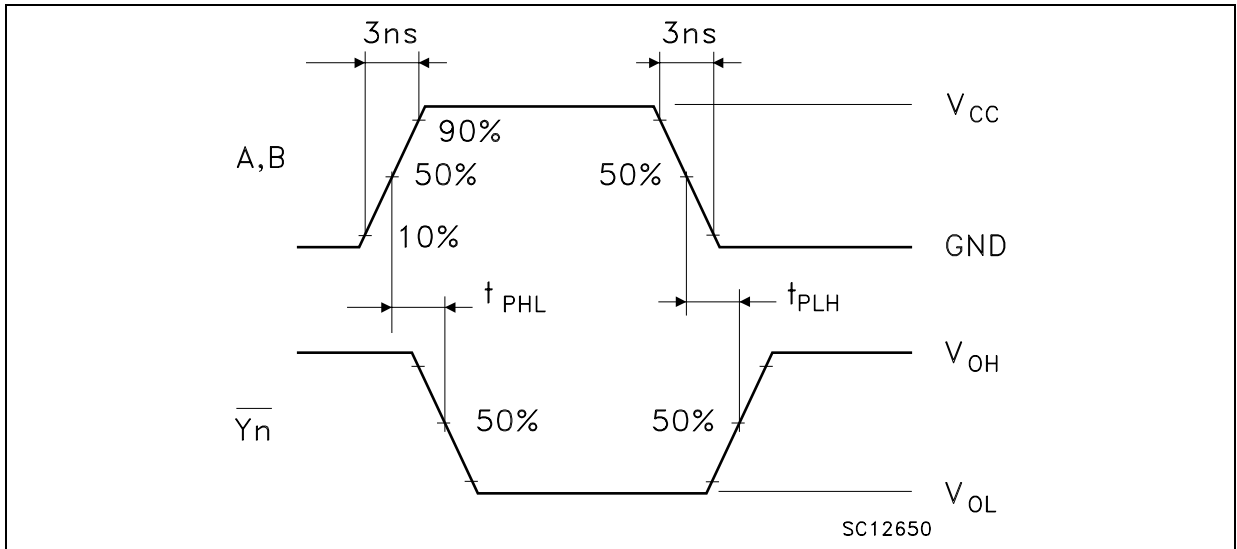
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per Decoder)

TEST CIRCUIT

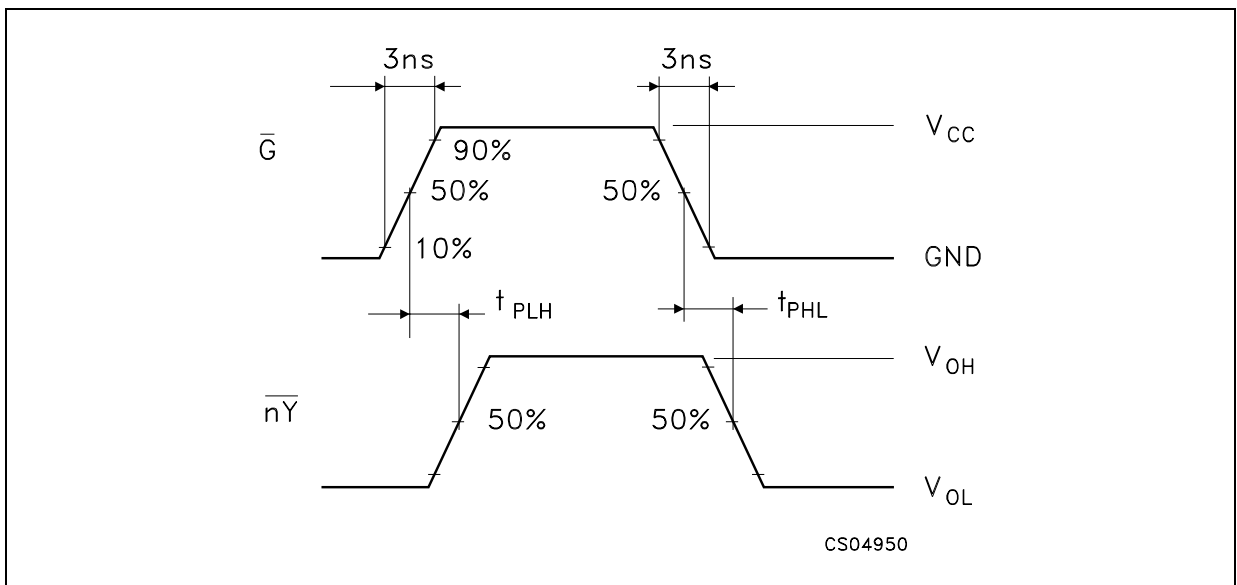


C_L = 15/50pF or equivalent (includes jig and probe capacitance)
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING OUTPUTS (f=1MHz; 50% duty cycle)

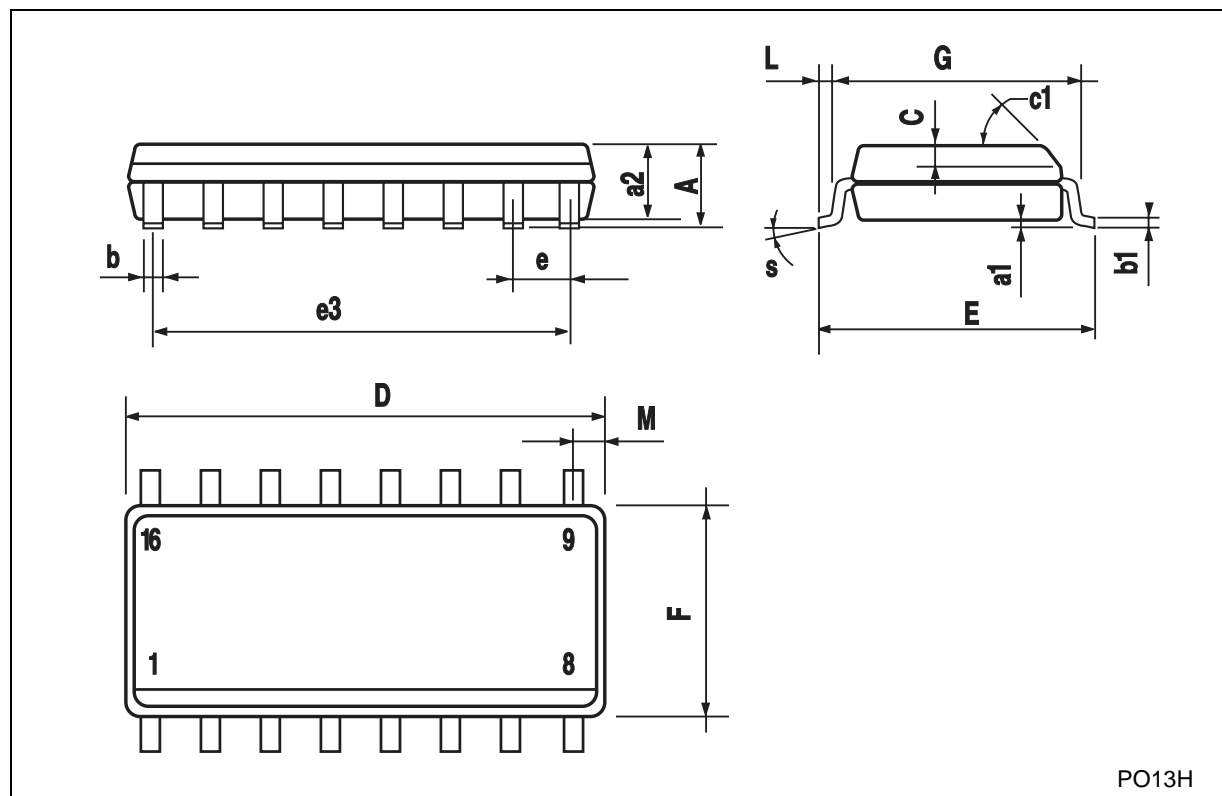


WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING OUTPUTS (f=1MHz; 50% duty cycle)



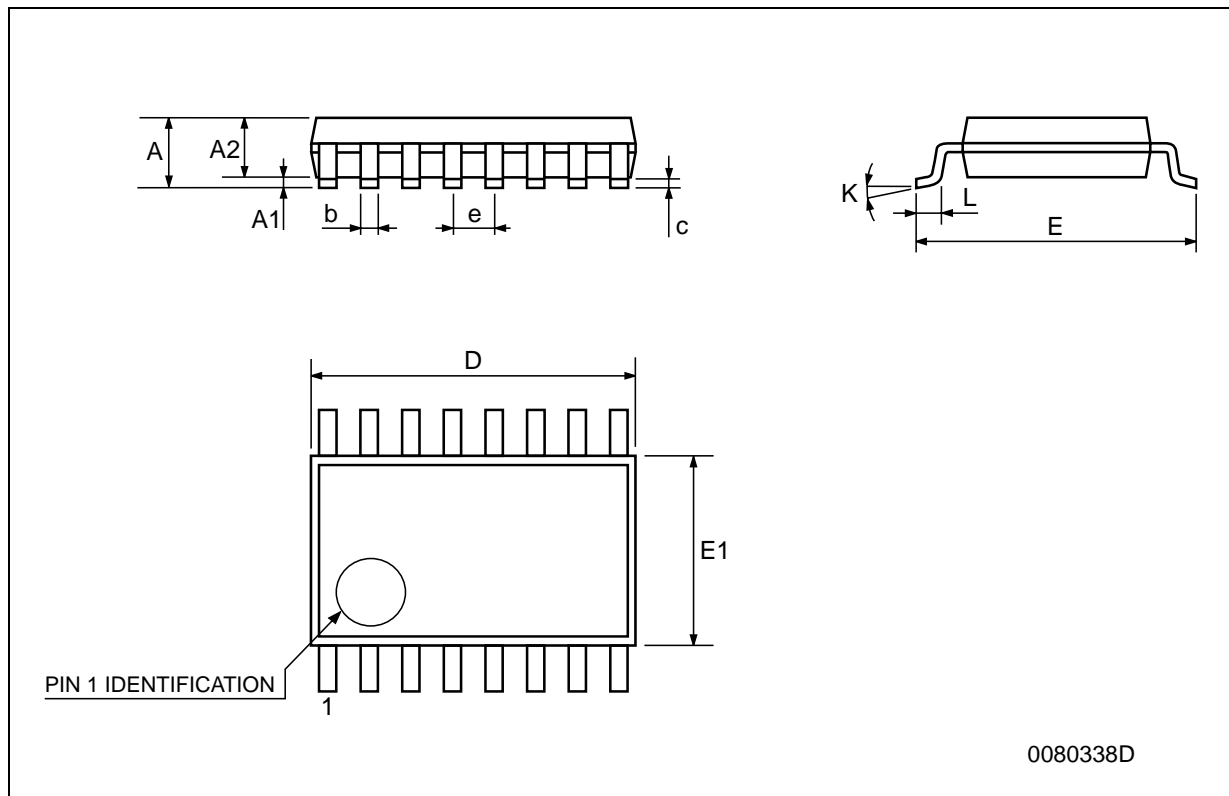
SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



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