CY7C439

Bidirectional 2K x 9 FIFO

Features

- **2048 x 9 FIFO buffer memory**
- **Bidirectional operation**
- **High-speed 28.5-MHz asynchronous reads and writes**
- **Simple control interface**
- **Registered and transparent bypass modes**
- **Flags indicate Empty, Full, and Half Full conditions**
- **5V ± 10% supply**
- **Available in 300-mil DIP, PLCC, LCC, and SOJ packages**
- **TTL compatible**

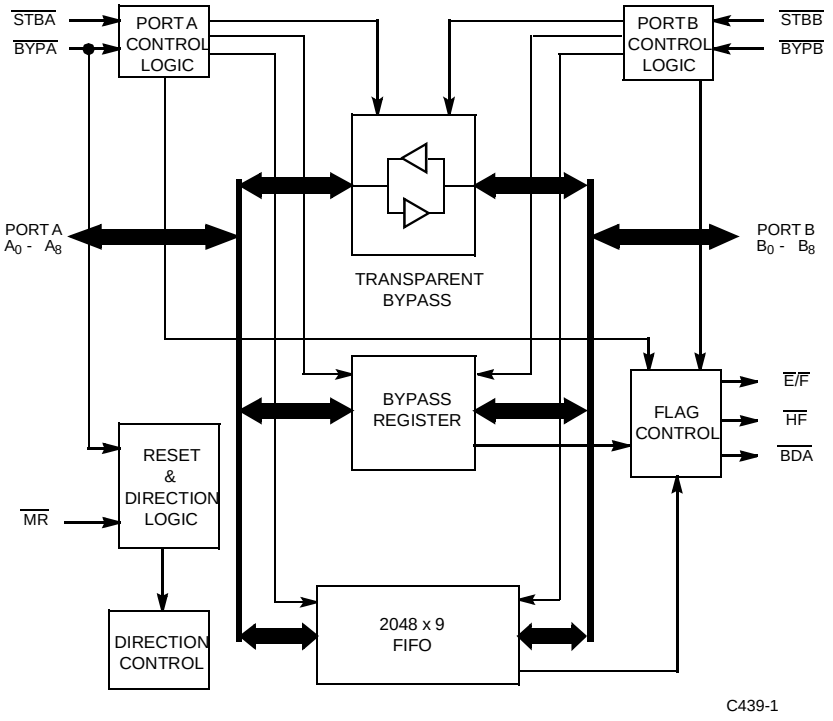
Functional Description

The CY7C439 is a 2048 x 9 FIFO memory capable of bidirectional operation. As the term first-in first-out (FIFO) implies, data becomes available to the output port in the same order that it was presented to the input port. There are two pins that indicate the amount of data contained within the FIFO block—$\overline{E}/\overline{F}$ (Empty/Full) and $\overline{HF}$ (Half Full). These pins can be decoded to determine one of four states. Two 9-bit data ports are provided. The direction selected for the FIFO determines the input and output ports. The FIFO direction can be programmed by the user at any time through the use of the reset pin ($\overline{MR}$) and the bypass/direction pin ($\overline{BYPA}$). There are no control or status registers on the CY7C439, making the part simple to use while meeting the needs of the majority of bidirectional FIFO applications.

FIFO read and write operations may occur simultaneously, and each can occur at up to 28.5 MHz. The port designated as the write port drives its strobe pin ($\overline{STBX}$, X = A or B) LOW to initiate the write operation. The port designated as the read port drives its strobe pin LOW to initiate the read operation. Output port pins go to a high-impedance state when the associated strobe pin is HIGH. All normal FIFO operations require the bypass control pin ($\overline{BYPX}$, X = A or B) to remain HIGH.

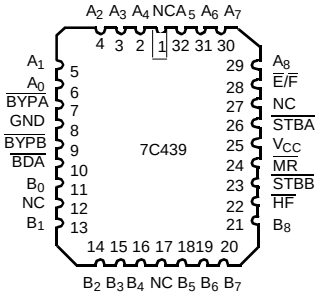
In addition to the FIFO, two other data paths are provided; registered bypass and transparent bypass. Registered bypass can be considered as a single-word FIFO in the reverse direction to the main FIFO. The

Logic Block Diagram



Pin Configurations

PLCC/LCC Top View



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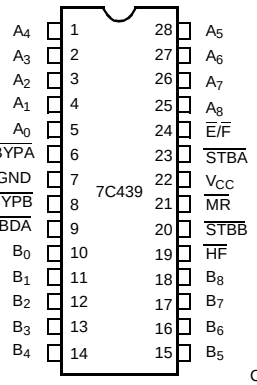
DIP Top View



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Selection Guide

		7C439-25	7C439-30	7C439-40	7C439-65
Frequency (MHz)		28.5	25	20	12.5
Maximum Access Time (ns)		25	30	40	65
Maximum Operating Current (mA)	Commercial	147	140	130	115
	Military		170	160	145

Functional Description (continued)

bypass register provides a means of sending a 9-bit status or control word to the FIFO-write port. The bypass data available pin ($\overline{BDA}$) indicates whether the bypass register is full or empty. The direction of the bypass register is always opposite to that of the main FIFO.

The port designated to write to the bypass register drives its bypass control pin ($\overline{BYPX}$) LOW. The other port detects the presence of data by monitoring $\overline{BDA}$ and reads the data by driving its bypass control pin ($\overline{BYPX}$) LOW. Registered bypass operations require that the associated FIFO strobe pin ($\overline{STBX}$) remains HIGH. Registered bypass operations do not affect data residing in the FIFO, or FIFO operations at the other port.

Transparent bypass provides a means of transferring a single word (9 bits) of data immediately in either direction. This feature allows the device to act as a simple 9-bit bidirectional buffer. This is useful for allowing the controlling circuitry to access a dumb peripheral for control/programming information.

For transparent bypass, the port wishing to send immediate data to the other side drives both its bypass and its strobe pins LOW simultaneously. This causes the buffered data to be driven out of the other port. On-chip circuitry detects conflicting use of the control pins and causes both data ports to enter a high-impedance state until the conflict is resolved.

Additionally, a Test mode is offered on the CY7C439. This mode allows the user to load data into the FIFO and then read it back out of the same port. Built-In Self Test (BIST) and diagnostic functions can take advantage of these features.

The CY7C439 is fabricated using an advanced 0.8µ N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by reliable layout techniques, guard rings, and a substrate bias generator.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0V

DC Input Voltage ..... –3.0V to +7.0V

Power Dissipation 1.0W

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	–55°C to +125°C	5V ± 10%

Notes:
1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
$A_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPA}$ and $\overline{STBA}$
$B_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPB}$ and $\overline{STBB}$
$\overline{BYPA}$	I	Registered Bypass Mode Select for A Side
$\overline{BYPB}$	I	Registered Bypass Mode Select for B Side
$\overline{BDA}$	O	Bypass Data Available Flag
$\overline{STBA}$	I	Data Strobe for A Side
STBB	I	Data Strobe for B Side
$\overline{E/F}$	O	Encoded Empty/Full Flag
$\overline{HF}$	O	Half Full Flag
MR	I	Master Reset

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions		7C439-25		7C439-30		7C439-40		7C439-65		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -2.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Com'l	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
			Mil			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			–3.0	0.8	–3.0	0.8	–3.0	0.8	–3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	$\overline{STBX}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l[3]		147		140		130		115	mA
			Mil[4]				170		160		145	
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Com'l		40		40		40		40	mA
			Mil				45		45		45	
I_{SB2}	Power-Down Current	All Inputs V_{CC} - 0.2V	Com'l		20		20		20		20	mA
			Mil				25		25		25	
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND			–90		–90		–90		–90	mA

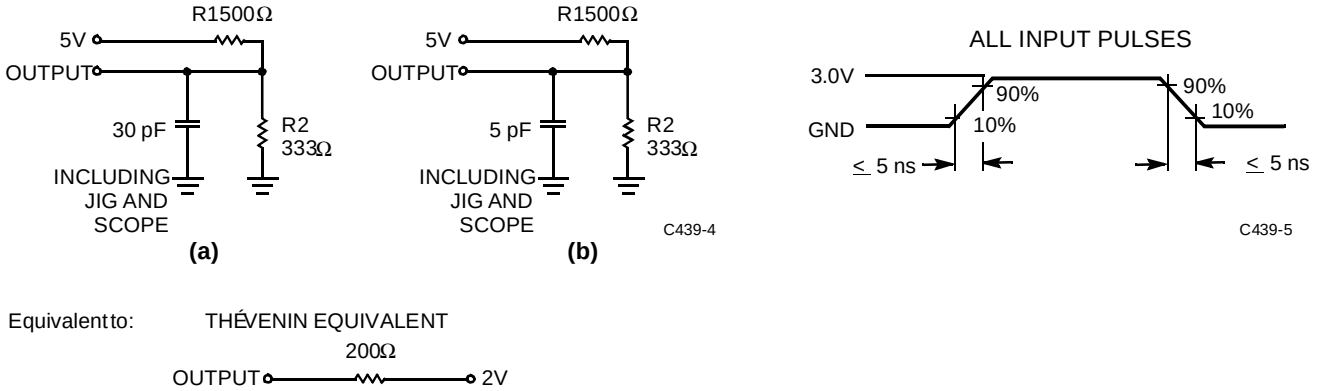
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 4.5V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

2. See the last page of this specification for Group A subgroup testing information.
3. I_{CC} (commercial) = 115 mA + [(f - 12.5) • 2 mA/MHz] for f ≥ 12.5 MHz where f = the larger of the write or read operating frequency.
4. I_{CC} (military) = 145 mA + [(f - 12.5) • 2 mA/MHz] for f ≥ 12.5 MHz where f = the larger of the write or read operating frequency.
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveform



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[2, 7]

Parameter	Description	7C439-25		7C439-30		7C439-40		7C439-65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		40		50		80		ns
t_{A}	Access Time		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		15		ns
t_{PR}	Read Pulse Width	25		30		40		65		ns
t_{LZR}[8, 9]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[8, 9]	Data Valid from Read HIGH	3		3		3		3		ns
t_{HZR}[8, 9]	Read HIGH to High Z		18		20		25		30	ns
t_{WC}	Write Cycle Time	35		40		50		80		ns
t_{PW}	Write Pulse Width	25		30		40		65		ns
t_{HWZ}[8, 9]	Write HIGH to Low Z	10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		15		ns
t_{SD}	Data Set-Up Time	15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		15		ns
t_{RPS}	$\overline{STBX}$ HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{RPBS}	$\overline{BYPA}$ to $\overline{MR}$ HIGH	10		10		15		20		ns
t_{RPBH}	$\overline{BYPA}$ Hold after $\overline{MR}$ HIGH	0		0		0		0		ns
t_{BDH}	$\overline{MR}$ LOW to $\overline{BDA}$ HIGH		35		40		50		80	ns
t_{BSR}	$\overline{STBX}$ HIGH to $\overline{BYPA}$ LOW	10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{E}/\overline{F}$ LOW		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{BRS}	$\overline{BYPX}$ HIGH to $\overline{STBX}$ LOW	10		10		10		15		ns
t_{REF}	$\overline{STBX}$ LOW to $\overline{E}/\overline{F}$ LOW (Read)		25		30		35		60	ns
t_{RFF}	$\overline{STBX}$ HIGH to $\overline{E}/\overline{F}$ HIGH (Read)		25		30		35		60	ns
t_{WEF}	$\overline{STBX}$ HIGH to $\overline{E}/\overline{F}$ HIGH (Write)		25		30		35		60	ns

Switching Characteristics Over the Operating Range[2, 7] (Continued)

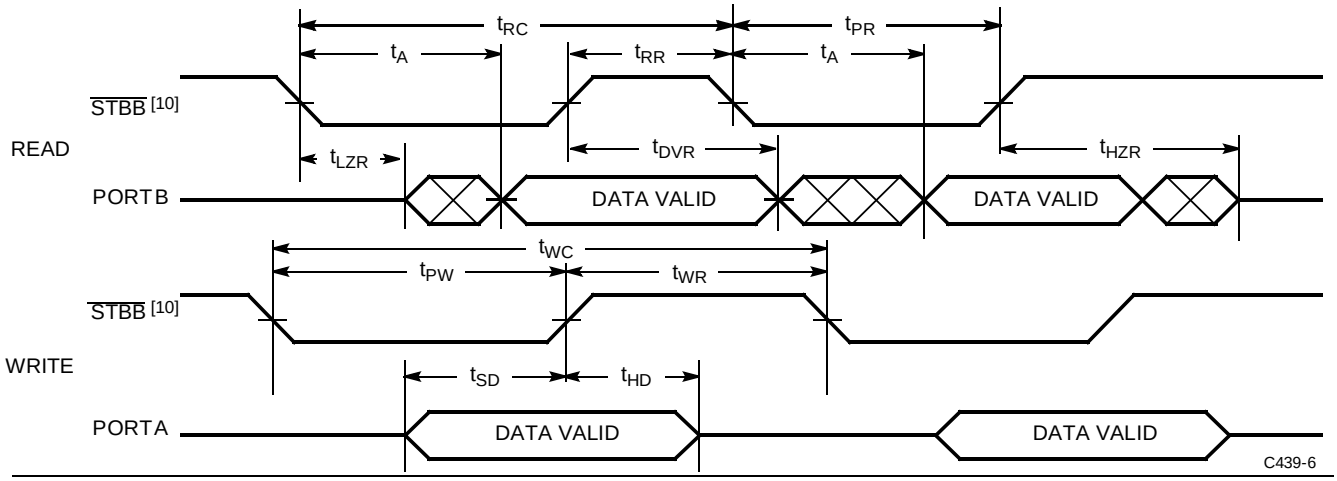
Parameter	Description	7C439-25		7C439-30		7C439-40		7C439-65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WFF}	$\overline{STBX}$ LOW to $\overline{E}/\overline{F}$ LOW (Write)		25		30		35		60	ns
t_{BDA}	$\overline{BYPX}$ HIGH to $\overline{BDA}$ LOW (Write)		25		30		35		60	ns
t_{BDB}	$\overline{BYPX}$ HIGH to $\overline{BDA}$ HIGH (Read)		25		30		35		60	ns
t_{BA}	$\overline{BYPX}$ LOW to Data Valid (Read)		30		30		40		60	ns
t_{BHZ}[8, 9]	$\overline{BYPX}$ HIGH to High Z (Read)		18		20		25		30	ns
t_{TSB}	$\overline{STBX}$ HIGH to $\overline{BYPX}$ LOW Set-Up	10		10		10		15		ns
t_{TBS}	$\overline{STBX}$ LOW after $\overline{BYPX}$ LOW	0	10	0	10	0	10	0	10	ns
t_{TSN}	$\overline{STBX}$ HIGH Recovery Time	10		10		10		15		ns
t_{TSD}[8, 9]	$\overline{STBX}$ HIGH to Data High Z		18		20		25		30	ns
t_{TBN}	$\overline{BYPX}$ HIGH Recovery Time	10		10		10		15		ns
t_{TBD}	$\overline{BYPX}$ HIGH to Data High Z		18		20		25		30	ns
t_{TPD}[8, 9]	$\overline{STBX}$ LOW to Data Valid		20		20		30		55	ns
t_{DL}	Transparent Propagation Delay		20		20		25		30	ns
t_{ESD}[8, 9]	$\overline{STBX}$ LOW to High Z		18		20		25		30	ns
t_{EBD}[8, 9]	$\overline{BYPX}$ LOW to High Z		18		20		25		30	ns
t_{EDS}	$\overline{STBX}$ HIGH to Low Z		18		20		25		30	ns
t_{EDB}	$\overline{BYPX}$ HIGH to Low Z		18		20		25		30	ns
t_{BPW}	$\overline{BYPX}$ Pulse Width (Trans.)	25		30		40		65		ns
t_{TSP}	$\overline{STBX}$ Pulse Width (Trans.)	20		20		30		55		ns
t_{BLZ}[8, 9]	$\overline{BYPX}$ LOW to Low Z (Read)	10		10		10		10		ns
t_{BDV}	$\overline{BYPX}$ HIGH to Data Invalid (Read)	3		3		3		3		ns
t_{WHF}	$\overline{STBX}$ LOW to $\overline{HF}$ LOW (Write)		35		40		50		80	ns
t_{RHF}	$\overline{STBX}$ HIGH to $\overline{HF}$ HIGH (Read)		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{E}/\overline{F}$ HIGH	25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{E}/\overline{F}$ HIGH	25		30		40		65		ns
t_{BSU}	Bypass Data Set-Up Time	15		18		20		30		ns
t_{BHL}	Bypass Data Hold Time	0		0		0		10		ns

Notes:

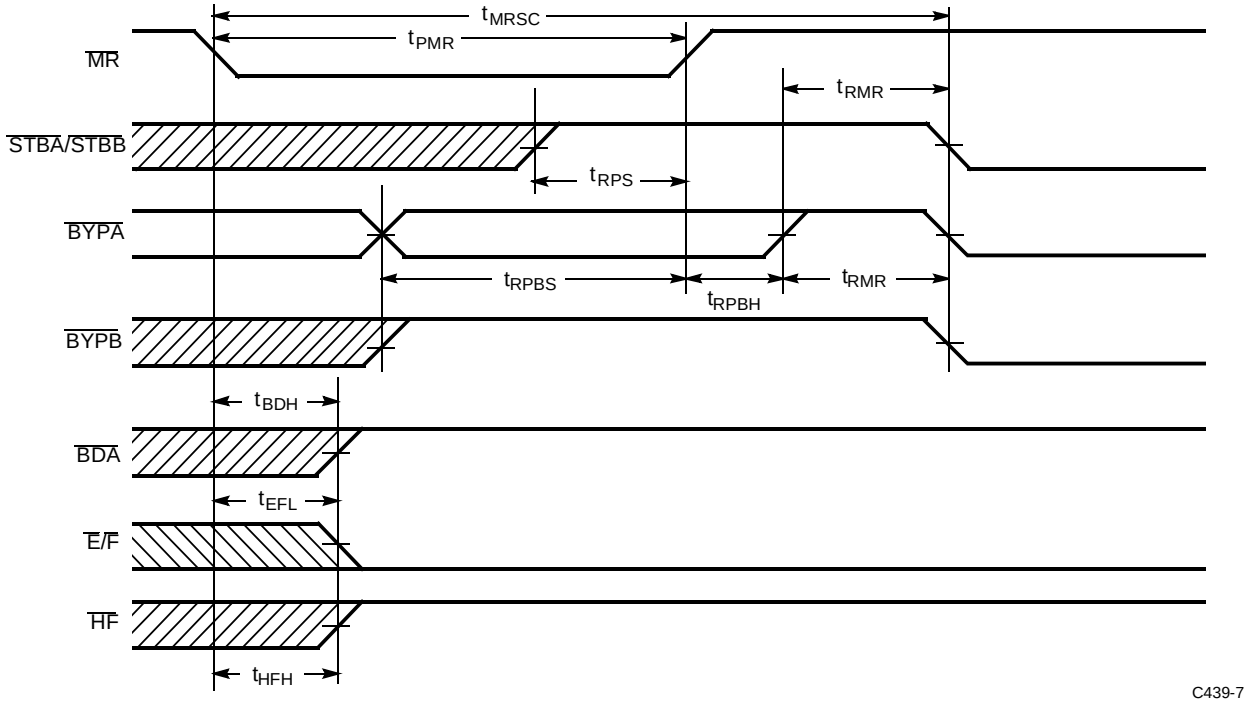
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance as in part (a) of AC Test Loads, unless otherwise specified.
8. t_{DVR}, t_{BDV}, t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, t_{TSD}, t_{LZR}, t_{HWZ}, and t_{BLZ} use capacitance loading as in part (b) of AC Test Loads.
9. t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, and t_{TSD} transition is measured at +500 mV from V_{OL} and - 500 mV from V_{OH}. t_{DVR} and t_{BDV} transition is measured at the 1.5V level. t_{LZR}, t_{HWZ}, and t_{BLZ} transition is measured at ±100 mV from the steady state.

Switching Waveforms

Asynchronous Read and Write Timing Diagram

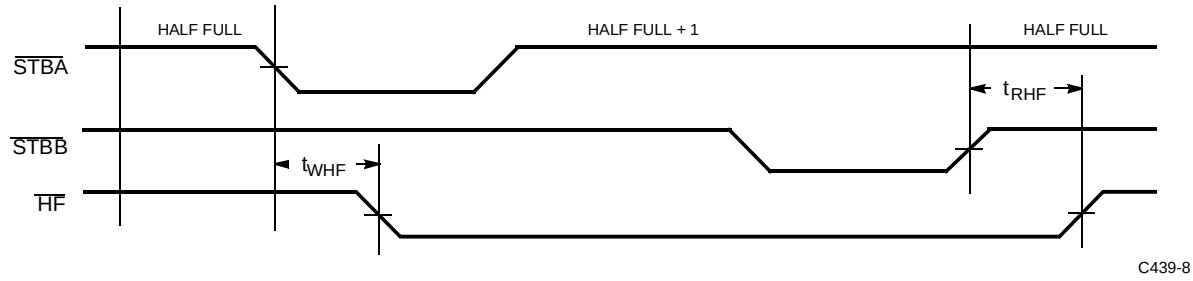


Master Reset Timing Diagram

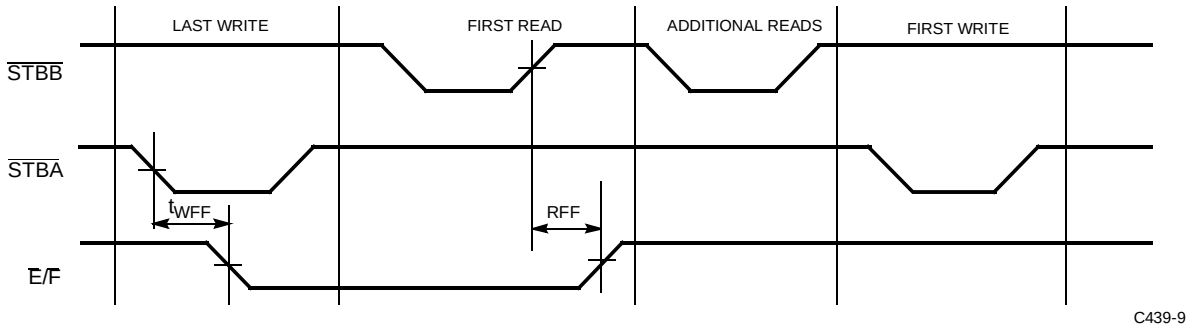


Switching Waveforms (Continued)

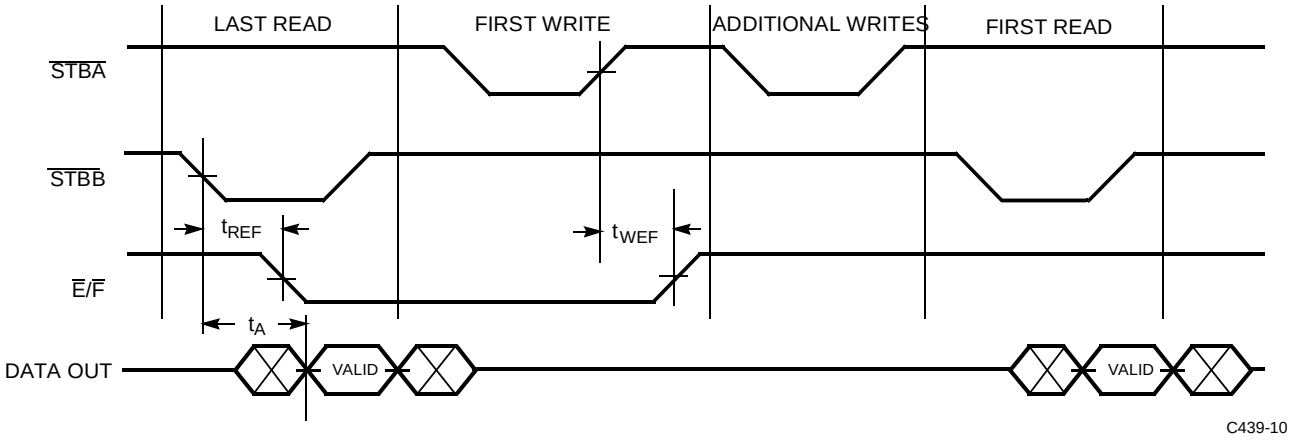
Half–Full Flag Timing Diagram[11]



Last Write to First Read Empty/Full Flag Timing Diagram[11]



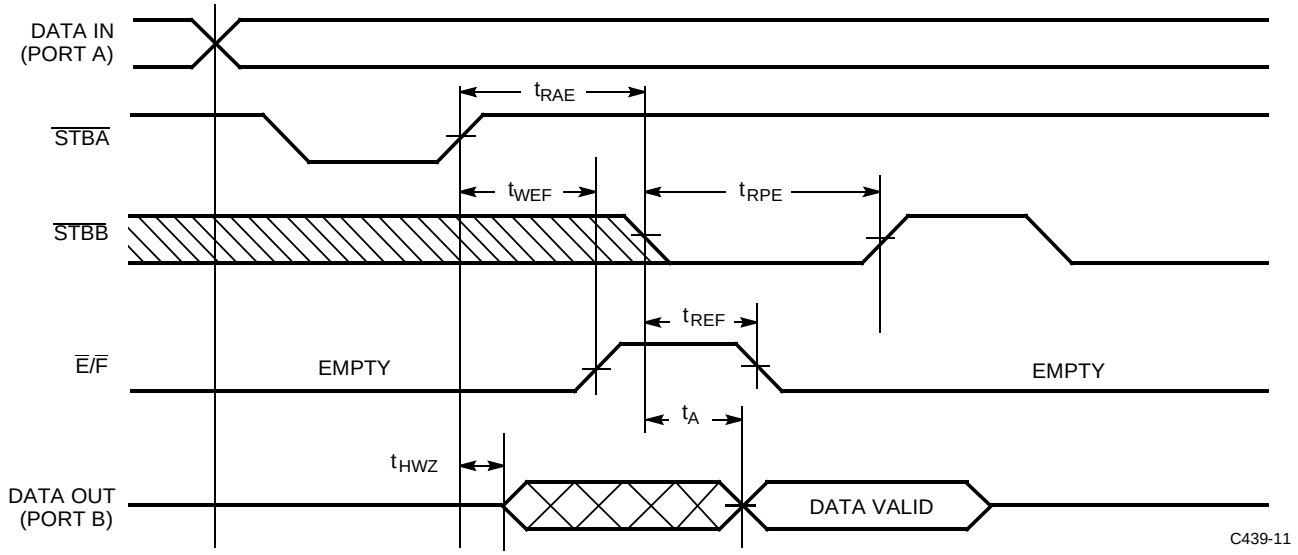
Last Read to First Write Empty/Full Flag Timing Diagram[11]



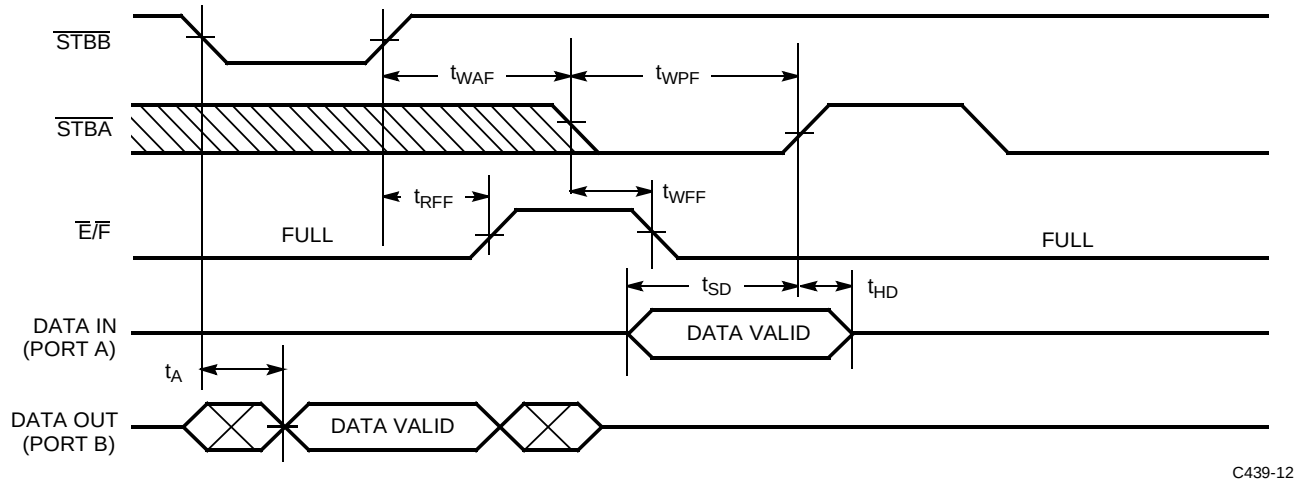
Notes:
10. Direction selected Port A to Port B.
11. Direction selected as A to B.

Switching Waveforms (Continued)

Empty/Full Flag and Read Bubble–Through Mode Timing Diagram[11]

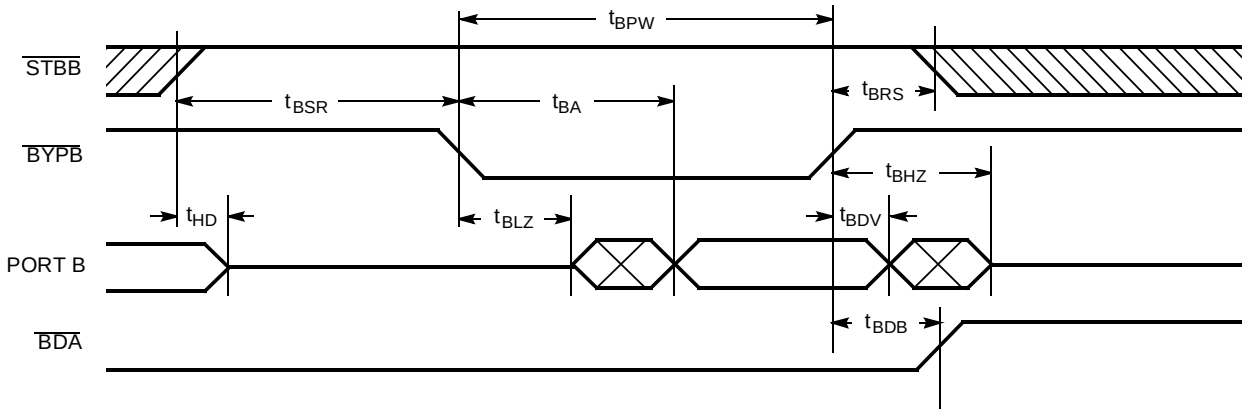


Empty/Full Flag and Write Bubble–Through Mode Timing Diagram[11]



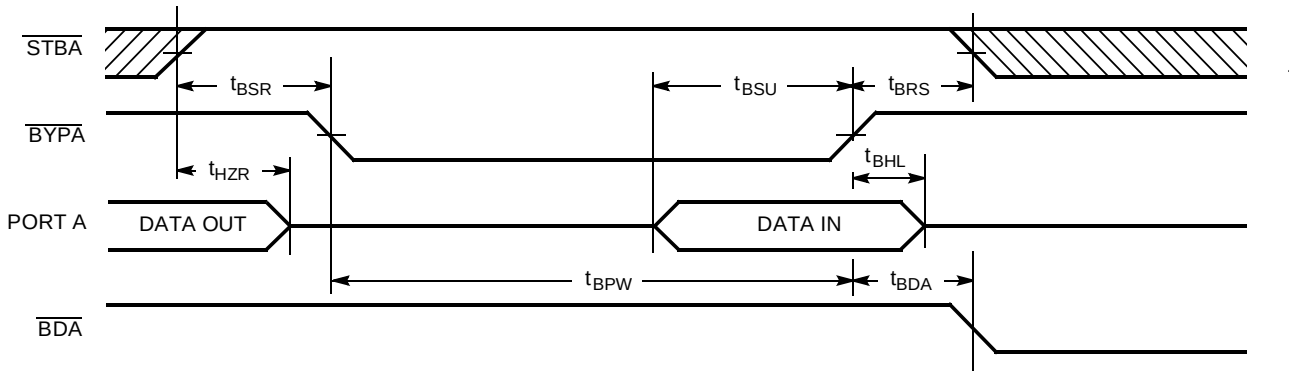
Switching Waveforms (Continued)

Registered Bypass Read Timing Diagram[12]



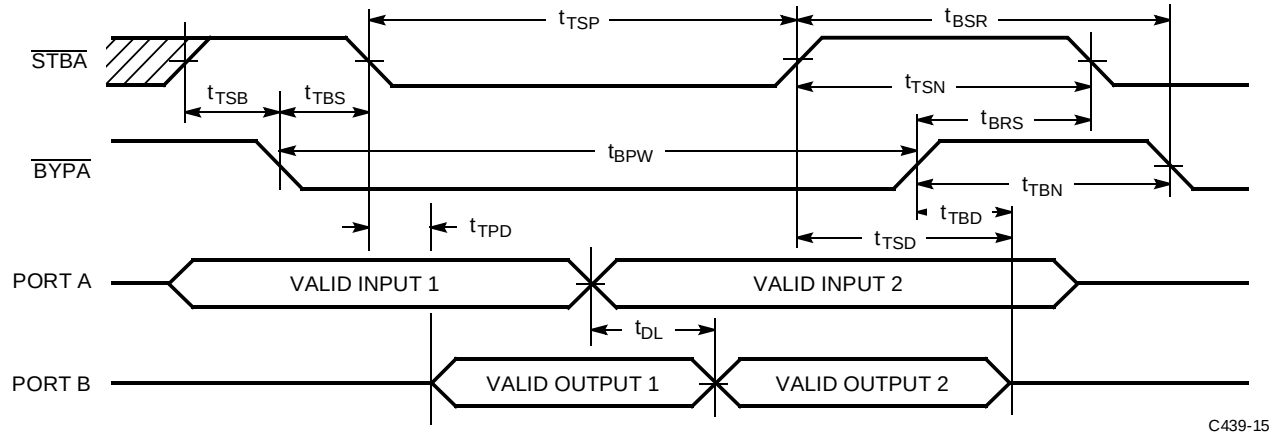
C439-13

Registered Bypass Write Timing Diagram[13]



C439-14

Transparent Bypass Read Timing Diagram[14]



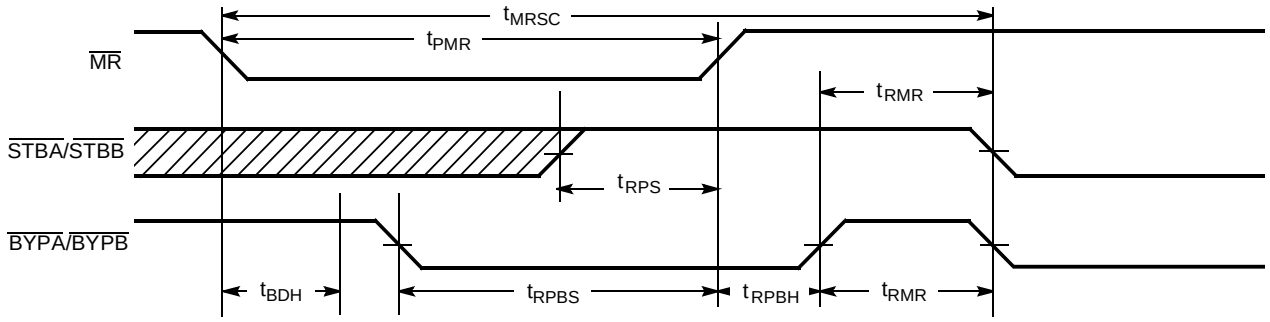
C439-15

Notes:

12. Port B selected to read bypass register (FIFO direction Port B to Port A).
13. Port A selected to write bypass register (FIFO direction Port B to Port A.
14. Diagram shows transparent bypass initiated by Port A. Times are identical if initiated by Port B.

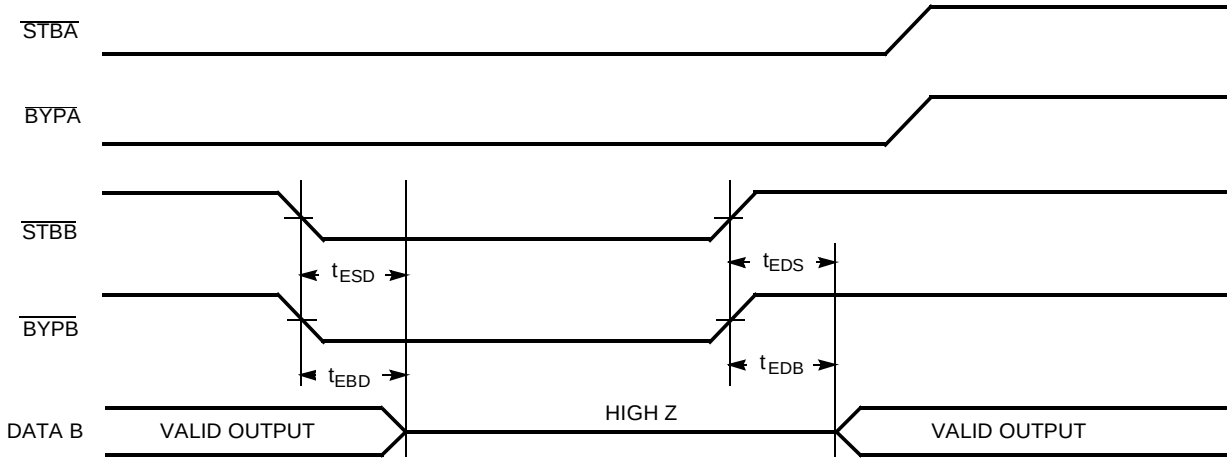
Switching Waveforms (Continued)

Test Mode Timing Diagram



C439-16

Exception Condition Timing Diagram[14]



C439-17

Architecture

The CY7C439 consists of a 2048 by 9-bit dual-ported RAM array, a read pointer, a write pointer, data switching circuitry, buffers, a bypass register, control signals ($\overline{STBA}$, $\overline{STBB}$, $\overline{BYPA}$, $\overline{BYPB}$, $\overline{MR}$), and flags ($\overline{E}/\overline{F}$, $\overline{HF}$, $\overline{BDA}$).

Operation at Power-On

Upon power-up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. During an $\overline{MR}$ cycle, the user can initialize the device by choosing the direction of FIFO operation (see *Table 1*). There is a minimum LOW period for $\overline{MR}$, but no maximum time. The state of $\overline{BYPA}$ is latched internally by the rising edge of $\overline{MR}$ and used to determine the direction of subsequent data operations.

Resetting the FIFO

During the reset condition (see *Table 1*), the FIFO three-states the data ports, sets $\overline{BDA}$ and $\overline{HF}$ HIGH, $\overline{E}/\overline{F}$ LOW, and ignores the state of $\overline{BYPA}/B$ and $\overline{STBA}/B$. The bypass registers are initialized to zero. During this time the user is expected to set the direction of the FIFO by driving $\overline{BYPA}$ HIGH or LOW, and $\overline{BYPB}$, $\overline{STBA}$, and $\overline{STBB}$ HIGH. If $\overline{BYPA}$ is LOW (selecting direction B>A), the FIFO will then remain in a reset condition until the user terminates the reset operation by driving $\overline{BYPA}$ HIGH. If $\overline{BYPA}$ is HIGH (selecting direction A>B), the reset condition terminates after the rising edge of $\overline{MR}$. The entire reset phase can be accomplished in one cycle time of tRC.

FIFO Operation

The operation of the FIFO requires only one control pin per port ($\overline{STBX}$). The user determines the direction of the FIFO data flow by initiating an $\overline{MR}$ cycle (see *Table 1*), which clears the FIFO and bypass register and sets the data path and control signal multiplexers. The bypass register is configured in the opposite direction to the FIFO data flow. The FIFO direction can be reversed at any time by initiating another $\overline{MR}$ cycle. Data is written into the FIFO on the rising edge of the input, $\overline{STBX}$, and read from the FIFO by a low level at the output, $\overline{STBX}$. The two ports are asynchronous and independent. If the user attempts to read the FIFO when it is empty, no action takes place (the read pointer is not incremented) until the other port writes to the FIFO. Then a bubble-through read takes place, in which the read strobe is generated internally and the data becomes available at the read port shortly thereafter if the read strobe ($\overline{STBX}$) is still LOW. Similarly, for an attempted write operation when the FIFO is full, no internal operation takes place until the other port performs a read operation, at

which time the bubble-through write is performed if the write strobe ($\overline{STBX}$) is still LOW.

Registered Bypass Operation

The registered bypass feature provides a means of transferring one 9-bit word of data in the opposite direction to normal data flow without affecting either the FIFO contents or the FIFO write operations at the other port. The bypass register is configured during reset to provide a data path in the opposite direction to that of the FIFO (see *Table 1*). For example, if port A is writing data to the FIFO (hence port B is reading data from the FIFO) then $\overline{BYPB}$ is used to write to the bypass register at port B, and $\overline{BYPA}$ is used to read a single word from the bypass register at port A. The bypass data available flag ($\overline{BDA}$) is generated to notify port A that bypass data is available. $\overline{BDA}$ goes true on the trailing edge of the $\overline{BYPX}$ write operation and false upon the trailing edge of the $\overline{BYPX}$ read operation.

Data is written on the rising edge of $\overline{BYPX}$ into the bypass register for later retrieval by the other port, regardless of the state of $\overline{BDA}$. The bypass register is read by a low level at $\overline{BYPX}$, regardless of the state of $\overline{BDA}$.

Transparent Bypass Operation

The transparent bypass feature provides a means of sending immediate data “around” the FIFO in either direction. The FIFO contents are not affected by the use of transparent bypass, but the control signals for transparent bypass are shared with those of the normal FIFO operation. Hence there are limitations on the use of transparent bypass to ensure that data integrity and ease of use are preserved. The port wishing to send immediate data must ensure that the other port will not attempt a FIFO read or write during the transparent bypass cycle. If this is not possible, registered bypass or external circuitry should be used.

Transparent bypass mode is initiated by bringing both $\overline{BYPA}$ and $\overline{STBA}$ LOW together. Care should be taken to observe the following constraints on the timing relationships. Since $\overline{STBA}$ is used for normal FIFO operations, it must follow $\overline{BYPA}$ falling edge by tTBS to prevent erroneous FIFO read or write operations. Since $\overline{BYPA}$ is used alone to initiate registered bypass read and write, it is internally delayed before initiating registered bypass. If $\overline{STBA}$ falls during this time, delay registered bypass is averted, and transparent bypass is initiated. Identical arguments apply to $\overline{BYPB}$ and $\overline{STBB}$.

If a transparent bypass sequence is successfully accomplished, data presented to the initiating port (port A in the above discussion) will be buffered to the other (port B) after tDL. Either port can initiate a transparent bypass operation at any time, but if the control signals ($\overline{STBA}$/$\overline{B}$, $\overline{BYPA}$/$\overline{B}$) are in conflict (exception condition), internal circuitry will switch both ports to high-impedance until the conflict is resolved.

Test Mode Operation

The Test mode feature provides a means of reading the FIFO contents from the same port that the data was written to the FIFO. This feature is useful for Built-In Self Test (BIST) and diagnostic functions. To utilize this capability, initialize FIFO direction A to B and load data into the FIFO using normal write timing. In order to read data back out of the same port (port A), initiate a $\overline{MR}$ cycle with both $\overline{BYPA}$ and $\overline{BYPB}$ LOW (see Test Mode Timing diagram). After completing the cycle, the data can be read out of port A in FIFO order. Data will be inverted when read out of the device. Also, flags are not valid when reading data.

Flag Operation

There are two flags, Empty/Full ($\overline{E}/\overline{F}$) and Half Full ($\overline{HF}$), which are used to decode four FIFO states (see *Table 4*). The states are empty, 1-1024 locations full, 1025-2047 locations full, and full. Note that two conditions cause the $\overline{E}/\overline{F}$ pin to go LOW, Empty and Full, hence both flag pins must be used to resolve the two conditions.

Table 1. FIFO Direction Select Truth

$\overline{MR}$	$\overline{BYPA}$	$\overline{BYPB}$	$\overline{STBA}$	$\overline{STBB}$	Action
1	X	X	X	X	Normal Operation
⌐	1	1	1	1	FIFO Direction A to B, Registered Bypass Direction B to A
⌐	0	1	1	1	FIFO Direction B to A, Registered Bypass Direction A to B
0	X	X	X	X	Reset Condition

Table 2. Bypass Operation Truth Table

Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYPB}$	Action
A Á B	⌐¬	1	⌐¬	1	Normal FIFO Operations, Write at A, Read at B
A Á B	1	⌐¬	⌐¬	1	Normal FIFO Read at B, Bypass Register Read at A
A Á B	⌐¬	1	1	⌐¬	Normal FIFO Write at A, Bypass Register Write at B

Table 2. Bypass Operation Truth Table

B Á A		1		1	Normal FIFO Operations, Write at B, Read at A
B Á A	1			1	Normal FIFO Write at B, Bypass Register Write at A
B Á A		1	1		Normal FIFO Read at A, Bypass Register Read at B
X	0	0	1	1	No FIFO Operations, Transparent Data A to B
X	1	1	0	0	No FIFO Operations, Transparent Data B to A

Table 3. Exception Conditions: Operation Not Defined

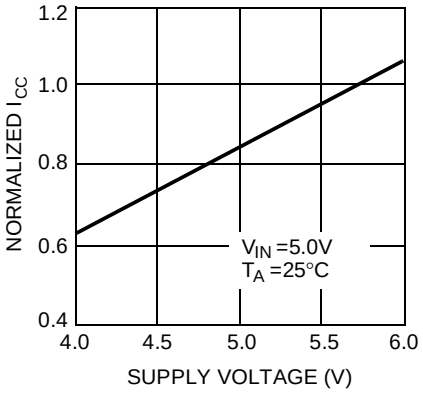
Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYBP}$	Action
X	0	1	0	0	Data Buses High Impedance
X	1	0	0	0	Data Buses High Impedance
X	0	0	0	0	Data Buses High Impedance
X	0	0	1	0	Data Buses High Impedance
X	0	0	0	1	Data Buses High Impedance

Table 4. Flag Truth Table.

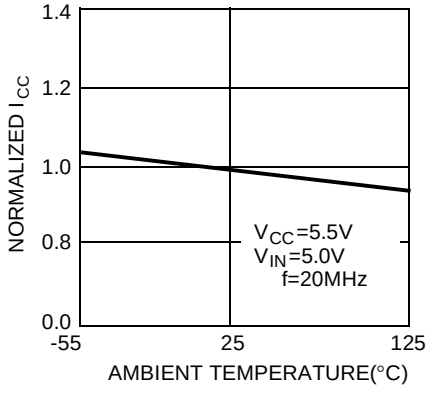
$\overline{E}/\overline{F}$	HF	State
0	1	Empty
1	1	1-1024 Locations Full
1	0	1025-2047 Locations Full
0	0	Full

Typical DC and AC Characteristics

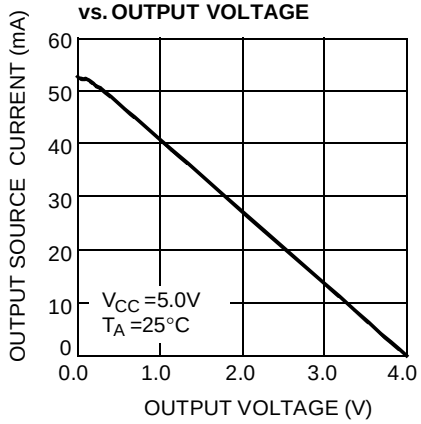
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



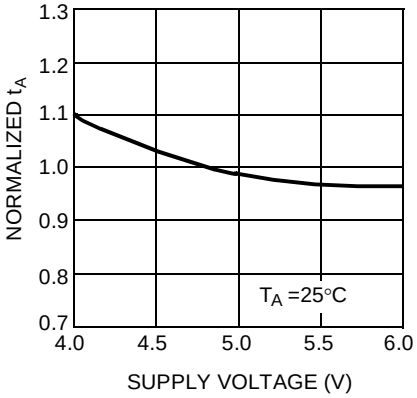
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



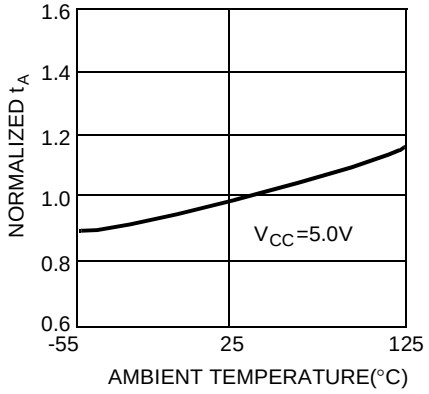
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



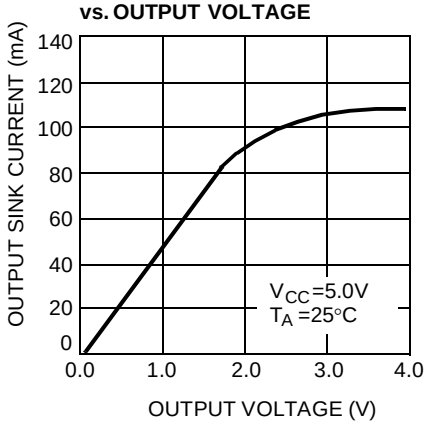
NORMALIZED t_A vs. SUPPLY VOLTAGE



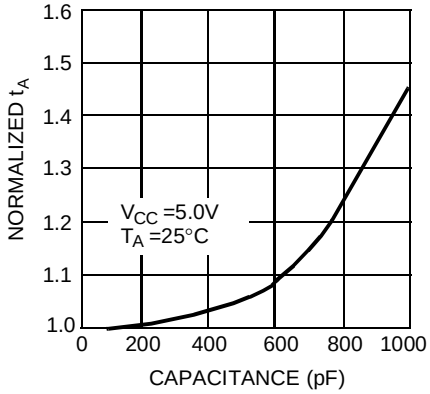
NORMALIZED t_A vs. AMBIENT TEMPERATURE



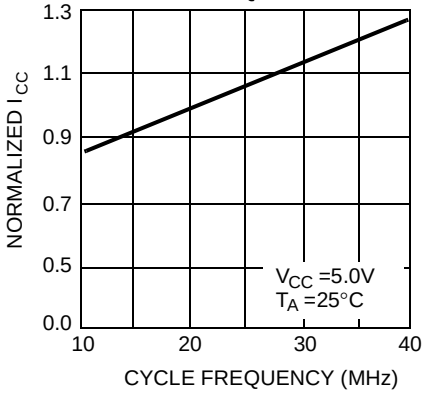
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED t_A CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE FREQUENCY



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7C439-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439-25PC	P21	28-Lead (300-Mil) Molded DIP	
30	CY7C439-30JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439-30PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C439-30DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439-30LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
40	CY7C439-40JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439-40PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C439-40DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439-40LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
6.5	CY7C439-65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C439-65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C439-65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C439-65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{OS}	1, 2, 3
I_{OZ}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9, 10, 11
t_{A}	9, 10, 11
t_{RR}	9, 10, 11
t_{PR}	9, 10, 11
t_{LZR}	9, 10, 11
t_{DVR}	9, 10, 11
t_{HZR}	9, 10, 11
t_{WC}	9, 10, 11
t_{PW}	9, 10, 11
t_{HWZ}	9, 10, 11
t_{WR}	9, 10, 11
t_{SD}	9, 10, 11
t_{HD}	9, 10, 11
t_{MRSC}	9, 10, 11
t_{PMR}	9, 10, 11
t_{RMR}	9, 10, 11
t_{RPS}	9, 10, 11
t_{RPBS}	9, 10, 11
t_{RPBH}	9, 10, 11
t_{BDH}	9, 10, 11
t_{BSR}	9, 10, 11

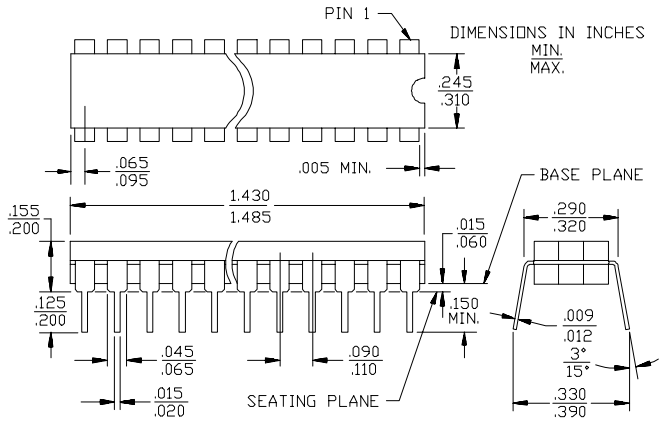
Switching Characteristics

Parameters	Subgroups
t_{EFL}	9, 10, 11
t_{HFH}	9, 10, 11
t_{BRS}	9, 10, 11
t_{REF}	9, 10, 11
t_{RFF}	9, 10, 11
t_{WEF}	9, 10, 11
t_{WFF}	9, 10, 11
t_{WHF}	9, 10, 11
t_{RHF}	9, 10, 11
t_{RAE}	9, 10, 11
t_{RPE}	9, 10, 11
t_{WAF}	9, 10, 11
t_{WPF}	9, 10, 11
t_{BSU}	9, 10, 11
t_{BHL}	9, 10, 11
t_{BDA}	9, 10, 11
t_{BDB}	9, 10, 11
t_{BA}	9, 10, 11
t_{BHZ}	9, 10, 11
t_{TSB}	9, 10, 11
t_{TBS}	9, 10, 11
t_{TSN}	9, 10, 11
t_{TSD}	9, 10, 11
t_{TBN}	9, 10, 11
t_{TBD}	9, 10, 11
t_{TPD}	9, 10, 11
t_{DL}	9, 10, 11
t_{ESD}	9, 10, 11
t_{EBD}	9, 10, 11
t_{EDS}	9, 10, 11
t_{EDB}	9, 10, 11
t_{BPW}	9, 10, 11
t_{TSP}	9, 10, 11
t_{BLZ}	9, 10, 11
t_{BDV}	9, 10, 11

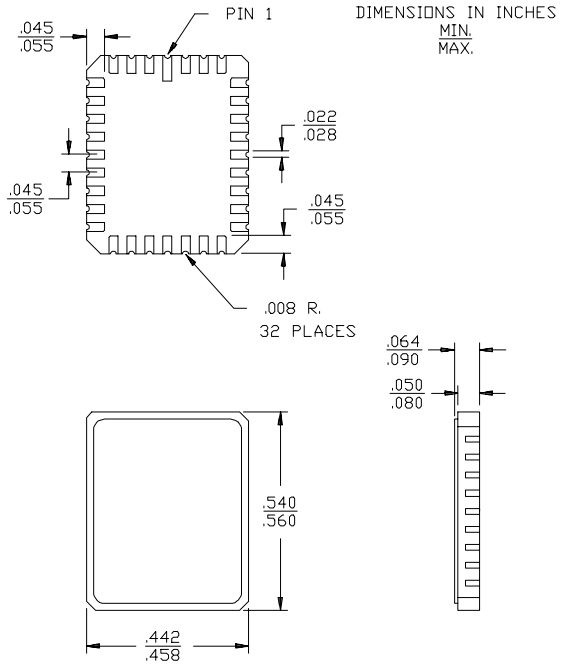
Document #: 38-00126-D

Package Diagrams

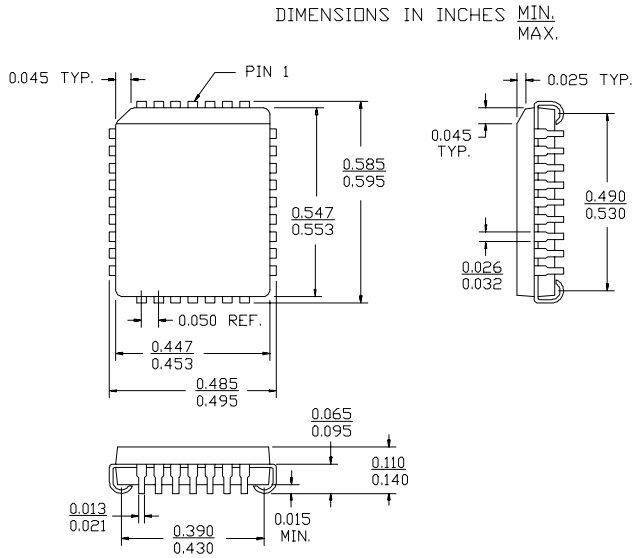
28–Lead (300–Mil) CerDIP D22
MIL-STD-1835 D-15Config.A



32–Pin Rectangular Leadless Chip Carrier L55
MIL-STD-1835 C-12



32–Lead Plastic Leaded Chip Carrier J65



Package Diagrams (Continued)

28–Lead (300–Mil) Molded DIP P21