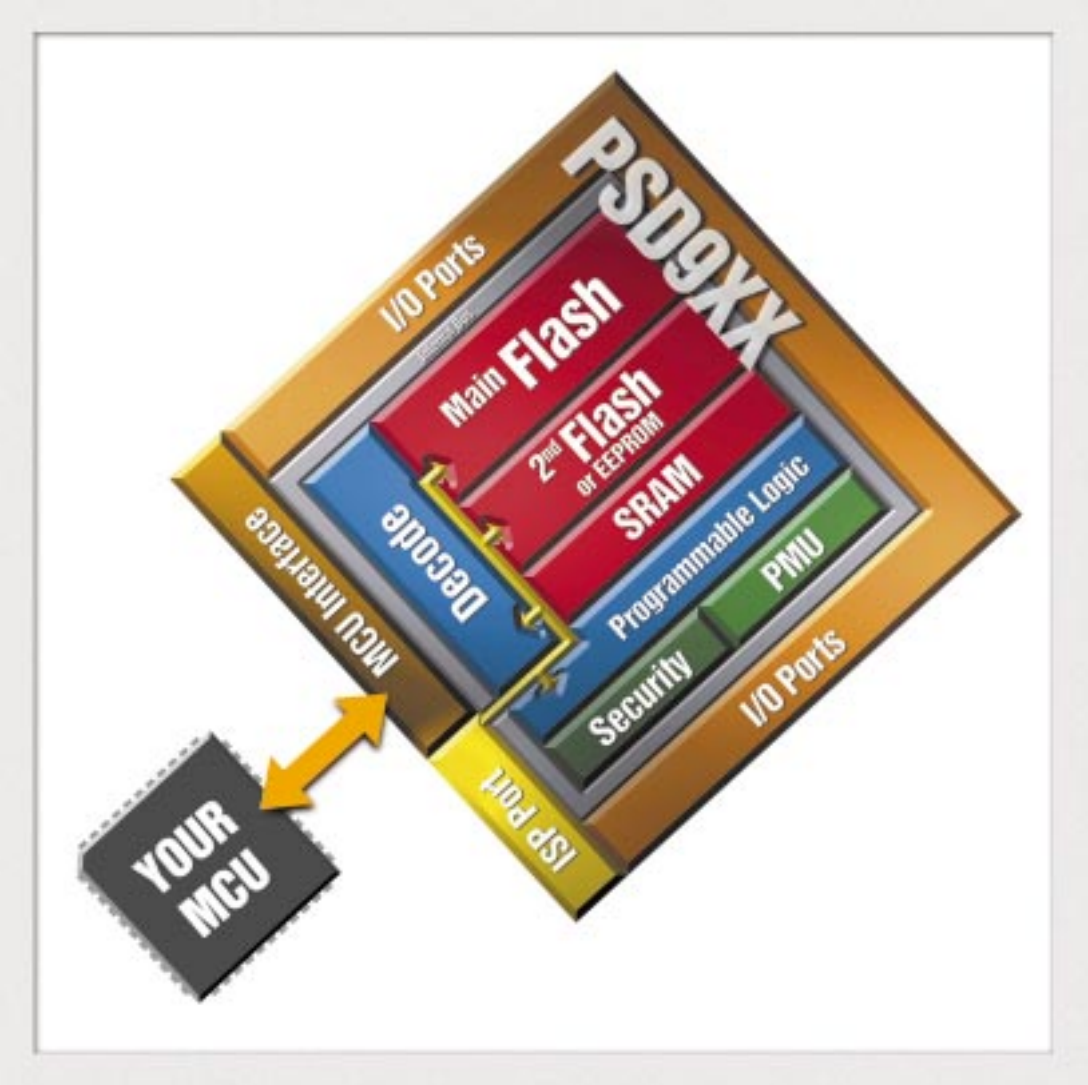
PSD9XX Family Product Brief

PSD913F2 PSD934F2

Configurable Memory System on a Chip for 8-Bit Microcontrollers

January, 2000
Preliminary



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PSD9XX Family Product Brief

PSD913F2 PSD934F2

Configurable Memory System on a Chip for 8-Bit Microcontrollers

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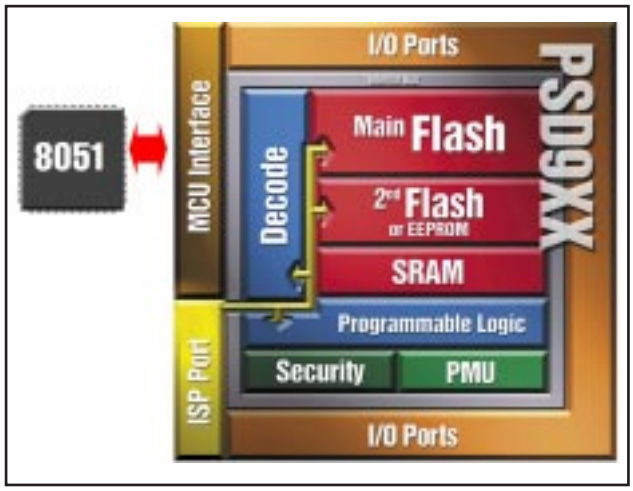
PSD913F2, PSD934F2

Configurable Memory System on a Chip for 8-Bit Microcontrollers

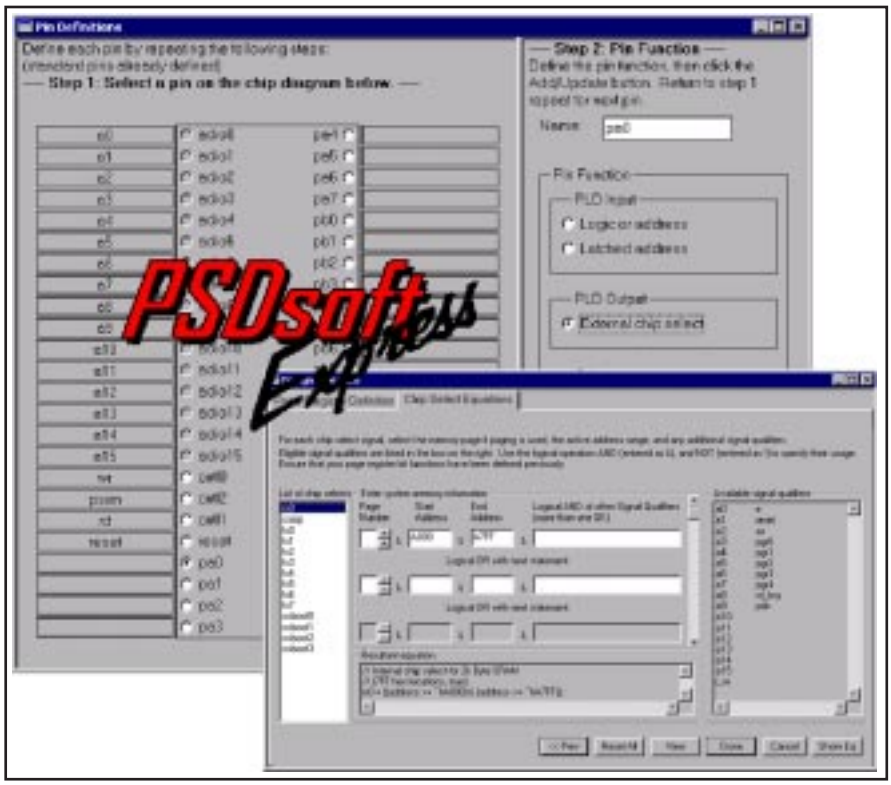
Product Brief

New! EasyFLASH™ PSD9XX

An EasyFLASH™ PSD, Programmable System Device, is the first configurable memory system for your MCU to offer In-System Programmability (ISP) of blank devices. This is accomplished via a 4 pin ISP port, based on the JTAG standard, which allows code to flow directly into the PSD memory banks by-passing the MCU. As a result, blank devices can be soldered onto the circuit board, and programmed at the end of the assembly line, thus eliminating the need to inventory pre-programmed devices. EasyFLASH PSDs also offer concurrent memory arrays, to support In-Application re-Programmability (IAP), which allows execution out of one memory array, while the other is being updated, and vice versa.



The EasyFLASH PSD9XX family, integrates up to 2Mbits of Flash, 256Kbits of concurrent Flash or EEPROM, up to 64Kbits of SRAM, additional I/O, power management, a security feature, and advanced ISP options onto a single chip. They are 100% configurable with PSDsoft Express, and programmable via the ISP port, your MCU's serial port, or a third party device programmer.



PSDsoft Express™ Simple! Point and Click Configuration.

PSDsoft ExpressTM allows for complete configuration of the PSD9XX family of PSDs. The simple point and click environment automatically configures the microcontroller interface based on the selected MCU, and then proceeds to step the designer through configuration, all the way through to programming your code and firmware into the PSD. It's never been easier to increase the functionality of your embedded design. Visit www.waferscale.com to download your embedded design. Visit www.waferscale.com to download your FREE fully functional copy of PSDsoft Express today!

1.0 Introduction

The PSD9XX family of Programmable System Devices (PSD) for 8-bit microcontrollers, brings In-System-Programmability (ISP) to Flash memory and programmable logic. The result is a simple and flexible solution for embedded designs. PSD9XX devices combine many of the peripheral functions found in MCU based applications:

- Up to 2 Mbit of Flash memory
- A secondary 256 Kbit Flash memory
- Over 2,000 gates of Flash programmable logic
- Up to 64 Kbit SRAM
- Reconfigurable I/O ports
- Programmable power management.

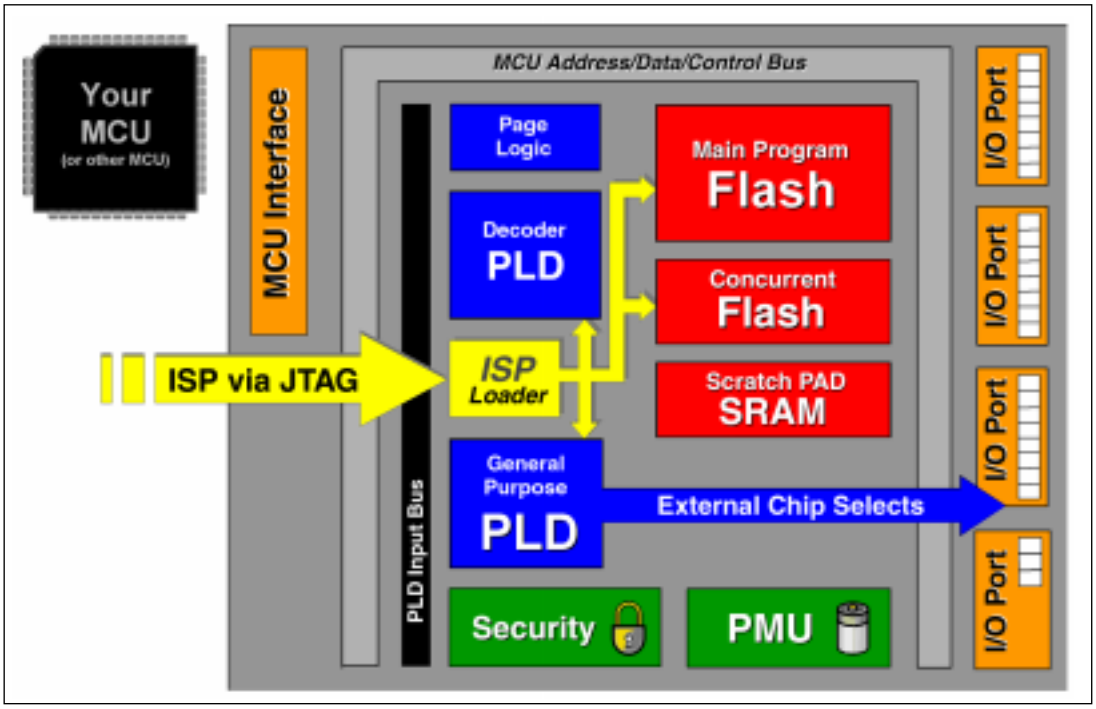
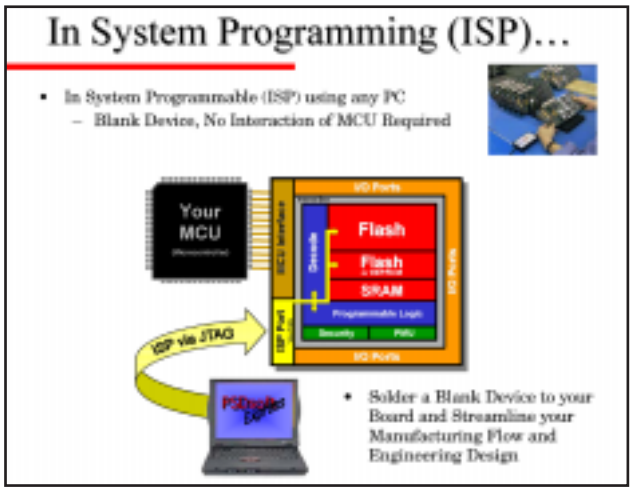
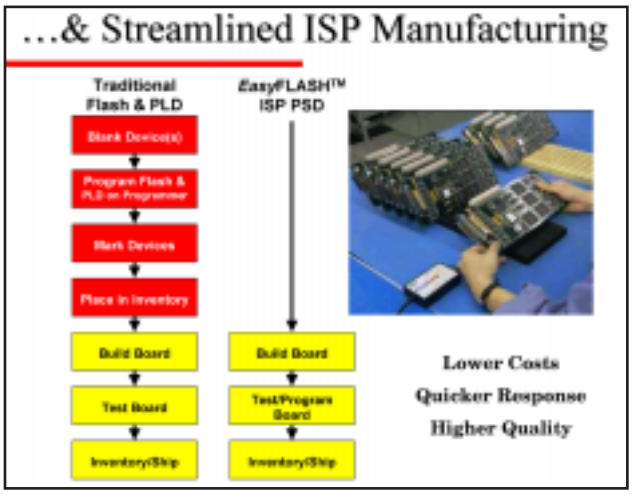


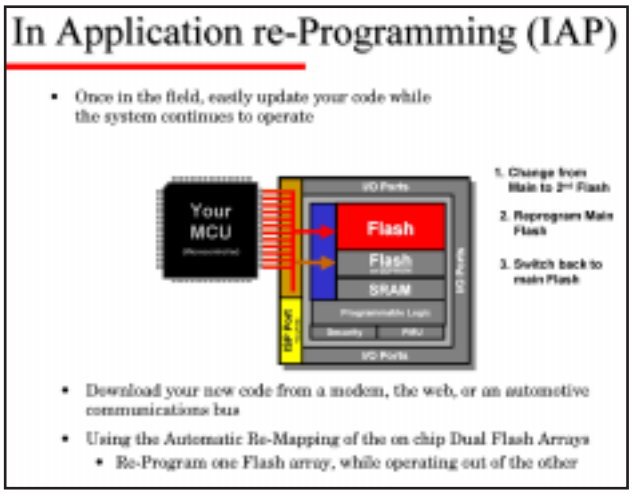
Figure 1. Block Diagram – PSD9XXF2 Programmable MCU Peripheral

1.0 Introduction (Cont.)

The PSD9XX family offers two methods to program PSD Flash memory while the PSD is soldered to a circuit board.







In-System Programming (ISP) via JTAG

An IEEE 1149.1 compliant JTAG interface is included on the PSD enabling the entire device (both flash memories, the PLD, and all configuration) to be programmed while soldered to the circuit board in a matter of seconds. This requires no MCU participation, which means the PSD can be programmed anytime, even when completely blank.

The innovative JTAG interface to flash memories is an industry first, solving key problems faced by designers and manufacturing houses, such as:

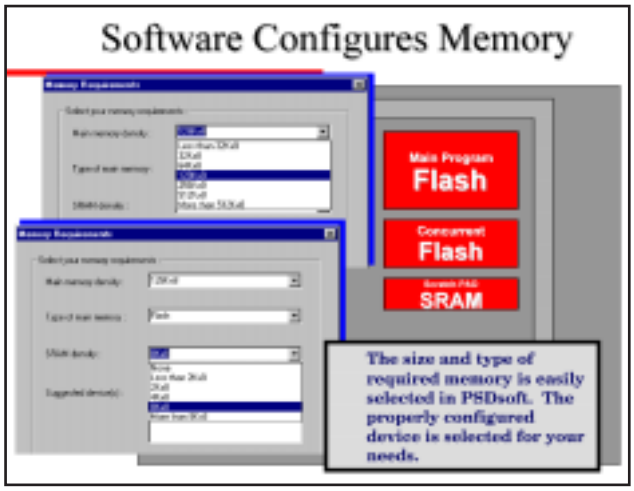
- **First time programming –** How do I get firmware into the flash the very first time? JTAG is the answer, program the PSD while blank with no MCU involvement.
- **Inventory build-up of pre-programmed devices –** How do I maintain an accurate count of pre-programmed flash memory and PLD devices based on customer demand? How many and what version? JTAG is the answer, build your hardware with blank PSDs soldered directly to the board and then custom program just before they are shipped to customer. No more labels on chips and no more wasted inventory.
- **Expensive sockets –** How do I eliminate the need for expensive and unreliable sockets? JTAG is the answer. Solder the PSD directly to the circuit board. Program first time and subsequent times with JTAG. No need to handle devices and bend the fragile leads.

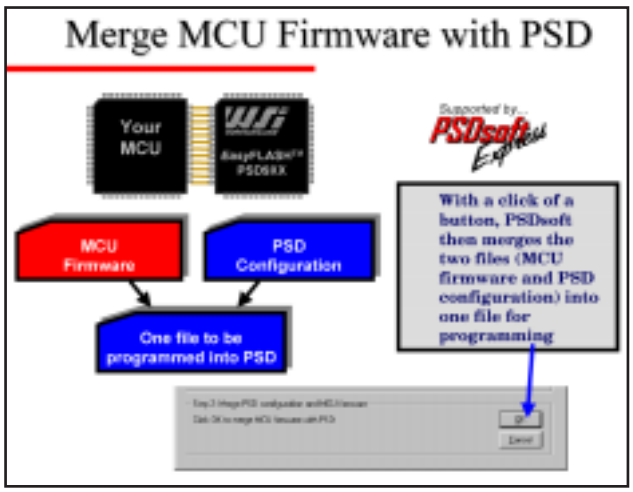
In-Application re-Programming (IAP)

Two independent flash memory arrays are included so the MCU can execute code from one memory while erasing and programming the other. Robust product firmware updates in the field are possible over any communication channel (CAN, Ethernet, UART, J1850, etc) using this unique architecture. Designers are relieved of these problems:

- **Simultaneous read and write to flash memory –** How can the MCU program the same memory from which it is executing code? It cannot. The PSD allows the MCU to operate the two flash memories concurrently, reading code from one while erasing and programming the other during IAP.
- **Complex memory mapping –** I have only a 64K-byte address space to start with.How can I map these two memories efficiently? A Programmable Decode PLD is the answer. The concurrent PSD memories can be mapped anywhere in MCU address space, segment by segment with extremely high address resolution. As an option, the secondary flash memory can be swapped out of the system memory map when IAP is complete. A built-in page register breaks the 64K-byte address limit.
- **Separate program and data space –** How can I write to flash memory while it resides in “program” space during field firmware updates, my MCU won’t allow it! The flash PSD provides means to “reclassify” flash memory as “data” space during IAP, then back to “program” space when complete.

1.0 Introduction (Cont.)





PSDsoft Express – Waferscale's software development tool – guides you through the design process step-by-step making it possible to complete an embedded MCU design capable of ISP/IAP in just hours. Select your MCU and PSDsoft Express will take you through the remainder of the design with point and click entry, covering...PSD selection, pin definitions, programmable logic inputs and outputs, MCU memory map definition, ANSI C code generation for your MCU, and merging your MCU firmware with the PSD design. When complete, two different device programmers are supported directly from PSDsoft – FlashLINK (JTAG) and PSDpro.

The PSD9XX is available in 52-pin PLCC and PQFP packages.

2.0 Key Features

- A simple interface to 8-bit microcontrollers that use either multiplexed or non-multiplexed busses. The bus interface logic uses the control signals generated by the microcontroller automatically when the address is decoded and a read or write is performed. A partial list of the MCU families supported include:
  - Intel 8031, 80196, 80186, 80C251
  - Motorola 68HC11, 68HC16, 68HC12, and 683XX
  - Philips 8031 and 8051XA
  - Zilog Z80, Z8, and Z180
  - Infineon C500
  - Dallas 80C320
- Internal 1 or 2 Mbit flash memory. This is the main Flash memory. It is divided into eight equal-sized blocks that can be accessed with user-specified addresses.
- Internal secondary 256 Kbit Flash memory. It is divided into four equal-sized blocks that can be accessed with user-specified addresses. This secondary memory brings the ability to execute code and update the main Flash **concurrently.**
- 16 or 64 Kbit SRAM. The SRAM's contents can be protected from a power failure by connecting an external battery.
- General Purpose PLD (GPLD) with 19 outputs. The GPLD may be used to implement external chip selects or combinatorial logic function.
- Decode PLD (DPLD) that decodes address for selection of internal memory blocks.
- 27 individually configurable I/O port pins that can be used for the following functions:
  - MCU I/Os
  - PLD I/Os
  - Latched MCU address output
  - Special function I/Os.
  - 16 of the I/O ports may be configured as open-drain outputs.

2.0 Key Features (cont.)

- ❑ Standby current as low as 50 µA for 5 V devices.
- ❑ Built-in JTAG compliant serial port allows full-chip In-System Programmability (ISP). With it, you can program a blank device or reprogram a device in the factory or the field.
- ❑ Internal page register that can be used to expand the microcontroller address space by a factor of 256.
- ❑ Internal programmable Power Management Unit (PMU). The PMU can automatically detect a lack of microcontroller activity and put the PSD9XX into Power Down Mode.
- ❑ Erase/Write cycles:
  - Flash memory – 100,000 minimum
  - PLD – 1,000 minimum

3.0 PSD9XX Family

There are 2 variants in the PSD9XX family. All PSD9XX devices provide these base features: 1 or 2 Mbit main Flash Memory, JTAG port, GPLD, DPLD, power management, and 27 I/O pins. The following table summarizes all the devices in the PSD9XX family. Additional devices will be introduced.

Table 1. PSD9XX Product Matrix

Part #		I/O Pins	No. of GPLD Output	Serial ISP JTAG/ISC Port	Flash Main Memory Kbit (8 Sectors)	Secondary Flash Memory Kbit (4 Sectors)	SRAM Kbit	Turbo Mode	Supply Voltage
PSD9XX Family	Device								
PSD9XX	PSD913F2	27	19	Yes	1024	256	16	Yes	5V
	PSD934F2	27	19	Yes	2048	256	64	Yes	5V

4.0 Package Information

Figure 1. Drawing J7 – 52-Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)

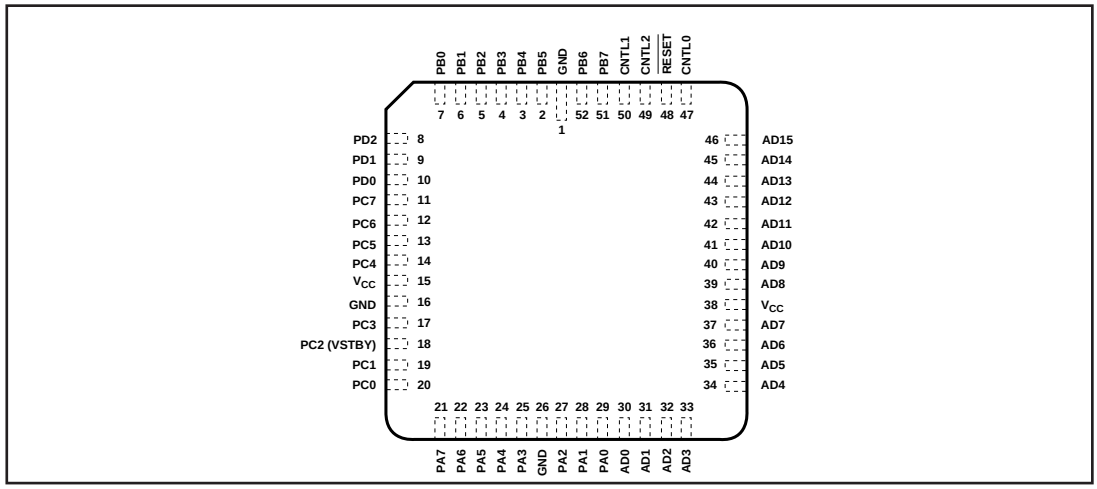
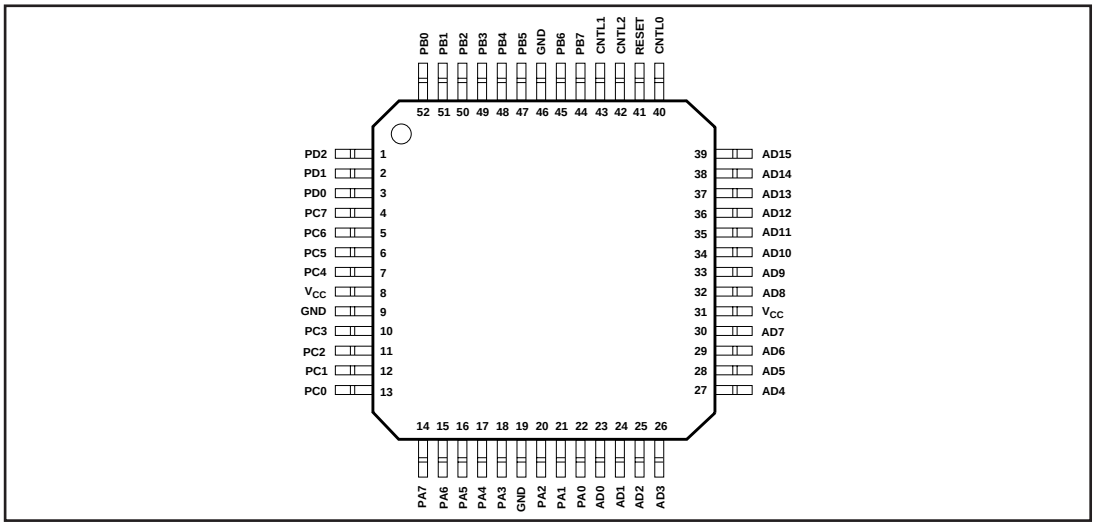


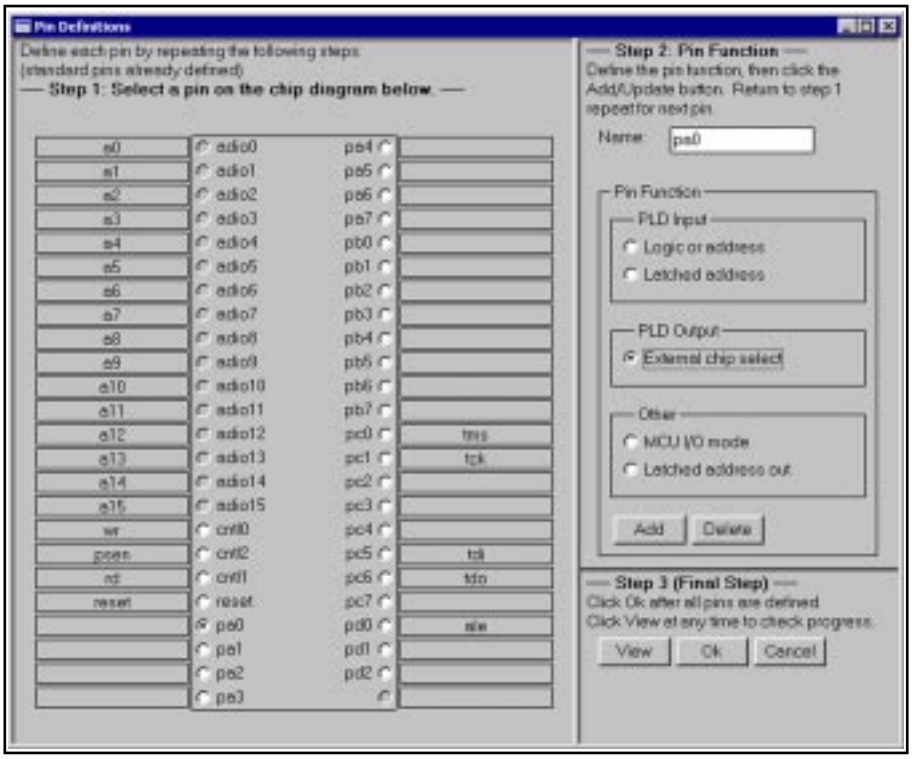
Figure 2. Drawing M3 – 52-Pin Plastic Quad Flatpack (PQFP) (Package Type M)



5.0 Table 2. PSD9XX Pin Descriptions

The following table describes the pin names and pin functions of the PSD9XX. Pins that have multiple names and/or functions are defined using PSDsoft's new Point and Click environment.

Pin Name	Type	Description
ADIO0-15	I/O	This is the lower Address/Data port. Connect your MCU address or address/data bus.
CNTL0-2	I	Configurable MCU control signals.
$\overline{\text{Reset}}$	I	Active low reset input. Resets I/O Ports and some of the configuration registers. Must be active at power up.
PA0-PA7	I/O	These pins make up Port A. These port pins are configurable and can have the following functions: 1. MCU I/O 2. General Purpose PLD outputs. 3. Inputs to the PLDs. 4. Latched address outputs. 5. As the data bus inputs D[0:7] for non-multiplexed address/data bus MCUs (PA0-PA7 only).
PB0-PB7	I/O	These pins make up Port B. These port pins are configurable and can have the following functions: 1. MCU I/O 2. General Purpose PLD outputs. 3. Inputs to the PLDs. 4. Latched address outputs.
PC0-PC7	I/O	PC0 pin of Port C. This port pin can be configured to have the following functions: 1. MCU I/O 2. Input to the PLDs. 3. JTAG interface signals. 4. Battery backed SRAM connections.
PD0-PD2	I/O	PD0 pin of Port D. This port pin can be configured to have the following functions: 1. ALE/AS input latches address output from the MCU (PD0 only). 2. MCU I/O — write or read from a standard output or input port. 3. Input to the PLDs. 4. General Purpose PLD output. 5. CLKIN — clock input to the automatic power-down unit's power-down counter, and the PLD AND array (PD1 only). 6. $\overline{\text{CSI}}$ — chip select input. When low, the MCU can access the PSD memory and I/O. When high, the PSD memory blocks are disabled to conserve power (PD2 only).
V_{CC}		Power pins
GND		Ground pins



PSDsoft Express Pin Definition

6.0 Architectural Overview

PSD9XX devices contain several major functional blocks. Figures 4 and 5 show the architecture of the PSD9XX device family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions and are user configurable.

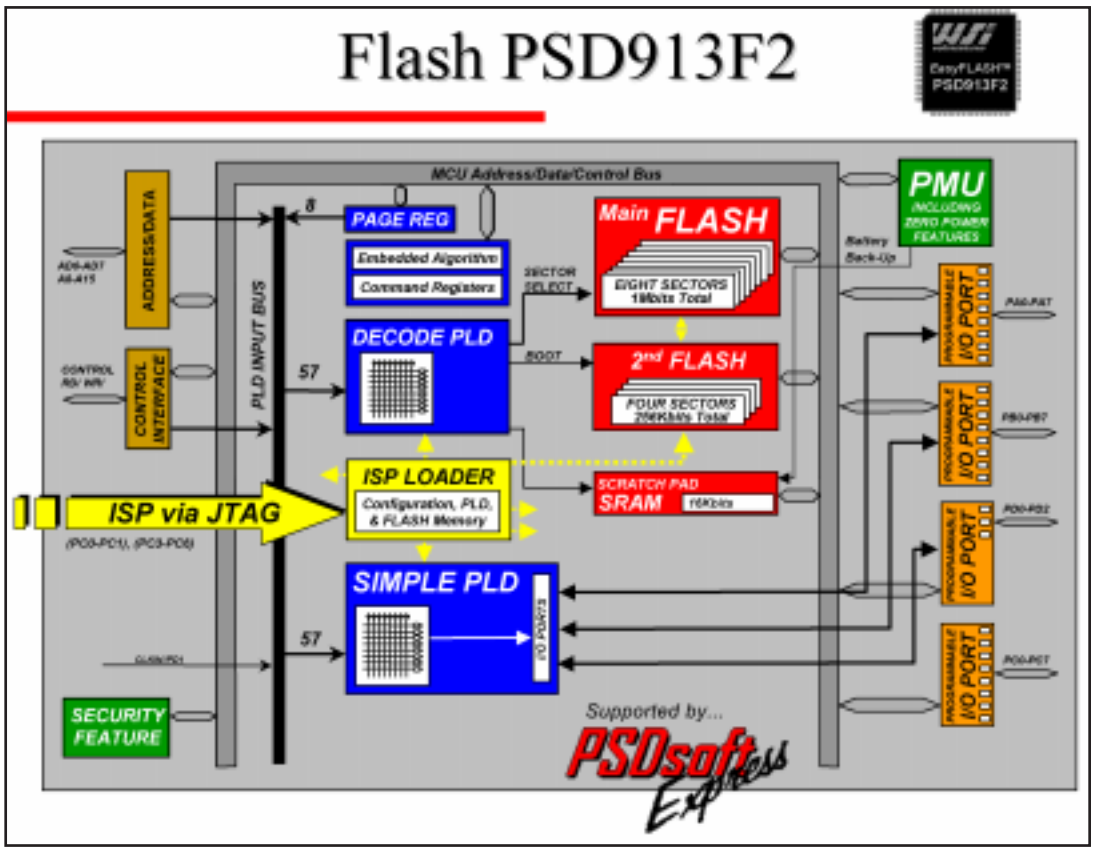


Figure 4

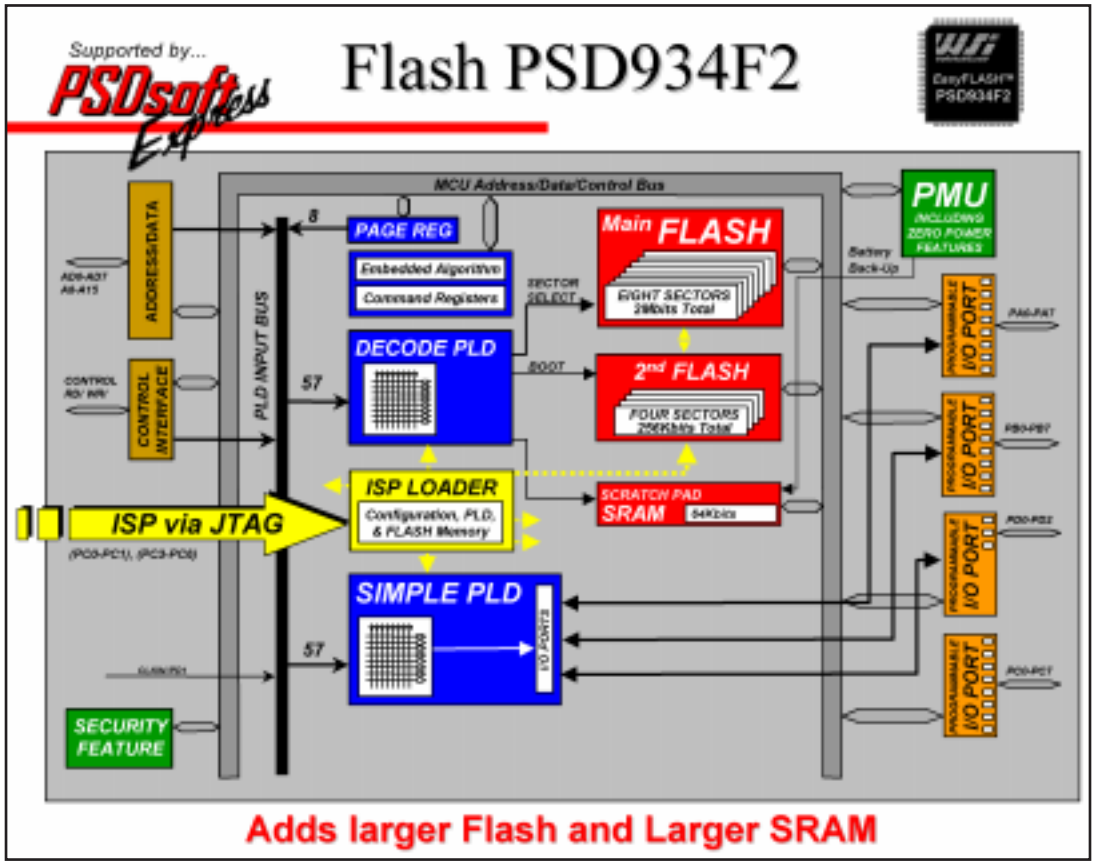


Figure 5

6.0 Architectural Overview

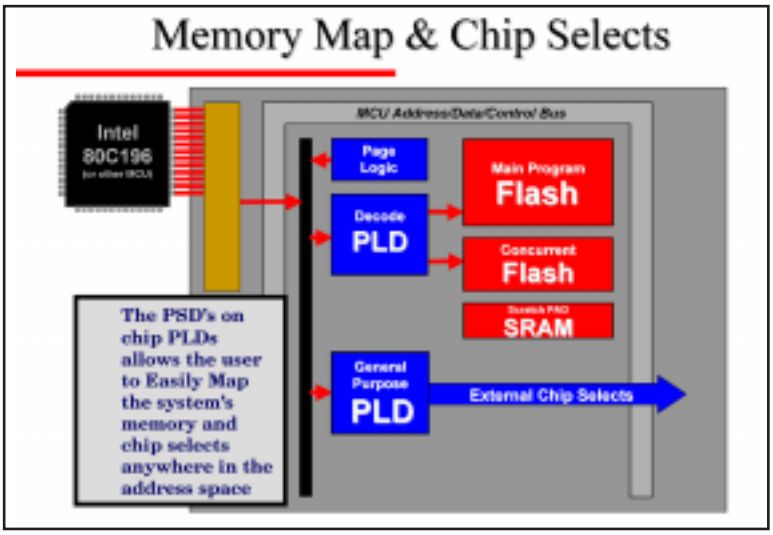
6.1 Memory

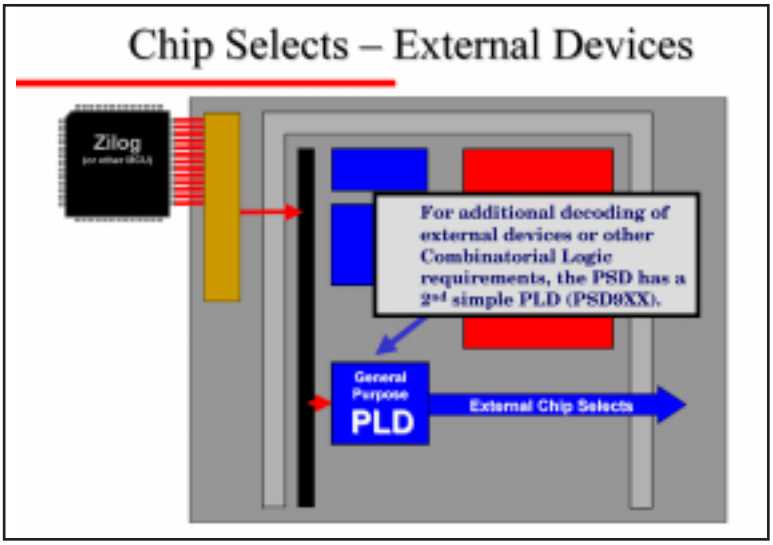
The PSD9XX contains the following memories:

- A 1 or 2 Mbit Flash
- A secondary 256 Kbit Flash memory
- 16 or 64 Kbit SRAM.

Each of the memories is briefly discussed in the following paragraphs. A more detailed discussion can be found in section 9.

The 1 or 2 Mbit Flash is the main memory of the PSD9XX. It is divided into eight equally-sized sectors that are individually selectable.





The 256 Kbit secondary Flash memory is divided into four equally-sized sectors. Each sector is individually selectable. This memory can hold boot code or data, and can be used by the MCU for operation during In-System re-Programming (IAP) of the main Flash.

The 16 or 64 Kbit SRAM is intended for use as a scratchpad memory or as an extension to the microcontroller SRAM. If an external battery is connected to the PSD9XX's Vstby pin, data will be retained in the event of a power failure.

Each block of memory can be located in a unique address space as defined by the user. The access times for all memory types includes the address latching and DPLD decoding time.

6.2 Page Register

The eight-bit Page Register expands the address range of the microcontroller by up to 256 times. The paged address can be used as part of the address space to access external memory and peripherals or internal memory and I/O. The Page Register can also be used to change the address mapping of blocks of Flash memory into different memory spaces IAP.

6.3 PLDs

The device contains two combinatorial PLD blocks, each optimized for a different function, as shown in Table 3. The functional partitioning of the PLDs reduces power consumption, optimizes cost/performance, and eases design entry.

The Decode PLD (DPLD) is used to decode addresses and generate chip selects for the PSD9XX internal memory and registers. The General Purpose PLD (GPLD) can implement user-defined external chip selects and logic functions.

The PLDs consume minimal power by using Zero-Power design techniques. The speed and power consumption of the PLD is controlled by the Turbo Bit in the PMMR0 register and other bits in the PMMR2 registers. These registers are set by the microcontroller at runtime.

6.4 I/O Ports

The PSD9XX has 27 I/O pins divided among four ports (Port A, B, C, and D). Each I/O pin can be individually configured for different functions. Ports A, B, C and D can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for microcontrollers using multiplexed address/data busses.

The JTAG pins can be enabled on Port C for In-System Programming (ISP).

Port A can also be configured as a data port for a non-multiplexed bus.

Table 3. PLD I/O Table

Name	Abbreviation	Inputs	Outputs	Product Terms
Decode PLD	DPLD	57	15	39
General Purpose PLD	GPLD	57	19	114

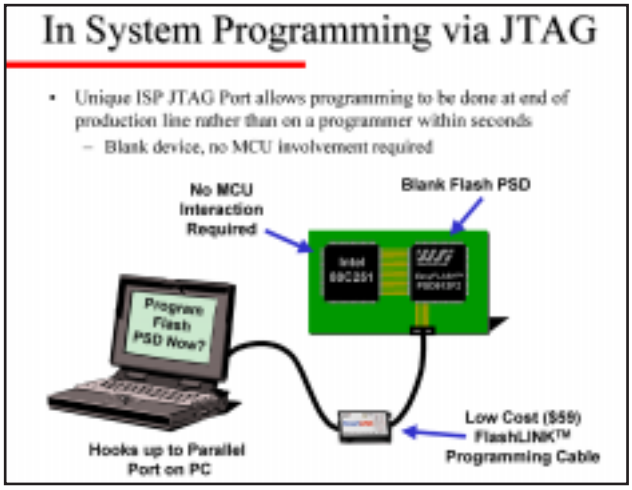
6.0 Architectural Overview (cont.)

6.5 Microcontroller Bus Interface

The PSD9XX easily interfaces with most 8-bit microcontrollers that have either multiplexed or non-multiplexed address/data busses. The device is configured to respond to the microcontroller's control signals, which are also used as inputs to the PLDs. Section 9.3.5 contains microcontroller interface examples.

6.6 In-System Programming (ISP) Port via JTAG

In-System Programming can be performed through the JTAG pins on Port C. This serial interface allows complete programming of the entire PSD9XX device. A blank device can be completely programmed. The JTAG signals (TMS, TCK, TSTAT, TERR, TDI, TDO) are enabled on Port C when selected or when a device is blank.



6.7 In-Application re-Programming (IAP)

The main Flash memory can also be programmed in-system by the microcontroller executing the programming algorithms out of the Secondary Flash memory, or SRAM (IAP). The Secondary Flash memory can be programmed the same way by executing out of the main Flash memory. This includes all the memory blocks, the PLD, MCU interface and all other configuration. Table 4 indicates which programming methods can program different functional blocks of the PSD9XX.

Table 4. Methods of Programming Different Functional Blocks of the PSD9XX

Functional Block	JTAG-ISP	Device Programmer	IAP
Main Flash Memory	Yes	Yes	Yes
Secondary Flash Memory	Yes	Yes	Yes
PLD Array (DPLD and GPLD)	Yes	Yes	No
PSD Configuration	Yes	Yes	No

7.0 Power Management

The PSD9XX offers configurable power saving options. These options may be used individually or in combinations, as follows:

- ❑ All memory types in a PSD (Flash, Secondary Flash Block, and SRAM) are built with Zero-Power technology. In addition to using special silicon design methodology, Zero-Power technology puts the memories into standby mode when address/data inputs are not changing (zero DC current). As soon as a transition occurs on an input, the affected memory "wakes up", changes and latches its outputs, then goes back to standby. The designer does **not** have to do anything special to achieve memory standby mode when no inputs are changing—it happens automatically.

  The PLD sections can also achieve standby mode when its inputs are not changing, see PMMR registers below.

- ❑ The Automatic Power Down (APD) logic allows the PSD to reduce to standby current automatically and keeps it in standby with no chance of noise or miscellaneous signals waking it up. The APD will block MCU address/data signals from reaching the memories and PLDs. This feature is available on all PSD9XX devices.

  Built in logic will monitor the address strobe of the MCU for activity. If there is no activity for a certain time period (MCU is asleep), the APD logic initiates Power Down Mode (if enabled). Once in Power Down Mode, all address/data signals are blocked from reaching PSD memories and PLDs, and the memories are deselected internally. This allows the memories and PLDs to remain in standby mode even if the address/data lines are changing state externally (noise, other devices on the MCU bus, etc.).

- ❑ The PSD Chip Select Input (CSI) on all families can be used to disable the internal memories, placing them in standby mode even if inputs are changing. This feature does not block any internal signals or disable the PLDs. This is a good alternative to using the APD logic, especially if your MCU has a chip select output. There is a slight penalty in memory access time when the CSI signal makes its initial transition from deselected to selected.

- ❑ The PMMR registers can be written by the MCU at run-time to manage power. All PSD devices support "blocking bits" in these registers that are set to block designated signals from reaching both PLDs. Current consumption of the PLDs is directly related to the composite frequency of the changes on their inputs Significant power savings can be achieved by blocking signals that are not used in PLD equations.

- ❑ The PSD9XX devices have a Turbo Bit in the PMMR0 register. This bit can be set to disable the Turbo Mode feature (default is Turbo Mode on). While Turbo Mode is disabled, the PLDs can achieve standby current when no PLD inputs are changing (zero DC current). Even when inputs do change, significant power can be saved at lower frequencies (AC current), compared to when Turbo Mode is enabled.

8.0 Development Tools

Development and Programming Software

The PSD9XX family is supported by the new PSDsoft Express, a Windows-based (95, 98, NT) software development tool. A PSD is quickly configured in a point and click environment. The designer does not need to enter Hardware Definition Language (HDL) equations to define PSD pin functions and memory map information. The general design flow is shown in Figure 6. PSDsoft Express is available free from our web site (www.waferscale.com) or the Waferscale Literature CD.

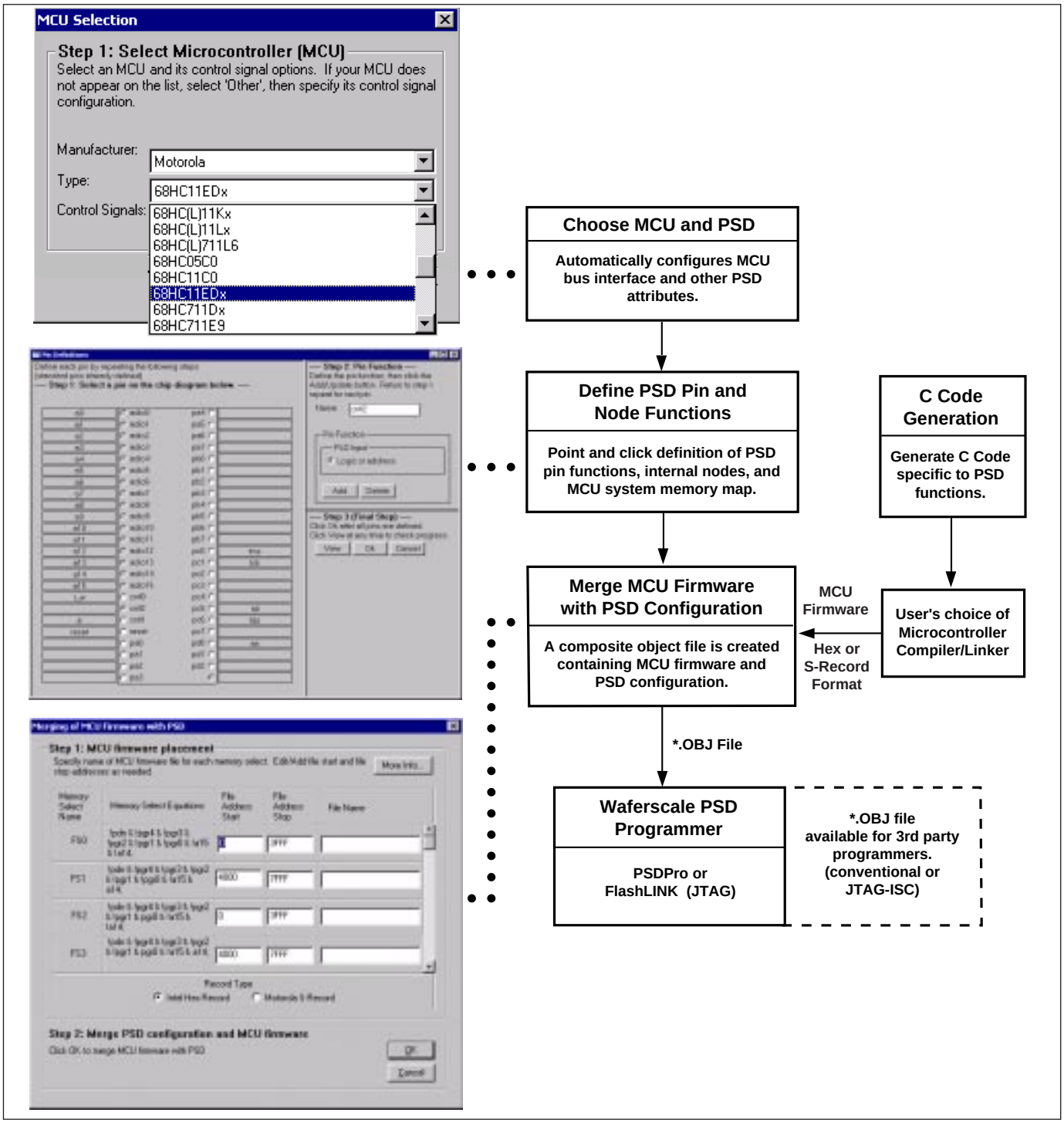
PSDsoft Express directly supports two low cost device programmers from Waferscale, PSDpro and FlashLINK (JTAG). Both of these programmers may be purchased through your local rep/distributor, or directly from our web site using a credit card. The PSD9XX is also supported by third party device programmers, see web site for current list.

Development Kit

DK900

- Supports New Flash PSD9XX
- FlashLINK™ Programmer
- Example ISP and IAP Templates
- Target Board for Programming using ISP via JTAG port
- PSDsoft Express for Free on Web
- $99 U.S. and can be ordered at www.waferscale.com or through any franchised distributor or sales representative

Figure 6. PSDsoft Express Design Flow



9.0 PSD9XX Register Description and Address Offset

Table 5 shows the offset addresses to the PSD9XX registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal PSD9XX registers. Table 5 provides brief descriptions of the registers in CSIOP space. For a more detailed description, refer to section 9.

Table 5. Register Address Offset

Register Name	Port A	Port B	Port C	Port D	Other*	Description
Data In	00	01	10	11		Reads Port pin as input, MCU I/O input mode
Control	02	03				Selects mode between MCU I/O or Address Out
Data Out	04	05	12	13		Stores data for output to Port pins, MCU I/O output mode
Direction	06	07	14	15		Configures Port pin as input or output
Drive Select	08	09	16	17		Configures Port pins as either CMOS or Open Drain on some pins, while selecting high slew rate on other pins.
Flash Protection					C0	Read only – Flash Sector Protection
Secondary Flash Protection					C2	Read only – PSD Security and Secondary Flash Sector Protection
PMMR0					B0	Power Management Register 0
PMMR2					B4	Power Management Register 2
Page					E0	Page Register
VM					E2	Places PSD memory areas in Program and/or Data space on an individual basis.

*Other registers that are not part of the I/O ports.

10.0 Figure 7. Interfacing the PSD9XX with an 80C31

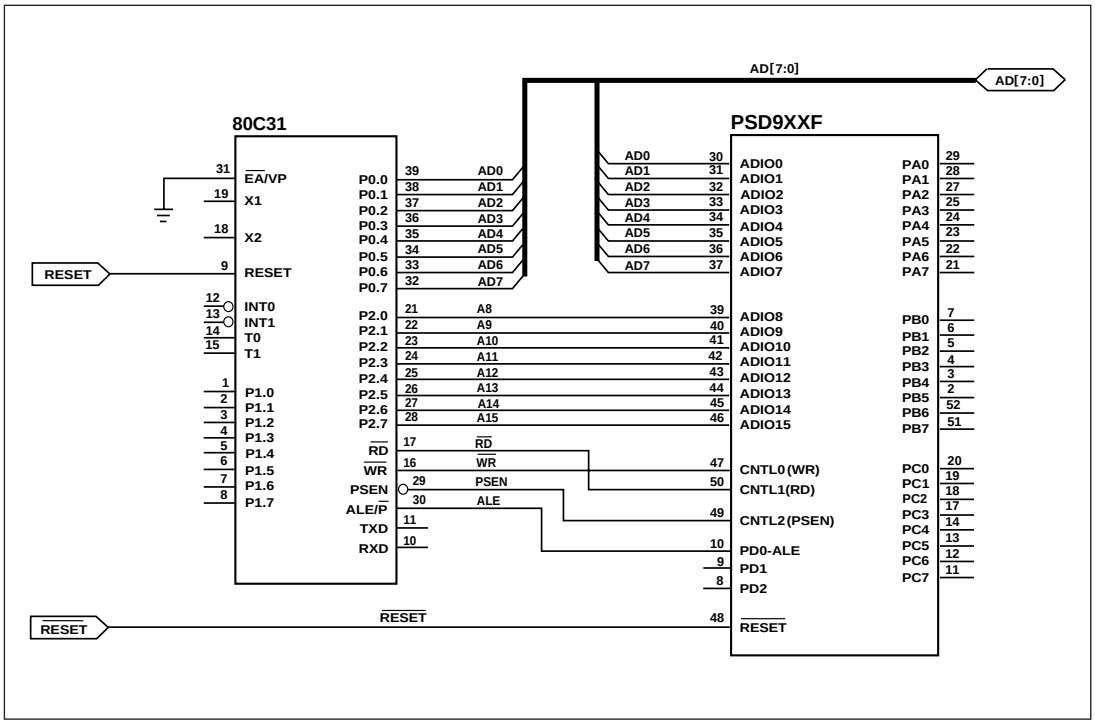
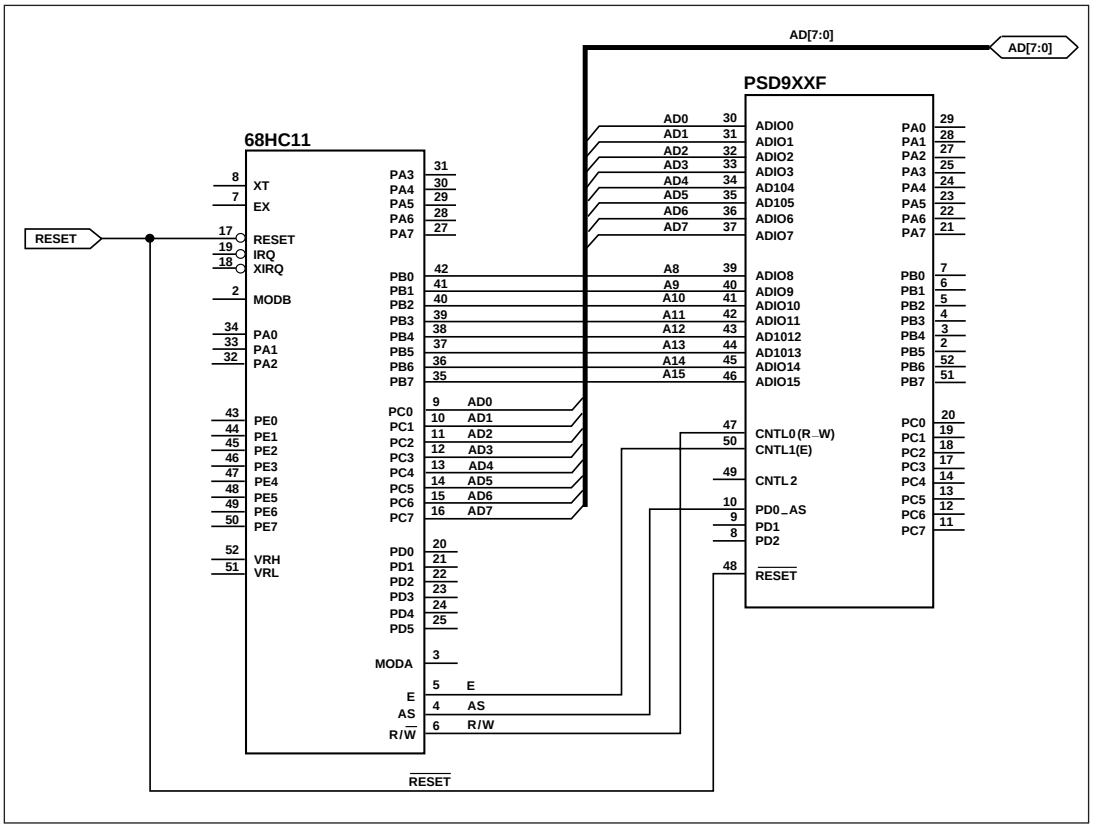


Figure 8. Interfacing the PSD9XX with a 68HC11 (Muxed Address/ Data Bus)



11.0 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
T_{STG}	Storage Temperature		– 65	+ 125	°C
	Operating Temperature	Commercial	0	+ 70	°C
		Industrial	– 40	+ 85	°C
	Voltage on any Pin	With Respect to GND	– 0.6	+ 7	V
V_{PP}	Device Programmer Supply Voltage	With Respect to GND	– 0.6	+ 14	V
V_{CC}	Supply Voltage	With Respect to GND	– 0.6	+ 7	V
	ESD Protection		>2000		V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

12.0 Operating Range

Range	Temperature	V_{CC} Tolerance
Commercial	0° C to +70°C	+ 5 V ± 10%
Industrial	–40° C to +85°C	+ 5 V ± 10%

Note: 3 V devices will be introduced at a later date.

13.0 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	All Speeds	4.5	5	5.5	V

Note: 3 V devices will be introduced at a later date.

14.0 AC/DC Parameters

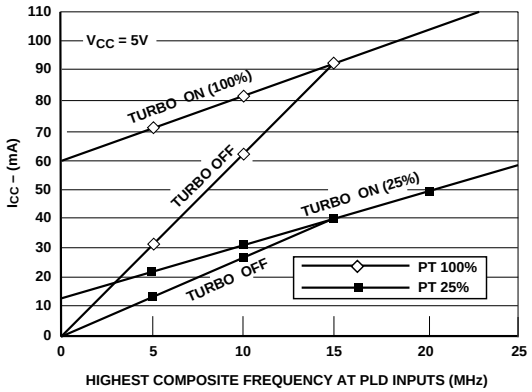
The following tables describe the AD/DC parameters of the PSD9XX family:

- ❑ DC Electrical Specification
- ❑ AC Timing Specification
  - PLD Timing
    - Combinatorial Timing
  - Microcontroller Timing
    - Read Timing
    - Write Timing
    - Power Down and Reset Timing

Following are issues concerning the parameters presented:

- ❑ In the DC specification the supply current is given for different modes of operation. Before calculating the total power consumption, determine the percentage of time that the PSD9XX is in each mode. Also, the supply power is considerably different if the Turbo bit is "OFF".
- ❑ The AC power component gives the PLD, Flash memory, and SRAM mA/MHz specification. Figure 9 shows the PLD mA/MHz as a function of the number of Product Terms (PT) used.
- ❑ In the PLD timing parameters, add the required delay when Turbo bit is "OFF".

Figure 9. PLD I_{CC}/Frequency Consumption (V_{CC} = 5 V ± 10%)



Example of PSD9XX Typical Power Calculation at V_{CC} = 5.0 V

Conditions		
Highest Composite PLD input frequency (Freq PLD)	=	8 MHz
MCU ALE frequency (Freq ALE)	=	4 MHz
% Flash Access	=	80%
% SRAM access	=	15%
% I/O access	=	5% (no additional power above base)
Operational Modes		
% Normal	=	10%
% Power Down Mode	=	90%
Number of product terms used (from fitter report)	=	45 PT
% of total product terms	=	45/153 = 29.4%
Turbo Mode	=	ON

Calculation (typical numbers used)

I_{CC} total = Ipwrdown x %pwrdown + %normal x (I_{CC} (ac) + I_{CC} (dc))

= Ipwrdown x %pwrdown + % normal x (%flash x 2.5 mA/MHz x Freq ALE + %SRAM x 1.5 mA/MHz x Freq ALE + % PLD x 2 mA/MHz x Freq PLD + #PT x 400 µA/PT

= 50 µA x 0.90 + 0.1 x (0.8 x 2.5 mA/MHz x 4 MHz + 0.15 x 1.5 mA/MHz x 4 MHz +2 mA/MHz x 8 MHz + 45 x 0.4 mA/PT)

= 45 µA + 0.1 x (8 + 0.9 + 16 + 18 mA)

= 45 µA + 0.1 x 42.9

= 45 µA + 4.29 mA

= 4.34 mA

This is the operating power with no Flash writes or erases. Calculation is based on I_{OUT} = 0 mA.

AC/DC Parameters (cont.)

Example of Typical Power Calculation at V_{CC} = 5.0 V in Turbo Off Mode

Conditions		
Highest Composite PLD input frequency (Freq PLD)	=	8 MHz
MCU ALE frequency (Freq ALE)	=	4 MHz
% Flash Access	=	80%
% SRAM access	=	15%
% I/O access	=	5% (no additional power above base)
Operational Modes		
% Normal	=	10%
% Power Down Mode	=	90%
Number of product terms used (from fitter report)	=	45 PT
% of total product terms	=	45/153 = 29.4%
Turbo Mode	=	Off

Calculation (typical numbers used)

I_{CC} total = Ipwrdown x %pwrdown + %normal x (I_{CC} (ac) + I_{CC} (dc))

= Ipwrdown x %pwrdown + % normal x (%flash x 2.5 mA/MHz x Freq ALE
+ %SRAM x 1.5 mA/MHz x Freq ALE
+ % PLD x (from graph using Freq PLD))

= 50 µA x 0.90 + 0.1 x (0.8 x 2.5 mA/MHz x 4 MHz + 0.15 x 1.5 mA/MHz x 4 MHz
+ 24 mA)

= 45 µA + 0.1 x (8 + 0.9 + 24)

= 45 µA + 0.1 x 32.9

= 45 µA + 3.29 mA

= 3.34 mA

This is the operating power with no Flash writes or erases. Calculation is based on I_{OUT} = 0 mA.

PSD9XX DC Characteristics (5 V ± 10% Versions)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		All Speeds	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		4.5 V < V_{CC} < 5.5 V	2		V_{CC} +.5	V
V_{IL}	Low Level Input Voltage		4.5 V < V_{CC} < 5.5 V	–.5		0.8	V
V_{IH1}	Reset High Level Input Voltage		(Note 1)	.8 V_{CC}		V_{CC} +.5	V
V_{IL1}	Reset Low Level Input Voltage		(Note 1)	–.5		.2 V_{CC} –.1	V
V_{HYS}	Reset Pin Hysteresis			0.3			V
V_{LKO}	V_{CC} Min for Flash Erase and Program			2.5		4.2	V
V_{OL}	Output Low Voltage		I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
			I_{OL} = 8 mA, V_{CC} = 4.5 V		0.25	0.45	V
V_{OH}	Output High Voltage Except V_{STBY} On		I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
			I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		V
V_{OH1}	Output High Voltage V_{STBY} On		I_{OH1} = 1 µA	V_{SBY} –0.8			V
V_{SBY}	SRAM Standby Voltage			2.0		V_{CC}	V
I_{SBY}	SRAM Standby Current (V_{STBY} Pin)		V_{CC} = 0 V		0.5	1	µA
I_{IDLE}	Idle Current (V_{STBY} Pin)		V_{CC} > V_{SBY}	–0.1		0.1	µA
V_{DF}	SRAM Data Retention Voltage		Only on V_{STBY}	2			V
I_{SB}	Standby Supply Current for Power Down Mode		CSI > V_{CC} –0.3 V (Notes 2 and 3)		50	200	µA
I_{LI}	Input Leakage Current		V_{SS} < V_{IN} < V_{CC}	–1	±.1	1	µA
I_{LO}	Output Leakage Current		0.45 < V_{IN} < V_{CC}	–10	±5	10	µA
I_{CC} (DC) (Note 5)	Operating Supply Current	PLD	PLD_TURBO = OFF, f = 0 MHz (Note 5)		0		mA
			PLD_TURBO = ON, f = 0 MHz		400	700	µA/PT
		Flash	During Flash Write/Erase Only		15	30	mA
			Read Only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC} (AC) (Note 5)	PLD AC Adder				Fig. 9 (Note 4)		
	FLASH AC Adder				2.5	3.5	mA/MHz
	SRAM AC Adder				1.5	3.0	mA/MHz

NOTE: 1. $\overline{\text{Reset}}$ input has hysteresis. V_{IL1} is valid at or below .2V_{CC} –.1. V_{IH1} is valid at or above .8V_{CC}.
2. $\overline{\text{CSI}}$ deselected or internal Power Down mode is active.
3. PLD is in non-turbo mode and none of the inputs are switching
4. Refer to Figure 32 for PLD current calculation.
5. I_{OUT} = 0 mA

Microcontroller Interface – PSD9XX AC/DC Parameters

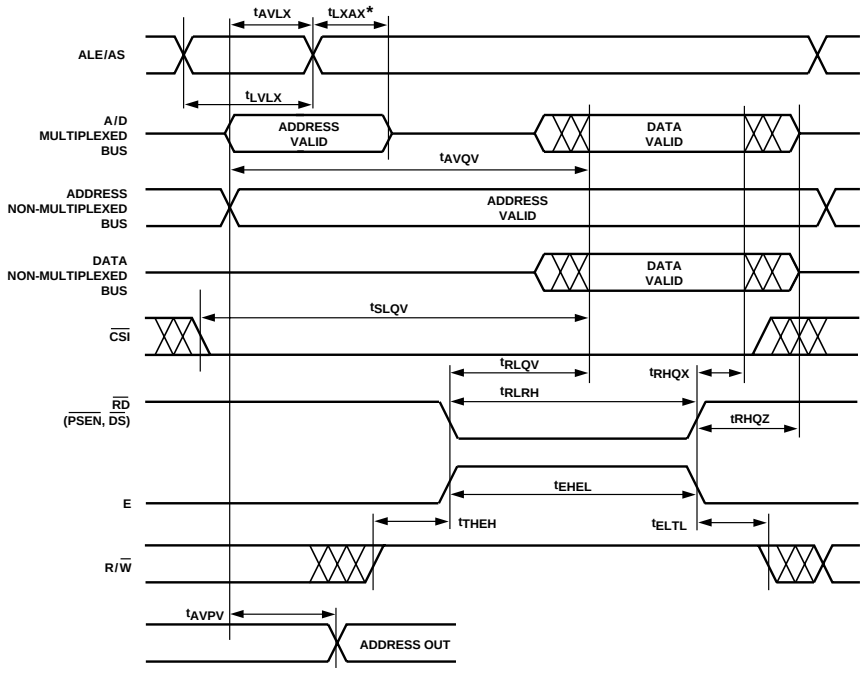
(5V ±10% Versions)

Read Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-90		-15		Turbo Off	Unit
			Min	Max	Min	Max		
t_{LVLX}	ALE or AS Pulse Width		20		28			ns
t_{AVLX}	Address Setup Time	(Note 3)	6		10			ns
t_{LXAX}	Address Hold Time	(Note 3)	8		11			ns
t_{AVQV}	Address Valid to Data Valid	(Note 3)		90		150	Add 10	ns
t_{SLQV}	CS Valid to Data Valid			100		150		ns
t_{RLQV}	$\overline{RD}$ to Data Valid 8-Bit Bus	(Note 5)		32		40		ns
	$\overline{RD}$ or $\overline{PSEN}$ to Data Valid 8-Bit Bus, 8-Bit Bus, 8031, 80251	(Note 2)		38		45		ns
t_{RHQX}	$\overline{RD}$ Data Hold Time	(Note 1)	0		0			ns
t_{RLRH}	$\overline{RD}$ Pulse Width	(Note 1)	32		38			ns
t_{RHQZ}	$\overline{RD}$ to Data High-Z	(Note 1)		25		30		ns
t_{EHEL}	E Pulse Width		32		38			ns
t_{THEH}	R/$\overline{W}$ Setup Time to Enable		10		18			ns
t_{ELTL}	R/$\overline{W}$ Hold Time After Enable		0		0			ns
t_{AVPV}	Address Input Valid to Address Output Delay	(Note 4)		25		32		ns

NOTES: 1. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, and $\overline{PSEN}$ signals.
2. $\overline{RD}$ and $\overline{PSEN}$ have the same timing.
3. Any input used to select an internal PSD9XX function.
4. In multiplexed mode, latched addresses generated from ADIO delay to address output on any Port.
5. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, and $\overline{UDS}$ signals.

Figure 10. Read Timing



*t_{AVLX} and t_{LXAX} are not required for 80C251 in Page Mode or 80C51XA in Burst Mode.

Microcontroller Interface – PSD9XX AC/DC Parameters

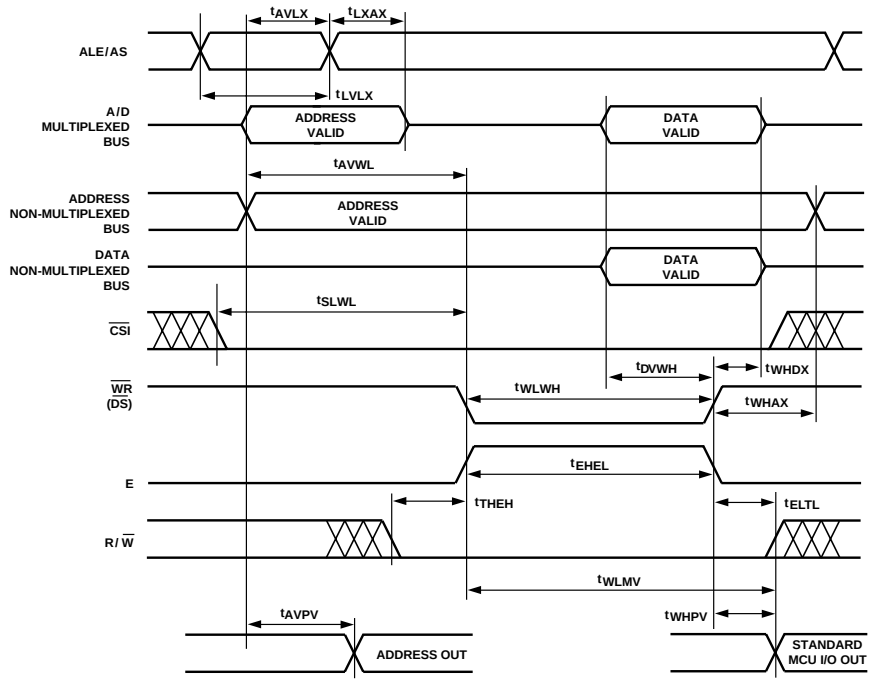
(5V ± 10% Versions)

Write Timing (5 V ± 10% Versions)

Symbol	Parameter	Conditions	-90		-15		Unit
			Min	Max	Min	Max	
t_{LVLX}	ALE or AS Pulse Width		20		28		
t_{AVLX}	Address Setup Time	(Note 1)	6		10		ns
t_{LXAX}	Address Hold Time	(Note 1)	8		11		ns
t_{AVWL}	Address Valid to Leading Edge of $\overline{WR}$	(Notes 1 and 3)	15		20		ns
t_{SLWL}	$\overline{CS}$ Valid to Leading Edge of $\overline{WR}$	(Note 3)	15		20		ns
t_{DVWH}	$\overline{WR}$ Data Setup Time	(Note 3)	35		45		ns
t_{WHDX}	$\overline{WR}$ Data Hold Time	(Note 3)	5		5		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	(Note 3)	35		45		ns
t_{WHAX1}	Trailing Edge of $\overline{WR}$ to Address Invalid	(Note 3)	8		10		ns
t_{WHAX2}	Trailing Edge of $\overline{WR}$ to DPLD Address Input Invalid	(Note 3 and 4)	0		0		ns
t_{WHPV}	Trailing Edge of $\overline{WR}$ to Port Output Valid Using I/O Port Data Register	(Note 3)		30		38	ns
t_{AVPV}	Address Input Valid to Address Output Delay	(Note 2)		25		30	ns

NOTES: 1. Any input used to select an internal PSD9XX function.
2. In multiplexed mode, latched addresses generated from ADIO delay to address output on any Port.
3. $\overline{WR}$ timing has the same timing as E, $\overline{LDS}$, $\overline{UDS}$, $\overline{WRL}$, and $\overline{WRH}$ signals.
4. Address Hold Time for DPLD inputs that are used to generate chip selects for internal PSD memory.

Figure 11. Write Timing



Microcontroller Interface – PSD9XX AC/DC Parameters

(5V ± 10% Versions)

PLD Combinatorial Timing (5 V ± 10%)

Symbol	Parameter	Conditions	-90		-15		TURBO OFF	Slew (Note 1)	Unit
			Min	Max	Min	Max			
t_{PD}	PLD Input Pin/Feedback to PLD Combinatorial Output			25		32	Add 10	Sub 2	ns
t_{ARD}	PLD Array Delay			16		22			ns

NOTE: 1. Fast Slew Rate output available on PA[3:0], PB[3:0], and PD[2:0].

Figure 12. Combinatorial Timing – PLD

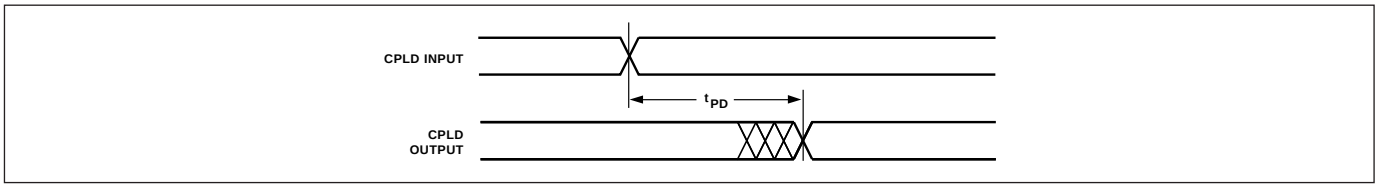
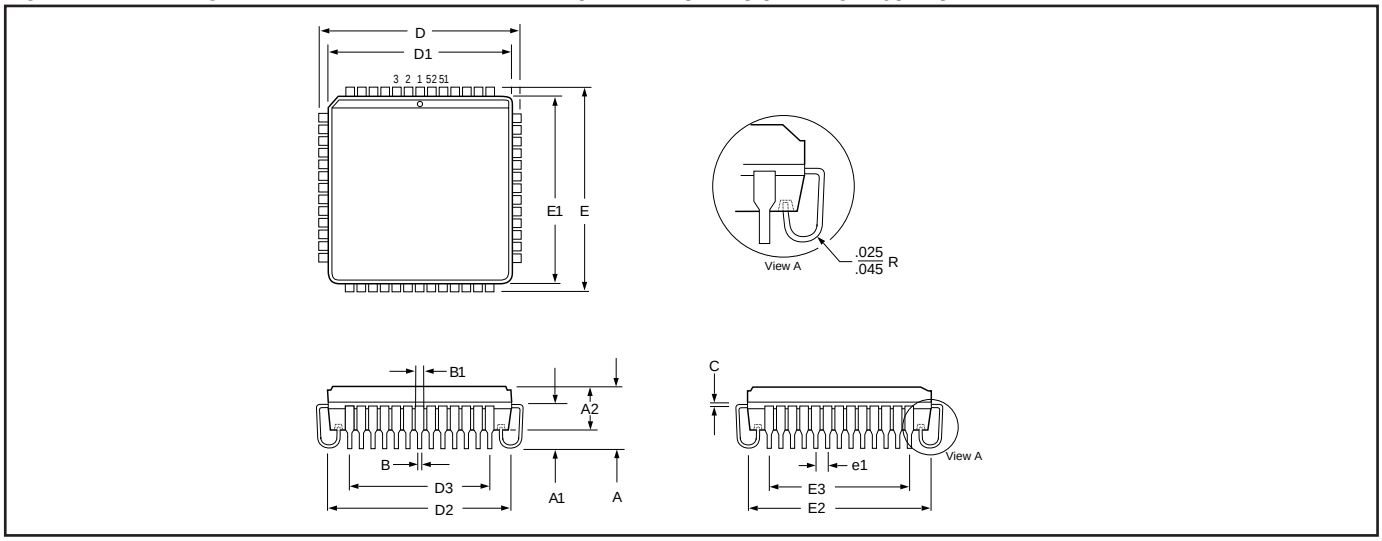


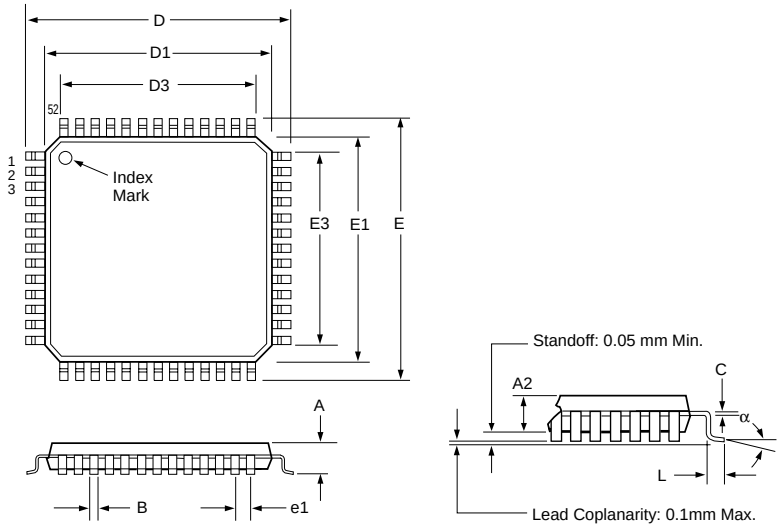
Figure 13. Drawing J7 – 52-Pin Plastic Leaded Chip Carrier (PLCC) (Package Type J)



Family: Plastic Leaded Chip Carrier

	Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes
A	4.19	4.57		0.165	0.180	
A1	2.54	2.79		0.100	0.110	
A2	3.66	3.86		0.144	0.152	
B	0.33	0.53		0.013	0.021	
B1	0.66	0.81		0.026	0.032	
C	0.246	0.261		0.0097	0.0103	
D	19.94	20.19		0.785	0.795	
D1	19.05	19.15		0.750	0.754	
D2	17.53	18.54		0.690	0.730	
D3	15.24		Reference	0.600		Reference
E	19.94	20.19		0.785	0.795	
E1	19.05	19.15		0.750	0.754	
E2	17.53	18.54		0.690	0.730	
E3	15.24		Reference	0.600		Reference
e1	1.27		Reference	0.050		Reference
N	52			52		

Figure 14. Drawing M3 – 52-Pin Plastic Quad Flatpack (PQFP) (Package Type M)



Family: Plastic Quad Flatpack (PQFP)

	Millimeters			Inches		
Symbol	**Min**	**Max**	**Notes**	**Min**	**Max**	**Notes**
α	0°	7°		0°	7°	
A	–	2.35		–	0.093	
A2	1.95	2.10		0.077	0.083	
B	0.22	0.38	Reference	0.009	0.015	
C		0.23			0.009	
D	13.15	13.25		0.518	0.522	
D1	9.95	10.05		0.392	0.396	
D3	7.80		Reference	0.307		Reference
E	13.15	13.25		0.518	0.522	
E1	9.95	10.05		0.392	0.396	
E3	7.80		Reference	0.307		Reference
e1	0.65		Reference	0.026		Reference
L	0.73	1.03		0.029	0.041	
N	52			52		

060198R0

15.0 Selector Guide

Selector Guide – PSD9XX Family

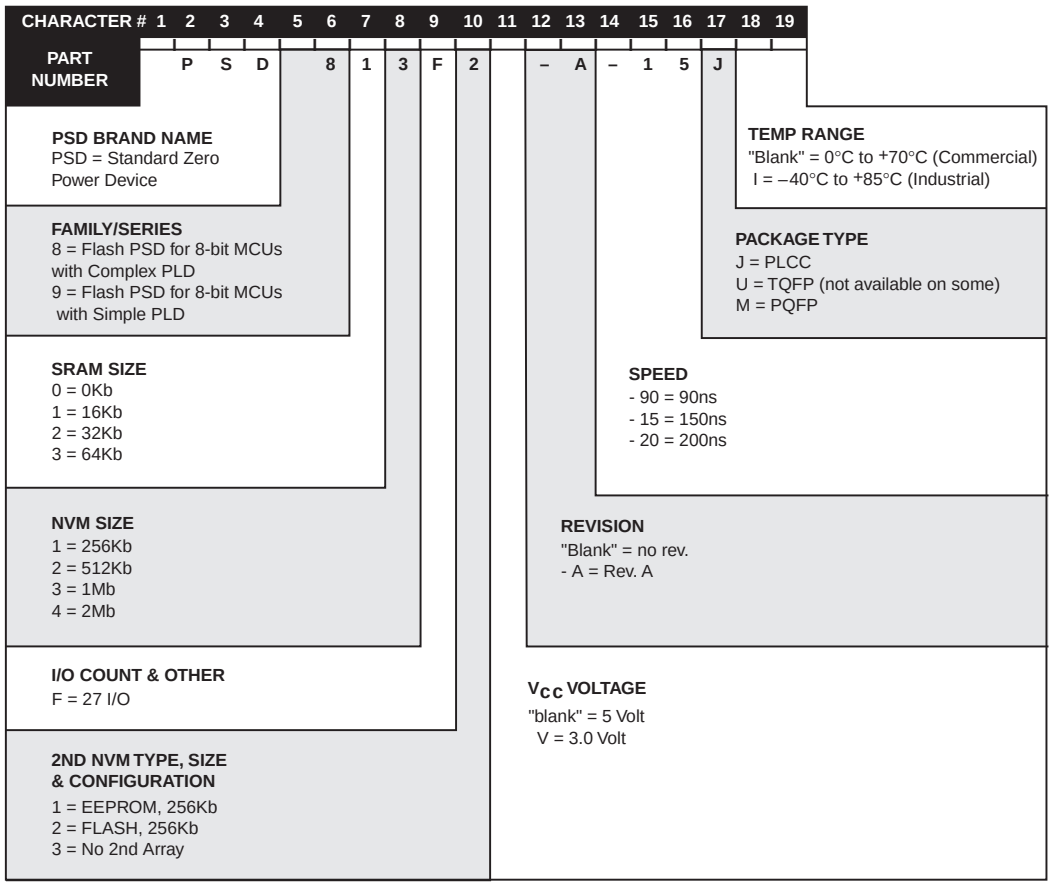
Part #	MCU		PLDs/Decoders			I/O	Memory			Other							
PSD @ 5 V	Data Path	Interface	PLD Inputs	PLD Outputs	Page Reg.	Ports	Flash Program Store	2nd Flash Boot	SRAM	ISP via JTAG	Parallel ISP	ISP Flash	ISP PLDs	Periph. Mode	Security	PMU	APD
PSD913F2	8	PLUS1	57	19	8-Bit	27	1MB	256Kb	16Kb	X	X	X	X		X	X	X
PSD934F2	8	PLUS1	57	19	8-Bit	27	2MB	256Kb	64Kb	X	X	X	X		X	X	X

Legend:

PLUS1 = New Intel 80C251 and Philips 8051XA supported plus all standard MCUs.
APD = Automatic Power Down.

16.0 Part Number Construction

Flash PSD Part Number Construction



17.0 Ordering Information

Part Number	Speed (ns)	Package Type	Operating Temperature Range
PSD913F2-90J	90	52 Pin PLCC	Comm'l
PSD913F2-90M	90	52 Pin PQFP	Comm'l
PSD913F2-90JI	90	52 Pin PLCC	Industrial
PSD913F2-90MI	90	52 Pin PQFP	Industrial
PSD913F2-15J	150	52 Pin PLCC	Comm'l
PSD913F2-15M	150	52 Pin PQFP	Comm'l
PSD934F2-90J	90	52 Pin PLCC	Comm'l
PSD934F2-90M	90	52 Pin PQFP	Comm'l
PSD934F2-90JI	90	52 Pin PLCC	Industrial
PSD934F2-90MI	90	52 Pin PQFP	Industrial
PSD934F2-15J	150	52 Pin PLCC	Comm'l
PSD934F2-15M	150	52 Pin PQFP	Comm'l

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