DATA SHEET

74LVC1G384
Bilateral switch

Preliminary specification
File under Integrated Circuits, IC24

2003 Aug 07

Philips
Semiconductors

PHILIPS

Bilateral switch 74LVC1G384

FEATURES

- Very low ON resistance
  10 Ω (TYP.) at V_{CC} = 2.7 V
  8 Ω (TYP.) at V_{CC} = 3.3 V
  6 Ω (TYP.) at V_{CC} = 5 V
- ESD protection:
  HBM EIA/JESD22-A114-A
  Exceeds 2000 V
  MM EIA/JESD22-A115-A
  Exceeds 200 V
- High noise immunity
- CMOS low power consumption
- Latch up performance
  exceeds 250 mA
- Direct interface TTL-levels
- Multiple package options
- Specified from –40 to +125 °C.

FUNCTION TABLE

See note 1.

INPUT $\overline{E}$	SWITCH
L	ON
H	OFF

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

DESCRIPTION

The 74LVC1G384 is a high-speed Si-gate CMOS device.

The 74LVC1G384 provides an analog switch. The switch has two input/output terminals (Y, Z) and an active LOW enable input ($\overline{E}$). When $\overline{E}$ is HIGH, the analog switch is turned off.

QUICK REFERENCE DATA

Ground = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PZH}/t_{PZL}	turn-on time E to V_{os}	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 3 V	2.5	ns
t_{PHZ}/t_{PLZ}	turn-off time E to V_{os}		3.4	ns
t_{PZH}/t_{PZL}	turn-on time E to V_{os}	C_L = 50 pF; R_L = 500 Ω; V_{CC} = 5 V	1.9	ns
t_{PHZ}/t_{PLZ}	turn-off time E to V_{os}		2.5	ns
C_I	input capacitance		2	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 10 MHz; VCC = 3.3 V; notes 1 and 2	16	pF
C_S	switch capacitance	OFF-state	5	pF
		ON-state	9.5	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L + C_S) \times V_{CC}^2 \times f_o$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   C_S = max. switch capacitance in pF;
   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G384GW	–40 to +125 °C	5	SC-88A	plastic	SOT353	?
74LVC1G384GV	–40 to +125 °C	5	SC-74A	plastic	SOT753	?

PINNING

PIN	SYMBOL	DESCRIPTION
1	Y	independent input/output
2	Z	independent output/input
3	GND	ground (0 V)
4	$\overline{E}$	enable input (active LOW)
5	V_{CC}	DC supply voltage

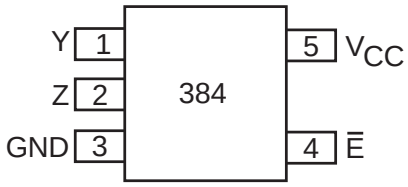


Fig.1 Pin configuration.

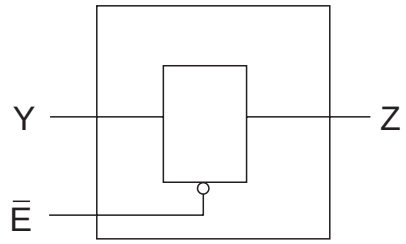


Fig.2 Logic symbol.

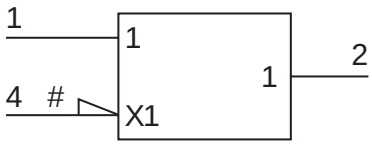


Fig.3 IEC logic symbol.

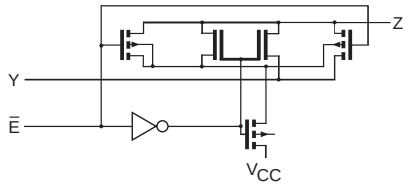


Fig.4 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	active mode	0	V_{CC}	V
		V_{CC} = 0 V; Power-down mode	0	5.5	V
T_{amb}	operating ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0	–	±50	mA
V_O	output voltage	active mode; notes 1 and 2	–0.5	V_{CC} + 0.5	V
		Power-down mode; notes 1 and 2	–0.5	+6.5	V
I_O	output diode current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation per package	for temperature range from –40 to +125 °C	–	250	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)		T_{amb} (°C)		UNIT
		OTHER	V_{CC} (V)	–40 to +85		–40 to +125		
				MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	$0.65 \times V_{CC}$	–	V
			2.3 to 2.7	1.7	–	1.7	–	V
			2.7 to 3.6	2.0	–	2.0	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	$0.7 \times V_{CC}$	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	$0.35 \times V_{CC}$	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	0.7	–	0.7	V
			2.7 to 3.6	–	0.8	–	0.8	V
			4.5 to 5.5	–	$0.3 \times V_{CC}$	–	$0.3 \times V_{CC}$	V

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			T_{amb} (°C)		UNIT
		OTHER	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
I_I	input leakage current (control pin)	V_I = 5.5 V or GND	5.5	–	±0.1	±5	–	100	µA
I_S	analog switch OFF-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC}$ – GND see Fig.6	5.5	–	±0.1	±5	–	200	µA
I_S	analog switch ON-state current	$V_I = V_{IH}$ or V_{IL}; $\|V_S\| = V_{CC}$ – GND; see Fig.7	5.5	–	±0.1	±5	–	200	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; V_S = GND or V_{CC}; I_O = 0 A	5.5	–	0.1	10	–	200	µA
ΔI_{CC}	additional quiescent supply current per control pin	$V_I = V_{CC}$ – 0.6 V; V_S = GND or V_{CC}; I_O = 0 A	5.5	–	5	500	–	5000	µA

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

SYMBOL	PARAMETER	TEST CONDITIONS			T_{amb} (°C)					UNIT
		OTHER	I_S (mA)	V_{CC} (V)	–40 to +85			–40 to +125		
					MIN.	TYP.(1)	MAX.	MIN.	MAX.	
R_{ON}	ON-resistance (peak)	V_S = GND to V_{CC}; $V_I = V_{IH}$; see Fig.5	4	1.65 - 1.95	–	35	100	–	150	Ω
			8	2.3 - 2.7	–	14	30	–	45	Ω
			12	2.7	–	11.5	25	–	38	Ω
			24	3.0 - 3.6	–	8.5	20	–	30	Ω
			32	4.5 - 5.5	–	6.5	15	–	23	Ω
R_{ON}	ON-resistance (rail)	V_S = GND; $V_I = V_{IH}$; see Fig.5	4	1.65 - 1.95	–	10	30	–	45	Ω
			8	2.3 - 2.7	–	8.5	20	–	30	Ω
			12	2.7	–	7.5	18	–	27	Ω
			24	3.0 - 3.6	–	6.5	15	–	23	Ω
			32	4.5 - 5.5	–	6	10	–	15	Ω
R_{ON}	ON-resistance (rail)	$V_S = V_{CC}$; $V_I = V_{IH}$; see Fig.5	4	1.65 - 1.95	–	12	30	–	45	Ω
			8	2.3 - 2.7	–	8.5	20	–	30	Ω
			12	2.7	–	7.5	18	–	27	Ω
			24	3.0 - 3.6	–	6.5	15	–	23	Ω
			32	4.5 - 5.5	–	6	10	–	15	Ω
R_{ON}	ON-resistance (flatness)	V_S = GND to V_{CC}; $V_I = V_{IH}$; see Figs. 9 to 12	4	1.8	–	100(2)	–	–	–	Ω
			8	2.5	–	17(2)	–	–	–	Ω
			12	2.7	–	10(2)	–	–	–	Ω
			24	3.3	–	5(2)	–	–	–	Ω
			32	5.0	–	3(2)	–	–	–	Ω

Note

1. All typical values are measured at T_{amb} = 25 °C.
2. R_{ON} flatness over operating temperature range (–40 to +85 °C).

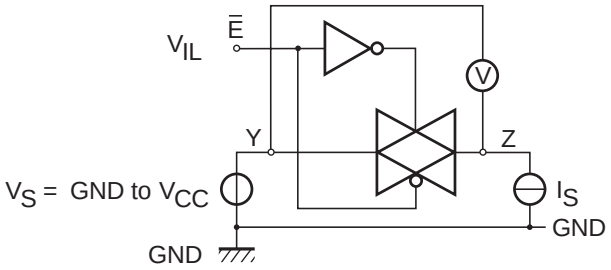


Fig.5 Test circuit for measuring ON-resistance (R_{ON}).

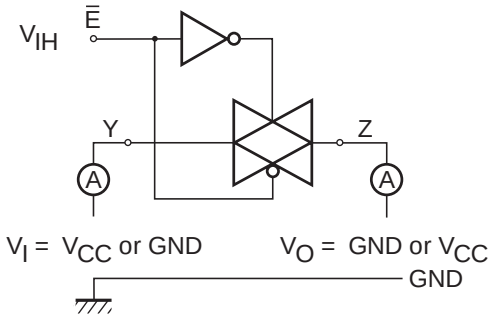


Fig.6 Test circuit for circuit OFF-state current.

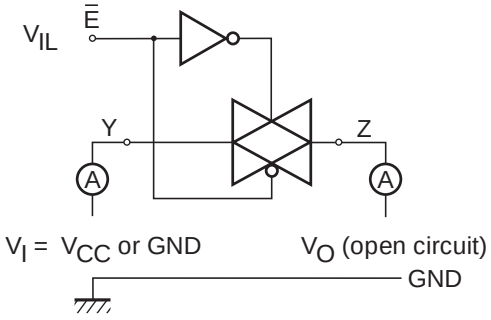


Fig.7 Test circuit for measuring ON-state current.

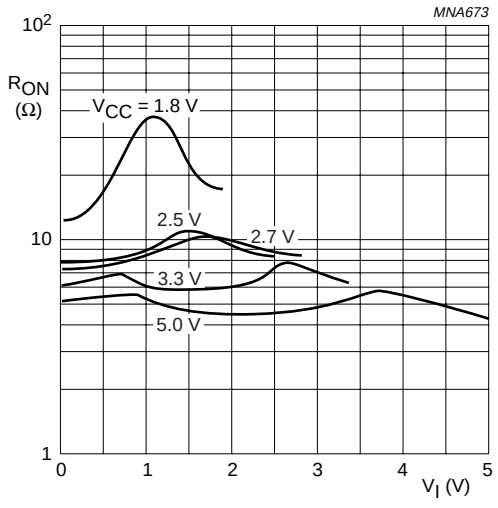


Fig.8 Typical ON-resistance (R_{ON}) as a function of input voltage (V_S) for V_S = GND to V_{CC}.

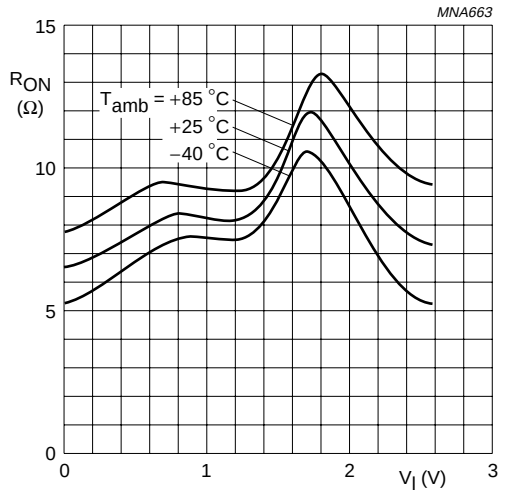


Fig.9 R_{ON} for V_{CC} = 2.5 V.

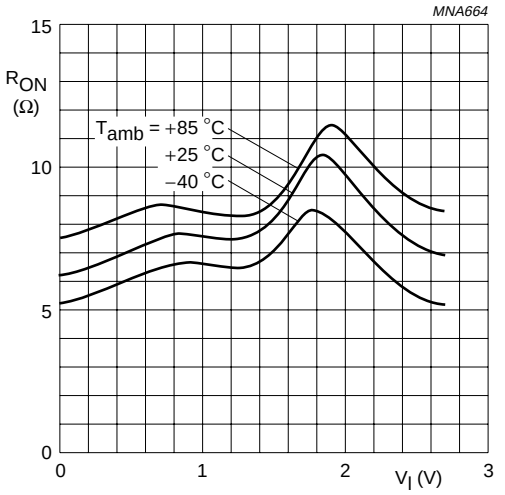


Fig.10 R_{ON} for V_{CC} = 2.7 V.

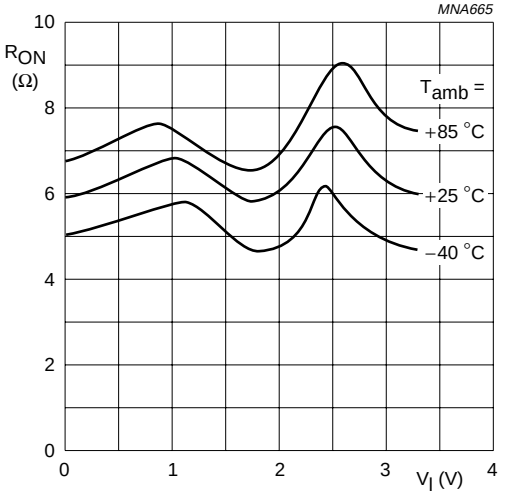


Fig.11 R_{ON} for V_{CC} = 3.3 V.

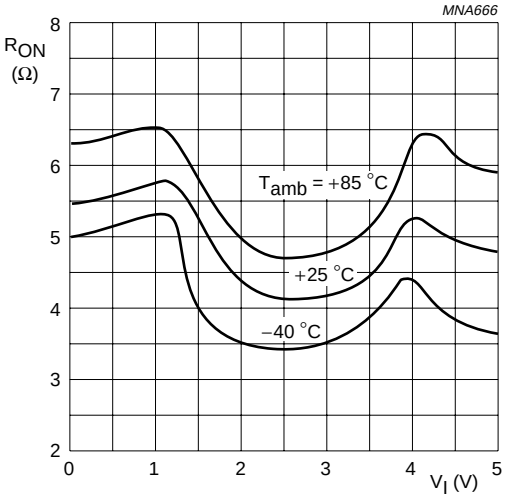


Fig.12 R_{ON} for V_{CC} = 5.0 V.

AC CHARACTERISTICS

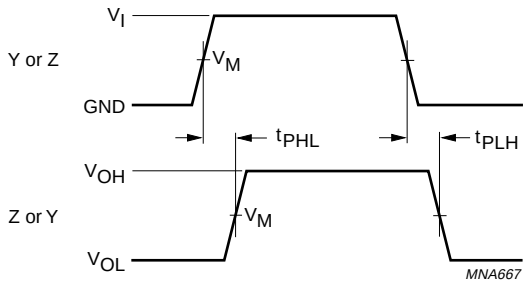
GND = 0 V; $t_r = t_f \leq 2.0$ ns; $C_L = 30$ pF; $R_L = 1$ kΩ; $V_{CC} = 1.65$ to 1.95 V;
GND = 0 V; $t_r = t_f \leq 2.0$ ns; $C_L = 30$ pF; $R_L = 500$ Ω; $V_{CC} = 2.3$ to 2.7 V;
GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500$ Ω; $V_{CC} \geq 2.7$ V.

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)					UNIT
		WAVEFORMS	V_{CC} (V)	−40 to +85			−40 to +125		
				MIN.	TYP.(1)	MAX.	MIN.	MAX.	
t_{PHL}/t_{PLH}	propagation delay inA; inB to outY	see Figs 13 and 15	1.65 to 1.95	–	0.8	2	–	3	ns
			2.3 to 2.7	–	0.4	1.2	–	2	ns
			2.7	–	0.4	1	–	1.5	ns
			3.0 to 3.6	–	0.3	0.8	–	1.5	ns
			4.5 to 5.5	–	0.2	0.6	–	1	ns
t_{PZH}/t_{PZL}	turn-ON time $\overline{E}$ to V_{OS}	see Figs 14 and 15	1.65 to 1.95	1	5.3	12.5	1	15.5	ns
			2.3 to 2.7	1	3.0	6.5	1	8.5	ns
			2.7	1	2.6	6.5	1	8	ns
			3.0 to 3.6	1	2.5	5.5	1	6.5	ns
			4.5 to 5.5	1	1.9	4.0	1	5.5	ns
t_{PHZ}/t_{PLZ}	turn-OFF time $\overline{E}$ to V_{OS}	see Figs 14 and 15	1.65 to 1.95	1	4.2	12.5	1	13	ns
			2.3 to 2.7	1	2.4	6.9	1	9	ns
			2.7	1	3.6	7.5	1	9.5	ns
			3.0 to 3.6	1	3.4	6.5	1	8.5	ns
			4.5 to 5.5	1	2.5	4.5	1	6.5	ns

Note

1. All typical values are measured at $T_{amb} = 25$ °C.

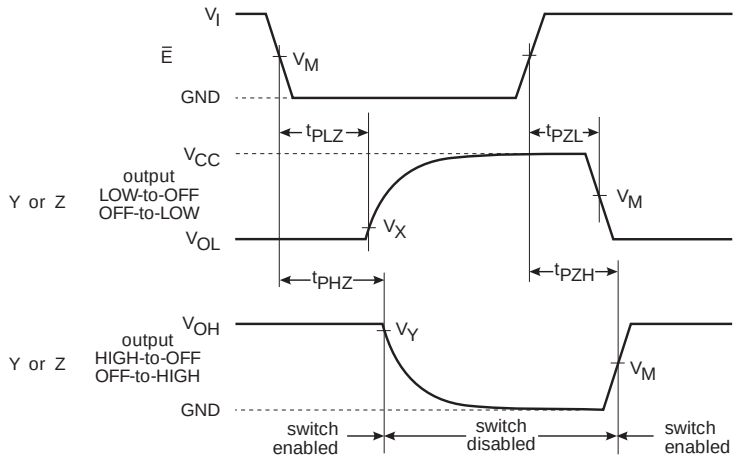
AC WAVEFORMS



V_{CC}	V_M	V_I	INPUT $t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7; 3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.13 The input (V_S) to output (V_O) propagation delays.

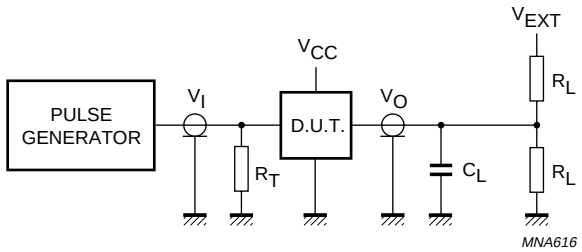


V_{CC}	V_M	V_I	INPUT $t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7; 3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_X = V_{OL} + 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V;
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_Y = V_{OH} - 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.14 The turn-on and turn-off times.



				V_{EXT}		
V_{CC}	**V_I**	**C_L**	**R_L**	**T_{PLH}/T_{PHL}**	**T_{PZH}/T_{PHZ}**	**T_{PZL}/T_{PLZ}**
1.65 to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7; 3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Fig.15 Load circuitry for switching times.

ADDITIONAL AC CHARACTERISTICS FOR THE 74LVC1G66

Recommended conditions and typical values at T_{amb} = 25 °C.

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	TYP.	UNIT
	sine-wave distortion	R_L = 10 kΩ; C_L = 50 pF; f_{in} = 1 kHz see Fig.17	1.65	0.032	%
			2.3	0.008	%
			3	0.006	%
			4.5	0.001	%
		R_L = 10 kΩ; C_L = 50 pF; f_{in} = 10 kHz see Fig.17	1.65	0.068	%
			2.3	0.009	%
			3	0.008	%
			4.5	0.006	%
	switch ON signal frequency response	R_L = 600 Ω; C_L = 50 pF; f_{in} = 1MHz; see Fig. 16; note 1	1.65	135	MHz
			2.3	145	MHz
			3	150	MHz
			4.5	155	MHz
		R_L = 50 Ω; C_L = 5 pF; f_{in} = 1MHz; see Fig. 16; note 1	1.65	>500	MHz
			2.3	>500	MHz
			3	>500	MHz
			4.5	>500	MHz
	switch OFF signal feed-through attenuation	R_L = 600 Ω; C_L = 50 pF; f_{in} = 1MHz; see Fig. 18; note 2	1.65	–46	dB
			2.3	–46	dB
			3	–46	dB
			4.5	–46	dB
		R_L = 0 Ω; C_L = 50 pF; f_{in} = 1MHz; see Fig. 18; note 2	1.65	–37	dB
			2.3	–37	dB
			3	–37	dB
			4.5	–37	dB
	crosstalk (control input to signal output)	R_L = 600 Ω; C_L = 50 pF; f_{in} = 1MHz; $t_r = t_f$ = 2 ns see Fig. 19	1.65	69	mV
			2.3	87	mV
			3	156	mV
			4.5	302	mV
f_{max}	minimum frequency response (–3 dB)	R_L = 50 Ω; C_L = 10 pF; see Fig. 16; note 1	1.65	200	MHz
			2.3	350	MHz
			3	410	MHz
			4.5	440	MHz

SYMBOL	PARAMETER	TEST CONDITIONS	V_{CC} (V)	TYP.	UNIT
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_{in} = 10 MHz	2.5	13.7	pF
			3.3	15.2	pF
			5.0	18.3	pF
Q	charge injection	C_L = 0.1 nF; V_{gen} = 0 V; R_{gen} = 0 Ω; f = 1 Mhz; R_L = 1 MΩ; see Fig.20; note 3	1.65 to 5.5	0.05	pC

Notes

1. Adjust f_{in} voltage to obtain 0 dBm level at output. Increase f_{in} frequency until dB meter reads –3 dB.
2. Adjust f_{in} voltage to obtain 0 dBm level at input.
3. Guaranteed by design.

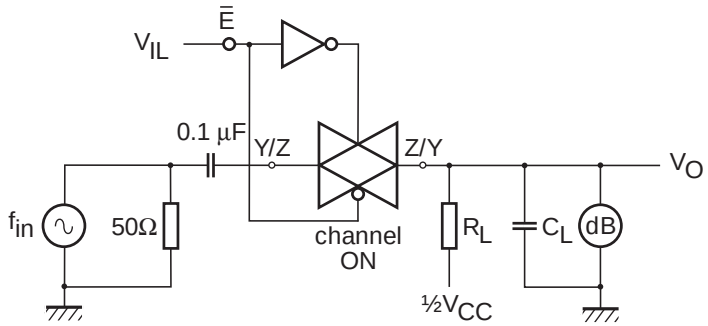
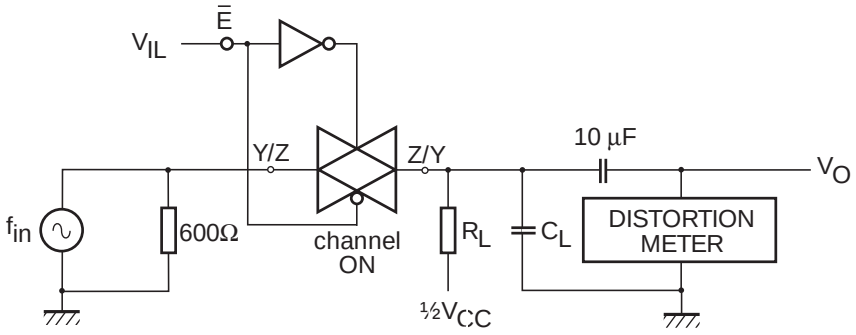


Fig.16 Test circuit for measuring the frequency response when switch is ON.



V_{CC}	V_I
1.65 V	1.4 V_{p-p}
2.3 V	2 V_{p-p}
3 V	2.5 V_{p-p}
4. V	4 V_{p-p}

Fig.17 Test circuit for measuring Sine-Wave distortion.

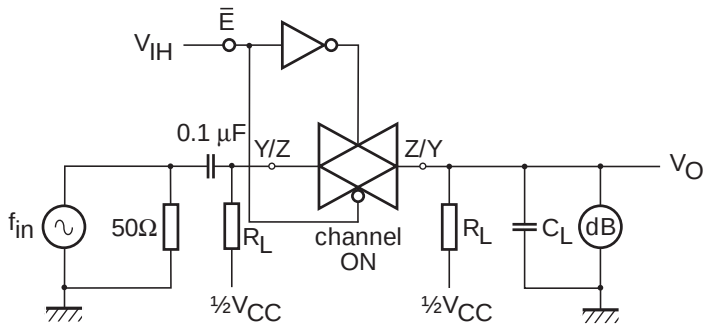


Fig.18 Test circuit for measuring feed-through when switch is OFF.

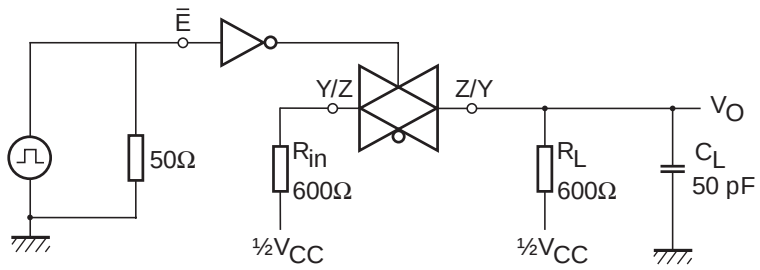


Fig.19 Crosstalk.

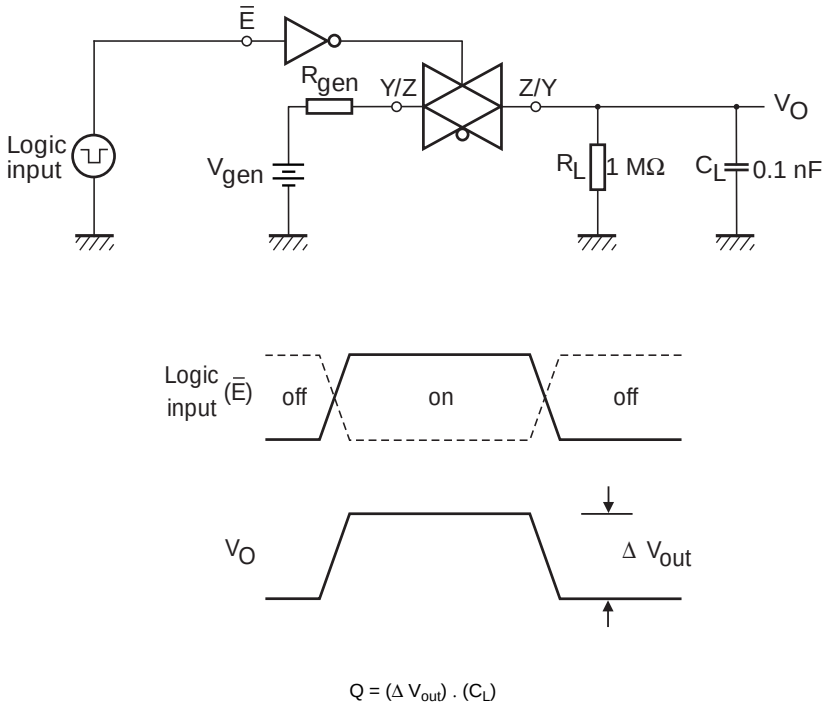
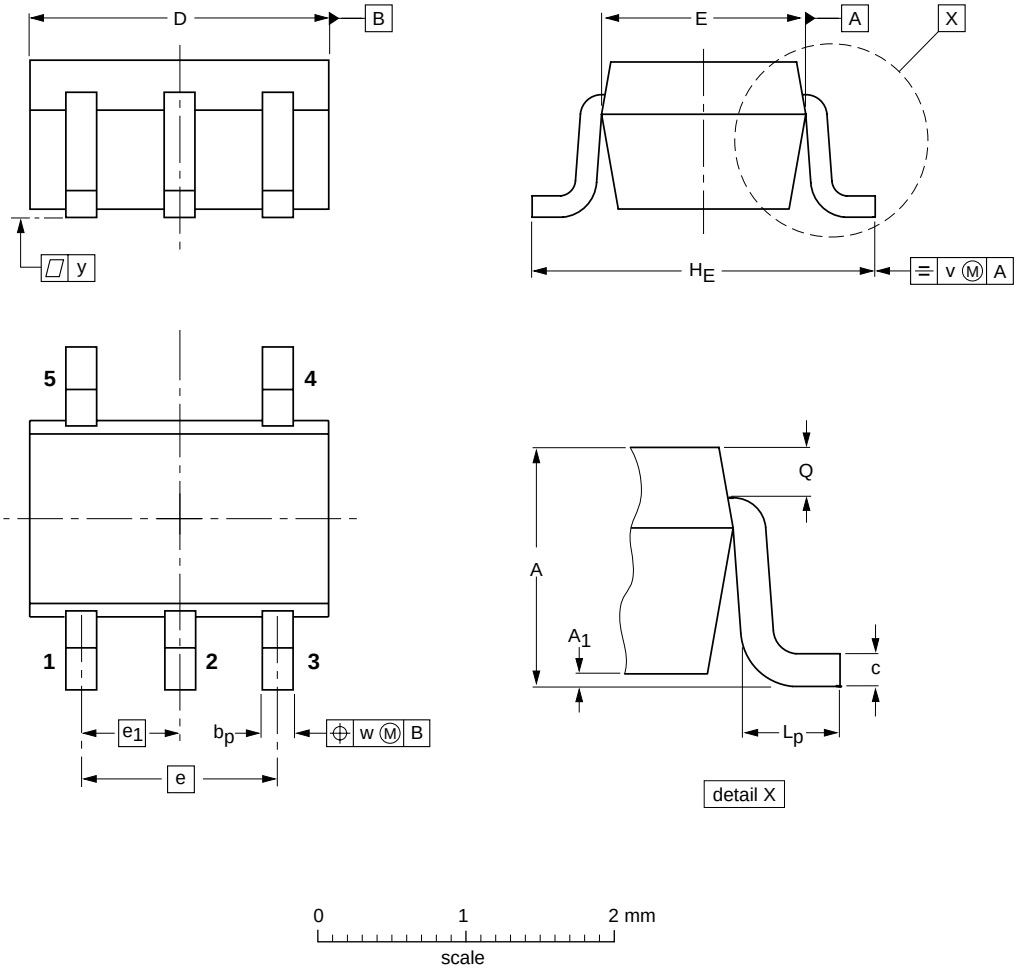


Fig.20 Charge injection test.

PACKAGE OUTLINE

Plastic surface mounted package; 5 leads **SOT353**

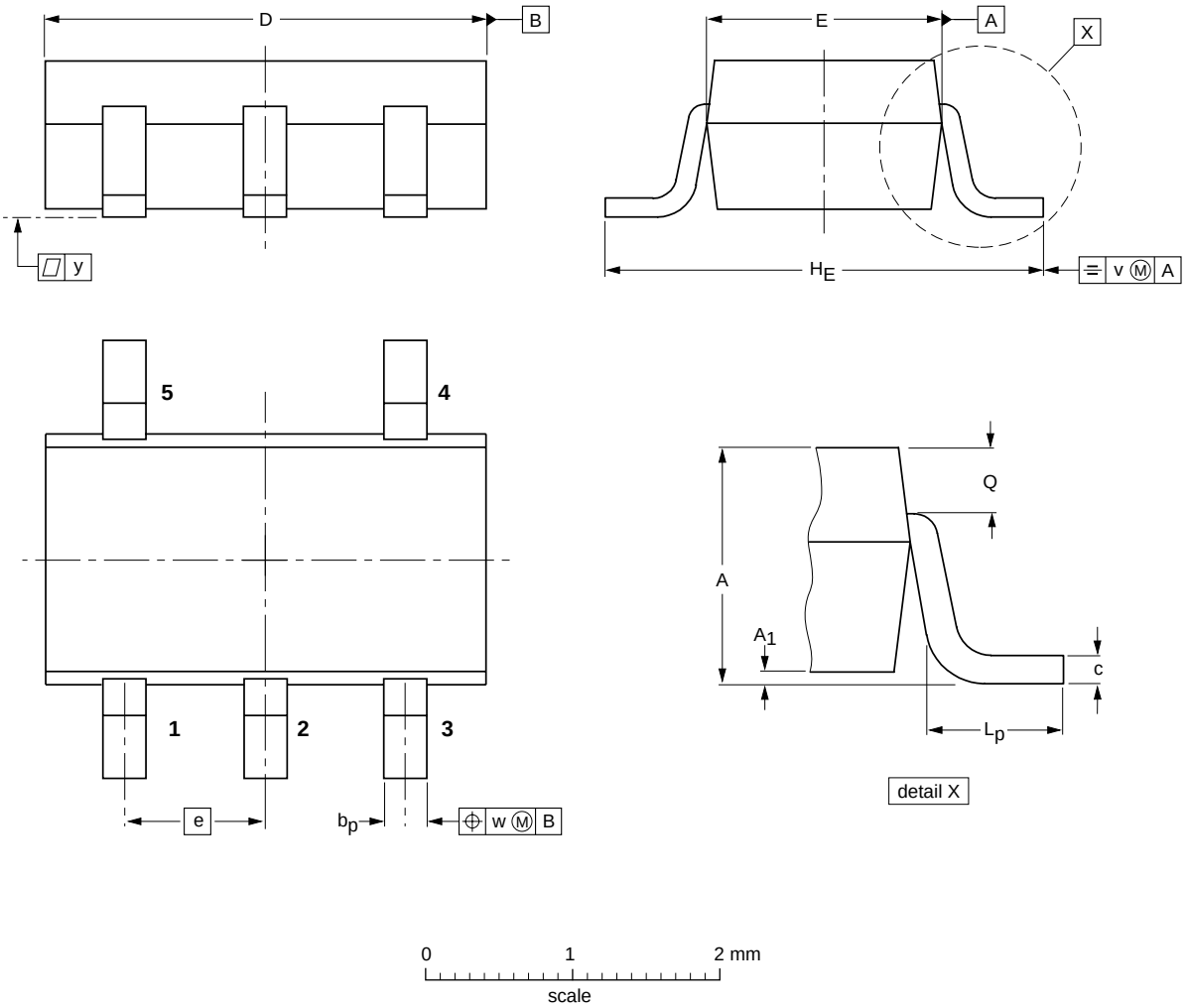


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Plastic surface mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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