SIEMENS

8M × 72-Bit Dynamic RAM Module (ECC - Module)

HYM 72V8000GS-50/-60
HYM 72V8010GS-50/-60

Preliminary Information

- 8 388 608 words by 72-bit ECC - mode, one bank organization
- Fast access and cycle time
  50 ns access time
  90 ns cycle time (-50 version)
  60 ns access time
  110 ns cycle time (-60 version)
- Fast page mode capability with
  35 ns cycle time (-50 version)
  40 ns cycle time (-60 version)
- Single + 3.3V ± 0.3 V supply
- Low power dissipation
  max. 4536 mW active (-50 version)
  max. 3888 mW active (-60 version)

  CMOS – 108 mW standby
  TTL – 180 mW standby
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$-only-refresh
- 9 decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully LVTTL & LVCMOS compatible
- 4 Byte interleave enabled, Dual Address inputs (A0/B0)
- Buffered inputs excepts $\overline{\text{RAS}}$ and DQ
- 168 pin, dual read-out, Single in-Line Memory Module
- Utilizes nine 8M × 8 -DRAMs and four BiCMOS 8-bit buffers/line drivers VT244A
- Two versions: HYM 72V8010GS with SOJ-components (9 mm module thickness)
  HYM 72V8000GS with TSOPII-components (4 mm module thickness)
- 4048 refresh cycles / 64 ms with 12 / 11 addressing
- Gold contact pad
- Double sided module with 25.35 mm (1000 mil) height

The HYM 72V8000/10GS-50/-60 is a 64 MByte DRAM module organized as 8 388 608 words by 72-bit in a 168-pin, dual read-out, single-in-line package comprising five HYB 3165800J/T 8M × 8 DRAMs in 500 mil wide SOJ or TSOPII - packages mounted together with nine 0.2 µF ceramic decoupling capacitors on a PC board. All inputs except $\overline{RAS}$ and DQ are buffered by using four BiCMOS 8-bit buffers/line drivers.

Each HYB 3165800J/T is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 72V8000GS-50	on request	L-DIM-168-4	DRAM module (access time 50 ns)
HYM 72V8000GS-60	on request	L-DIM-168-4	DRAM module (access time 60 ns)
HYM 72V8010GS-50	on request	L-DIM-168-4	DRAM module (access time 50 ns)
HYM 72V8010GS-60	on request	L-DIM-168-4	DRAM module (access time 60 ns)

Pin Names

A0-A12,B0	Row Address Inputs
A0-A11,B0	Column Address Inputs
DQ0 - DQ71	Data Input/Output
RAS0, RAS2	Row Address Strobe
CAS0 , CAS2	Column Address Strobe
WE0, WE2	Read / Write Input
OE0, OE2	Output Enable
Vcc	Power (+3.3 Volt)
Vss	Ground
PD1 - PD8	Presence Detect Pins
PDE	Presence Detect Enable
ID0 , ID1	ID indentification bit
N.C.	No Connection

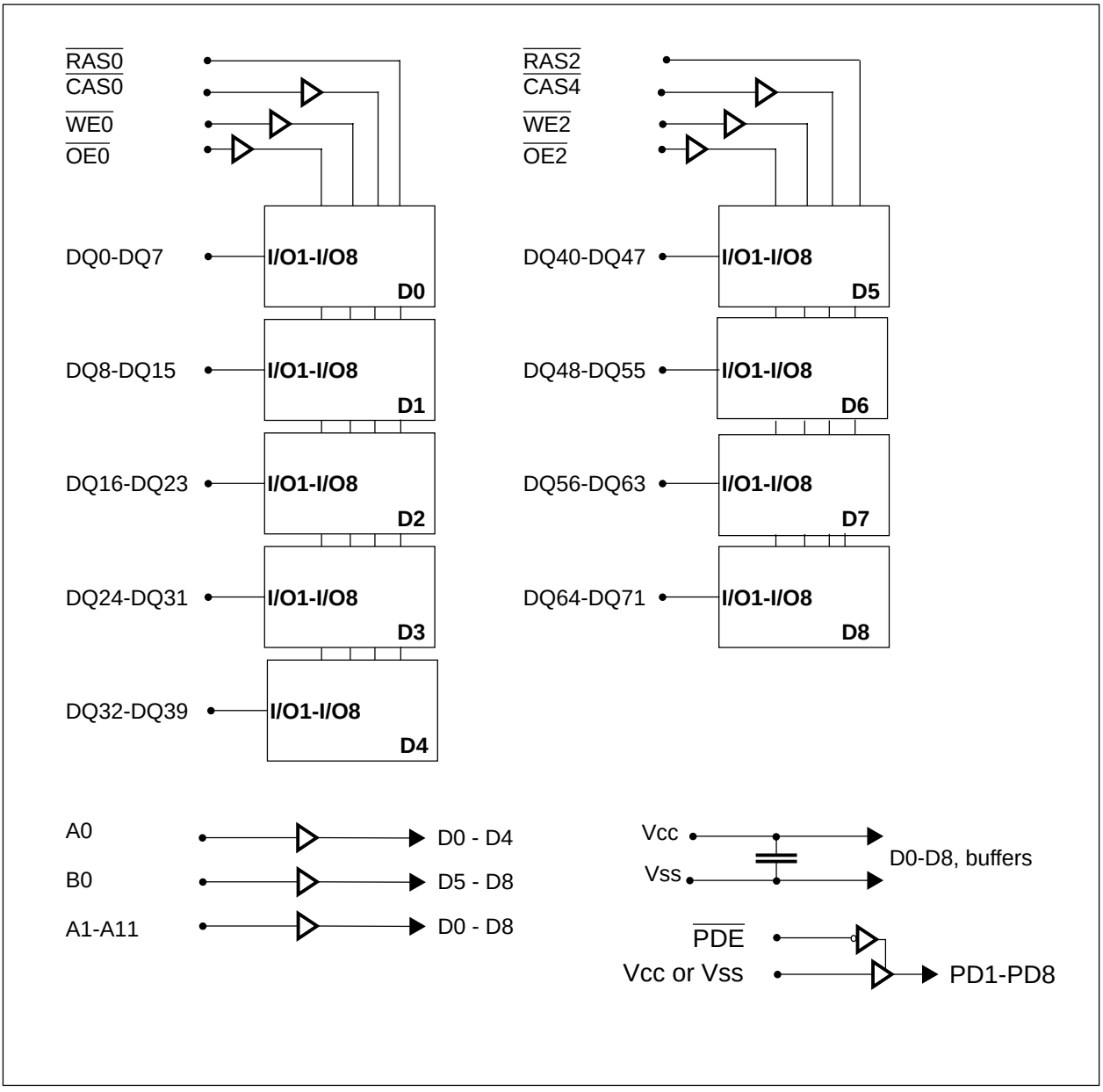
Presence-Detect and ID-pin Thruth Table:

Module	ID0	ID1	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8
HYM 728000GS-50	Vss	Vss	1	0	1	1	0	0	0	0
HYM 728000GS-60	Vss	Vss	1	0	1	1	0	1	1	0

Note: 1 = High Level (Driver Output) , 0 = Low Level (Driver Output) for $\overline{PDE}$ active (ground) . For $\overline{PDE}$ at a high level all PD terminal are in tri-state.

Pin Configuration

PIN #	Symbol	PIN #	Symbol		PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS		85	VSS	127	VSS
2	DQ0	44	OE2		86	DQ36	128	NC
3	DQ1	45	RAS2		87	DQ37	129	NC
4	DQ2	46	CAS4		88	DQ38	130	NC
5	DQ3	47	NC		89	DQ39	131	NC
6	VCC	48	WE2		90	VCC	132	PDE
7	DQ4	49	VCC		91	DQ40	133	VCC
8	DQ5	50	NC		92	DQ41	134	NC
9	DQ6	51	NC		93	DQ42	135	NC
10	DQ7	52	DQ18		94	DQ43	136	DQ54
11	DQ8	53	DQ19		95	DQ44	137	DQ55
12	VSS	54	VSS		96	VSS	138	VSS
13	DQ9	55	DQ20		97	DQ45	139	DQ56
14	DQ10	56	DQ21		98	DQ46	140	DQ57
15	DQ11	57	DQ22		99	DQ47	141	DQ58
16	DQ12	58	DQ23		100	DQ48	142	DQ59
17	DQ13	59	VCC		101	DQ49	143	VCC
18	VCC	60	DQ24		102	VCC	144	DQ60
19	DQ14	61	NC		103	DQ50	145	NC
20	DQ15	62	NC		104	DQ51	146	NC
21	DQ16	63	NC		105	DQ52	147	NC
22	DQ17	64	NC		106	DQ53	148	NC
23	VSS	65	DQ25		107	VSS	149	DQ61
24	NC	66	DQ26		108	NC	150	DQ62
25	NC	67	DQ27		109	NC	151	DQ63
26	VCC	68	VSS		110	VCC	152	VSS
27	WE0	69	DQ28		111	NC	153	DQ64
28	CAS0	70	DQ29		112	NC	154	DQ65
29	NC	71	DQ30		113	NC	155	DQ66
30	RAS0	72	DQ31		114	NC	156	DQ67
31	OE0	73	VCC		115	NC	157	VCC
32	VSS	74	DQ32		116	VSS	158	DQ68
33	A0	75	DQ33		117	A1	159	DQ69
34	A2	76	DQ34		118	A3	160	DQ70
35	A4	77	DQ35		119	A5	161	DQ71
36	A6	78	VSS		120	A7	162	VSS
37	A8	79	PD1		121	A9	163	PD2
38	A10	80	PD3		122	A11	164	PD4
39	NC	81	PD5		123	NC	165	PD6
40	VCC	82	PD7		124	VCC	166	PD8
41	NC	83	ID0 (VSS)		125	NC	167	ID1 (VSS)
42	NC	84	VCC		126	B0	168	VCC



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 ˚C
Storage temperature range..... – 55 to + 125 ˚C
Soldering temperature ..... 260 ˚C
Soldering time..... 10 s
Input/output voltage ..... -0.5 to min (Vcc+0.5, 4.6) V
Power supply voltage..... – 0.5V to 4.6 V
Power dissipation..... 5,8 W
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics [1)]

T_A = 0 to 70 ˚C; V_{CC} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	–
Input low voltage	V_{IL}	– 0.3	0.8	V	–
Output high voltage (LVTTL) Output „H“ level voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	–
Output low voltage (LVTTL) Output „L“ level voltage (I_{OUT} = + 2 mA)	V_{OL}	–	0.4	V	–
Output high voltage (LVCMOS) Output „H“ level voltage (I_{OUT} = – 100 A)	V_{OH}	Vcc-0.2	–	V	–
Output low voltage (LVCMOS) Output „L“ level voltage (I_{OUT} = + 100 A)	V_{OL}	–	0.2	V	–
Input leakage current (0 V < V_{IN} < Vcc, all other pins = 0 V)	$I_{I(L)}$	– 20	20	µA	–
Output leakage current (DO is disabled, 0 V < V_{OUT} < Vcc)	$I_{O(L)}$	– 20	20	µA	–
Average V_{CC} supply current: HYM 72V8000/10GS-60 HYM 72V8000/10GS-70 ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	I_{CC1}	 – –	 1260 1080	 mA mA	2), 3)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, one address change)	I_{CC2}	–	50	mA	–

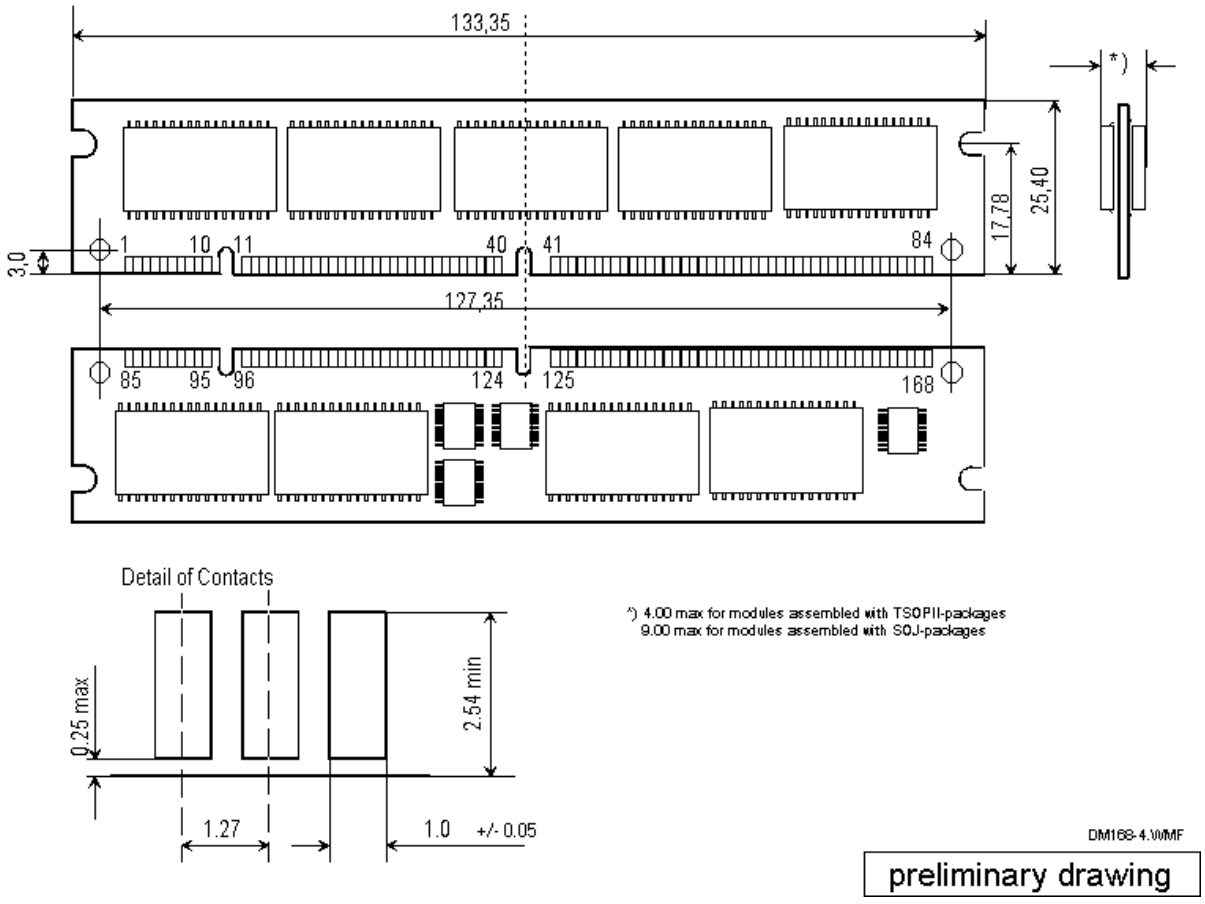
Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles:	I_{CC3}				2)
HYM 72V8000/10GS-50		–	1260	mA	
HYM 72V8000/10GS-60		–	1080	mA	
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					
Average V_{CC} supply current during fast page mode:	I_{CC4}				2), 3)
HYM 72V8000/10GS-50		–	765	mA	
HYM 72V8000/10GS-60		–	675	mA	
($\overline{RAS}$ = $V_{IL,}$ $\overline{CAS}$, address cycling t_{PC} = t_{PC} min.)		–			
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V, one address change)	I_{CC5}	–	30	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}				1)
HYM 72V8000/10GS-50		–	1260	mA	
HYM 72V8000/10GS-60		–	1080	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					

Capacitance

T_A = 0 to 70 °C; V_{CC} = 3.3 V ± 0.3 V; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11,B0)	C_{I1}	–	10	pF
Input capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	–	50	pF
Input capacitance ($\overline{CAS0}$, $\overline{CAS4}$)	C_{I3}	–	15	pF
Input capacitance ($\overline{WE0}$,$\overline{WE2}$,$\overline{OE0}$,$\overline{OE2}$)	C_{I4}	–	15	pF
I/O capacitance (DQ0-DQ71)	C_{IO1}	–	15	pF

L-DIM-168-4
Module package
(dual read-out, single in-line memory module)



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