
HN58C1001 Series

131072-word \times 8-bit Electrically Erasable and
Programmable CMOS ROM

HITACHI

ADE-203-028F (Z)

Rev. 6.0

Apr. 8, 1997

Description

The Hitachi HN58C1001 is a electrically erasable and programmable ROM organized as 131072-word \times 8-bit. It has realized high speed, low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 128-byte page programming function to make the write operations faster.

Features

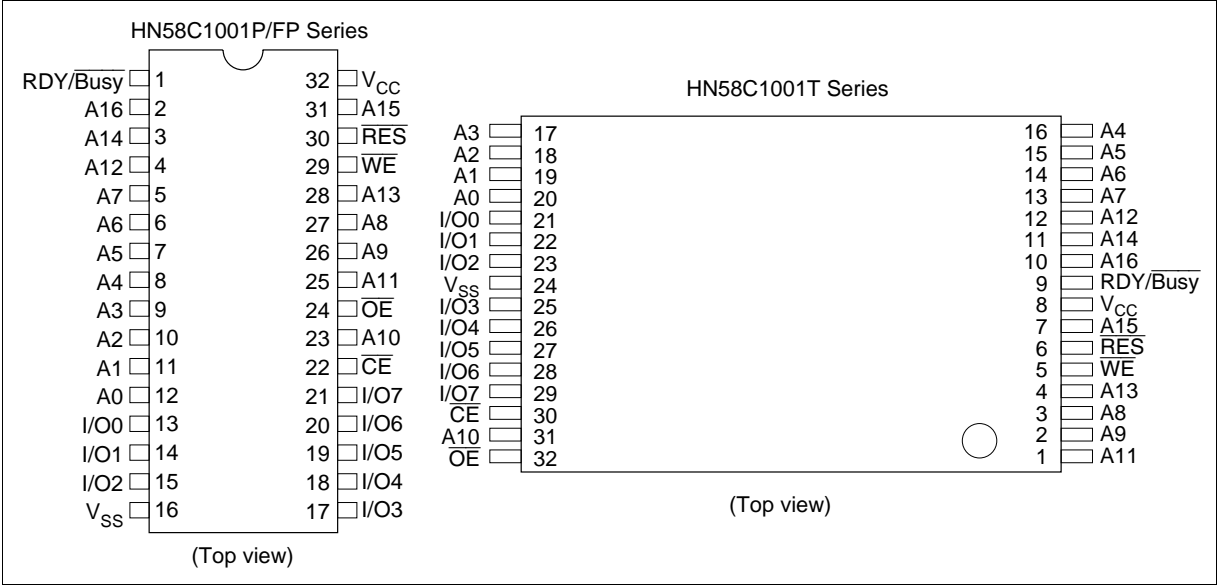
- Single supply: 5.0 V \pm 10%
- Access time: 150 ns (max)
- Power dissipation
 - Active: 20 mW/MHz, (typ)
 - Standby: 110 μ W (max)
- On-chip latches: address, data, $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$
- Automatic byte write: 10 ms (max)
- Automatic page write (128 bytes): 10 ms (max)
- $\overline{\text{Data}}$ polling and $\overline{\text{RDY/Busy}}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^4 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{\text{RES}}$ pin

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Ordering Information

Type No.	Access time	Package
HN58C1001P-15	150 ns	600 mil 32-pin plastic DIP (DP-32)
HN58C1001FP-15	150 ns	525 mil 32-pin plastic SOP (FP-32D)
HN58C1001T-15	150 ns	8 × 14 mm 32-pin plastic TSOP (TFP-32DA)

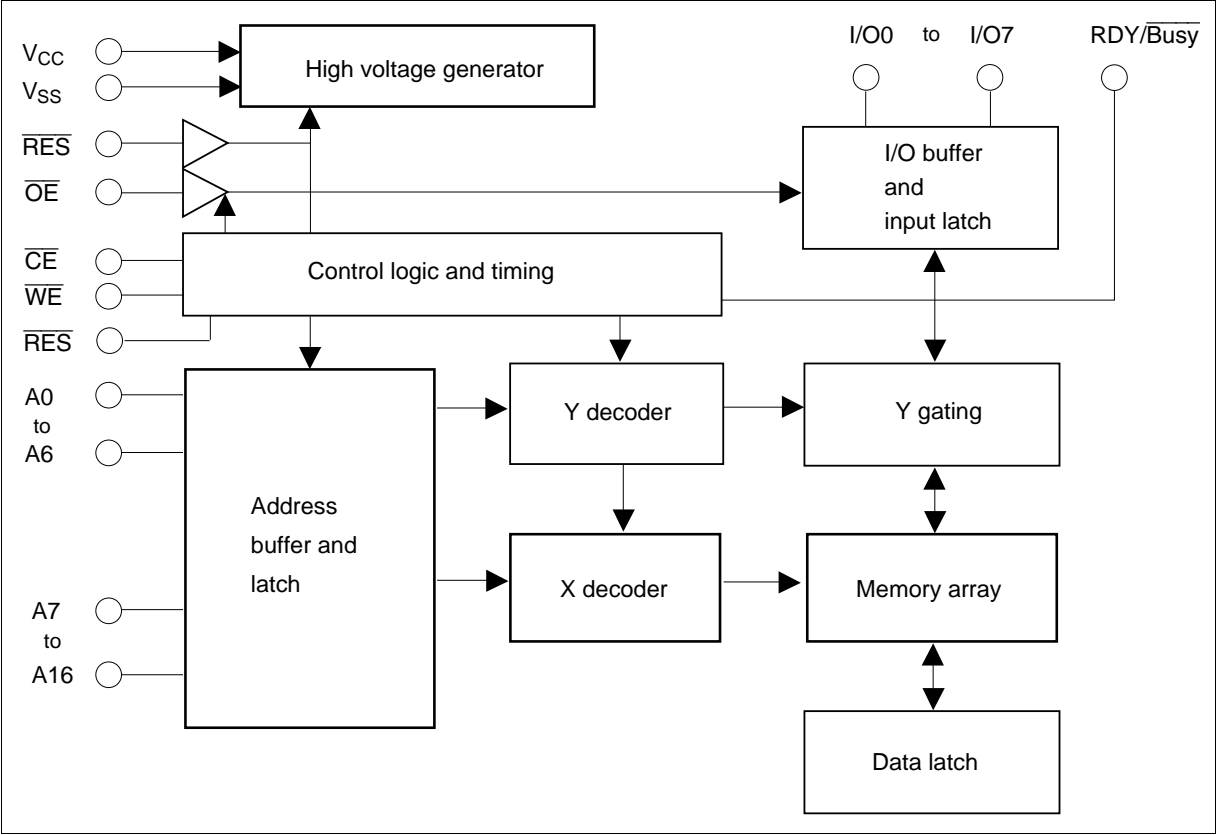
Pin Arrangement



Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
OE	Output enable
CE	Chip enable
WE	Write enable
V _{CC}	Power supply
V _{SS}	Ground
RDY/Busy	Ready busy
RES	Reset

Block Diagram



Operation Table

Operation	\overline{CE}	\overline{OE}	\overline{WE}	\overline{RES}	RDY/\overline{Busy}	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H^{*1}	High-Z	Dout
Standby	V_{IH}	\times^{*2}	\times	\times	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	\times	\times	V_{IH}	\times	—	—
	\times	V_{IL}	\times	\times	—	—
Data Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Dout (I/O7)
Program reset	\times	\times	\times	V_{IL}	High-Z	High-Z

Notes: 1. Refer to the recommended DC operating conditions.
2. \times : Don't care

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V _{SS}	V _{CC}	−0.6 to +7.0	V
Input voltage relative to V _{SS}	V _{in}	−0.5* ¹ to +7.0	V
Operating temperature range* ²	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C

Notes: 1. V_{in} min = −3.0 V for pulse width ≤ 50 ns
2. Including electrical characteristics and data retention

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input voltage	V _{IL}	−0.3* ¹	—	0.8	V
	V _{IH}	2.2	—	V _{CC} + 0.3	V
	V _H	V _{CC} − 0.5	—	V _{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

Note: 1. V_{IL} (min): −1.0 V for pulse width ≤ 50 ns

DC Characteristics (Ta = 0 to +70 °C, V_{CC} = 5.0V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	2* ¹	μA	V _{CC} = 5.5 V, V _{in} = 5.5 V
Output leakage current	I _{LO}	—	—	2	μA	V _{CC} = 5.5 V, V _{out} = 5.5/0.4 V
Standby V _{CC} current	I _{CC1}	—	—	20	μA	\overline{CE} = V _{CC}
	I _{CC2}	—	—	1	mA	\overline{CE} = V _{IH}
Operating V _{CC} current	I _{CC3}	—	—	15	mA	I _{out} = 0 mA, Duty = 100%, Cycle = 1 μs at V _{CC} = 5.5 V
		—	—	50	mA	I _{out} = 0 mA, Duty = 100%, Cycle = 150 ns at V _{CC} = 5.5 V
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = −400 μA

Notes: 1. I_{LI} on RES: 100 μA (max)

Capacitance ($T_a = 25^{\circ}\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*1	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*1	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics ($T_a = 0\text{ to }+70^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$)

Test Conditions

- Input pulse levels: 0.4 V to $\frac{2.4\text{ V}}{0\text{ V to }V_{CC}}$ (RES pin)
- Input rise and fall time: $\leq 20\text{ ns}$
- Output load: 1TTL Gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

Read Cycle

Parameter	Symbol	HN58C1001-15		Unit	Test conditions
		Min	Max		
Address to output delay	t_{ACC}	—	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
\overline{CE} to output delay	t_{CE}	—	150	ns	$\overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
\overline{OE} to output delay	t_{OE}	10	75	ns	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$
Address to output hold	t_{OH}	0	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
\overline{OE} (\overline{CE}) high to output float*1	t_{DF}	0	50	ns	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$
\overline{RES} low to output float*1	t_{DFR}	0	350	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$
\overline{RES} to output delay	t_{RR}	0	450	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$

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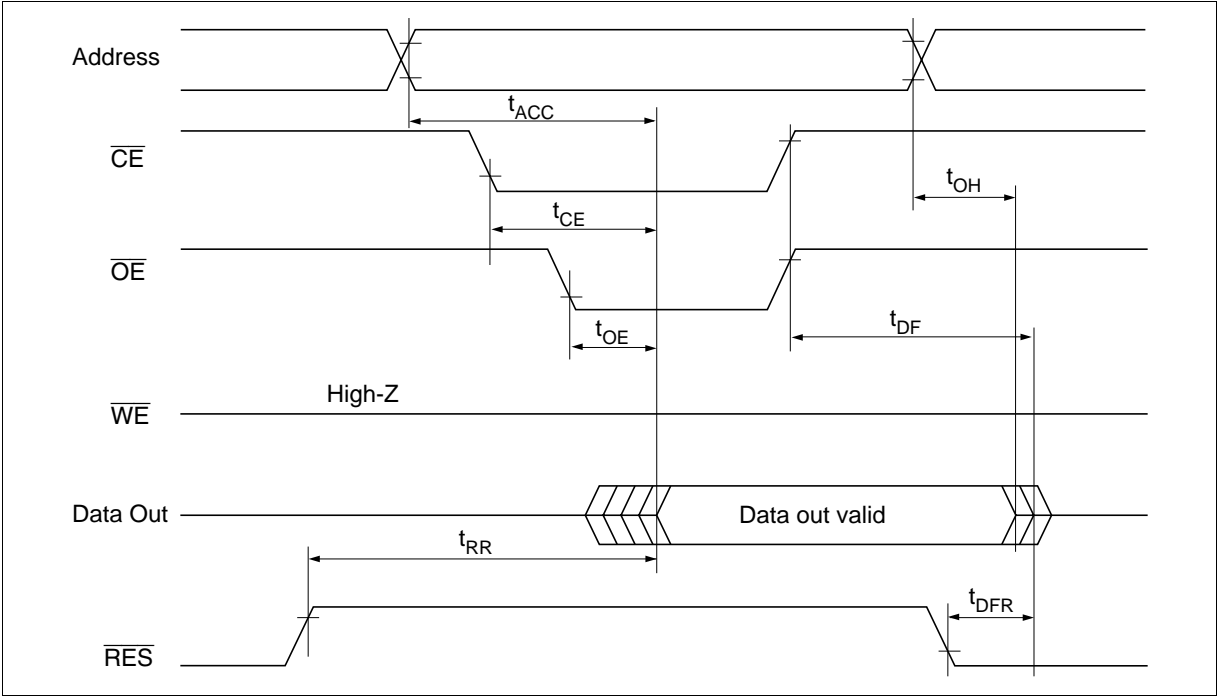
Write Cycle

Parameter	Symbol	Min*2	Typ	Max	Unit	Test conditions
Address setup time	t _{AS}	0	—	—	ns	
Address hold time	t _{AH}	150	—	—	ns	
$\overline{\text{CE}}$ to write setup time ($\overline{\text{WE}}$ controlled)	t _{CS}	0	—	—	ns	
$\overline{\text{CE}}$ hold time ($\overline{\text{WE}}$ controlled)	t _{CH}	0	—	—	ns	
$\overline{\text{WE}}$ to write setup time ($\overline{\text{CE}}$ controlled)	t _{WS}	0	—	—	ns	
$\overline{\text{WE}}$ hold time ($\overline{\text{CE}}$ controlled)	t _{WH}	0	—	—	ns	
$\overline{\text{OE}}$ to write setup time	t _{OES}	0	—	—	ns	
$\overline{\text{OE}}$ hold time	t _{OEH}	0	—	—	ns	
Data setup time	t _{DS}	100	—	—	ns	
Data hold time	t _{DH}	10	—	—	ns	
$\overline{\text{WE}}$ pulse width ($\overline{\text{WE}}$ controlled)	t _{WP}	250	—	—	ns	
$\overline{\text{CE}}$ pulse width ($\overline{\text{CE}}$ controlled)	t _{CW}	250	—	—	ns	
Data latch time	t _{DL}	300	—	—	ns	
Byte load cycle	t _{BLC}	0.55	—	30	μs	
Byte load window	t _{BL}	100	—	—	μs	
Write cycle time	t _{WC}	—	—	10*3	ms	
Time to device busy	t _{DB}	120	—	—	ns	
Write start time	t _{DW}	150*4	—	—	ns	
Reset protect time	t _{RP}	100	—	—	μs	
Reset high time*5	t _{RES}	1	—	—	μs	

- Notes:
1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
 2. Use this device in longer cycle than this value.
 3. t_{WC} must be longer than this value unless polling techniques or RDY/ $\overline{\text{Busy}}$ are used. This device automatically completes the internal write operation within this value.
 4. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/ $\overline{\text{Busy}}$ are used.
 5. This parameter is sampled and not 100% tested.
 6. A7 to A16 are page addresses and must be same within the page write operation.
 7. See AC read characteristics.

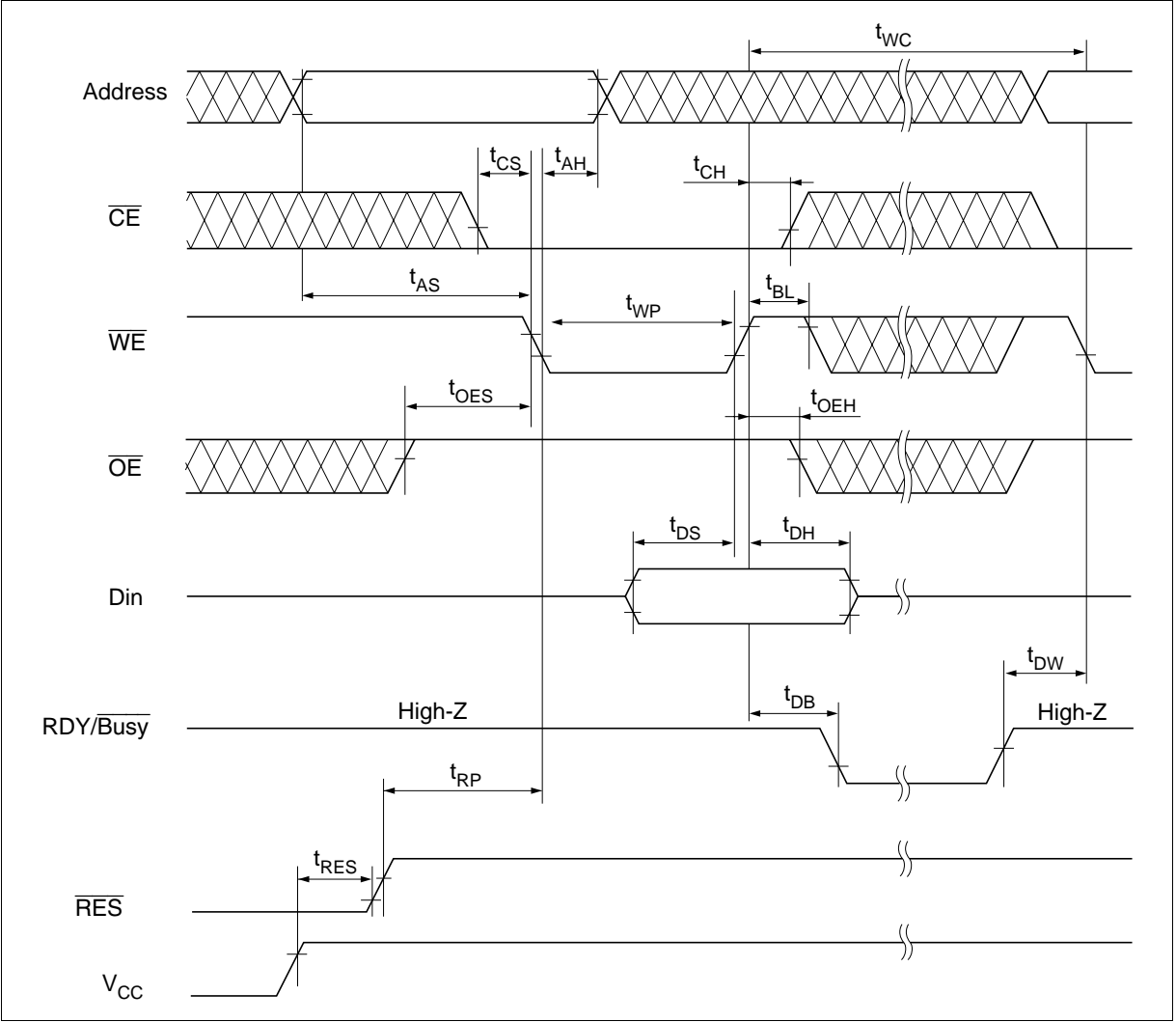
Timing Waveforms

Read Timing Waveform

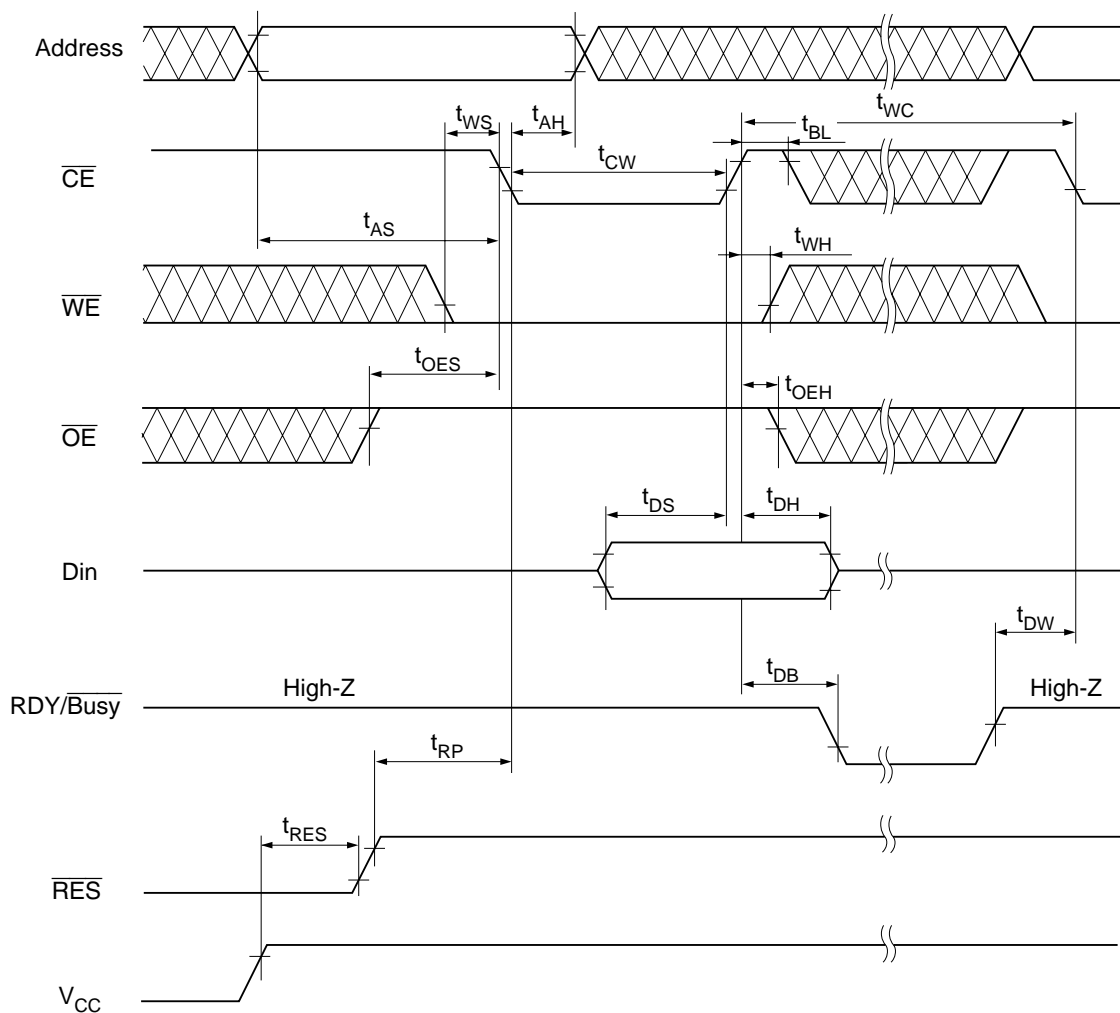


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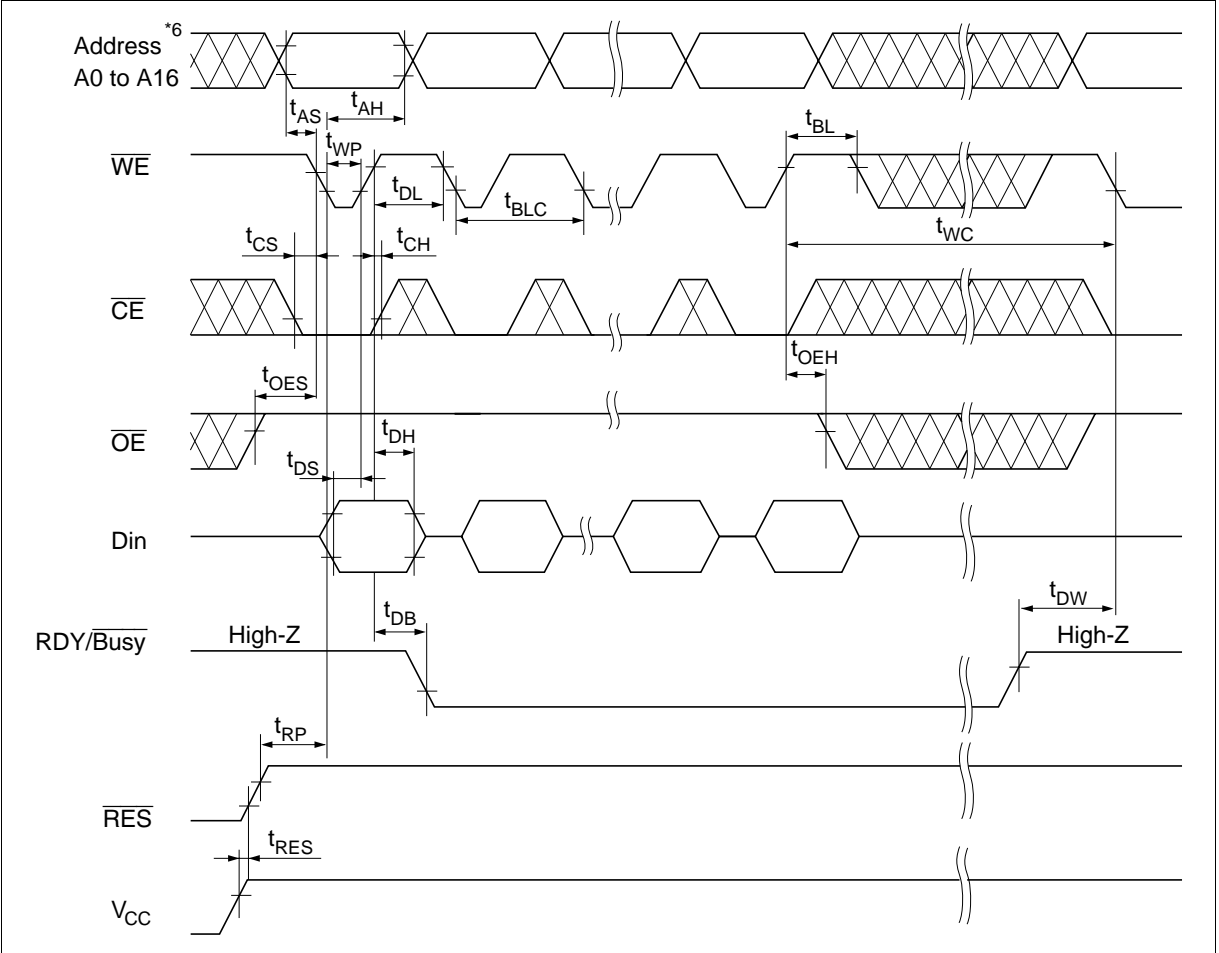
Byte Write Timing Waveform (1) ($\overline{\text{WE}}$ Controlled)



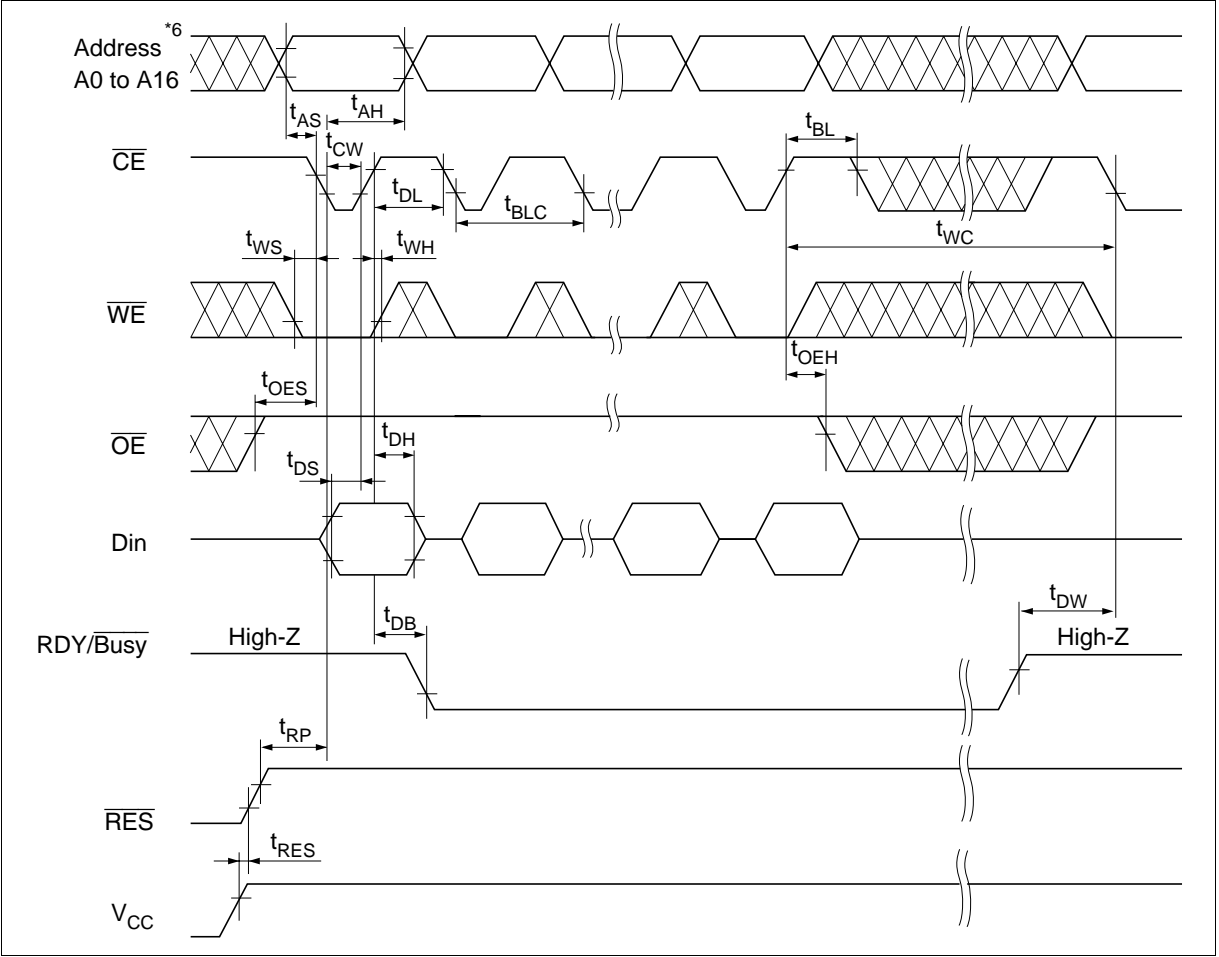
Byte Write Timing Waveform (2) ($\overline{\text{CE}}$ Controlled)



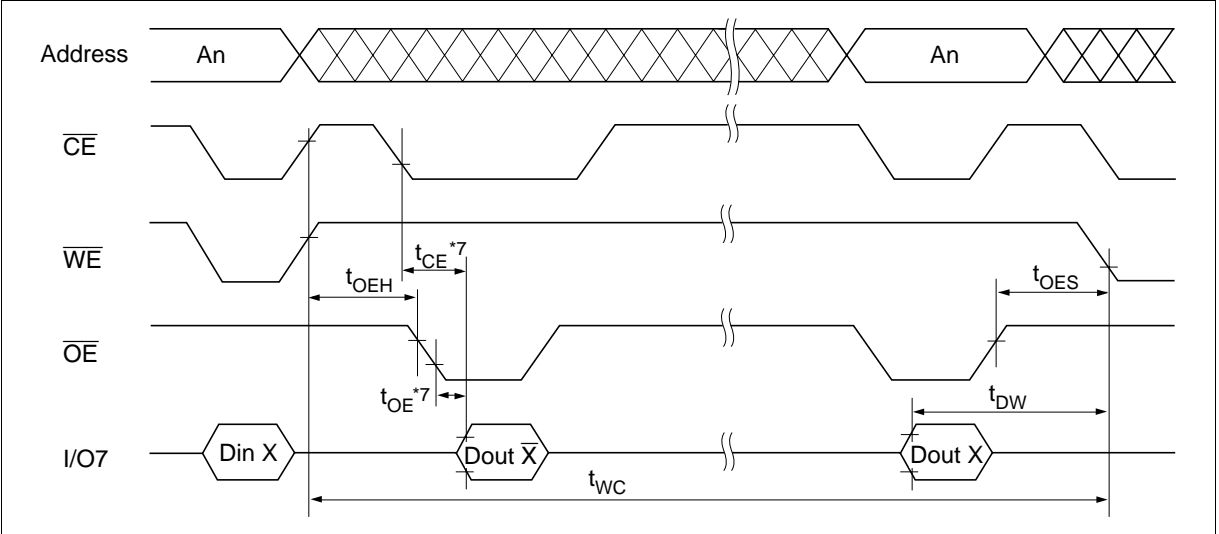
Page Write Timing Waveform (1) ($\overline{\text{WE}}$ Controlled)



Page Write Timing Waveform (2) ($\overline{\text{CE}}$ Controlled)



Data Polling Timing Waveform

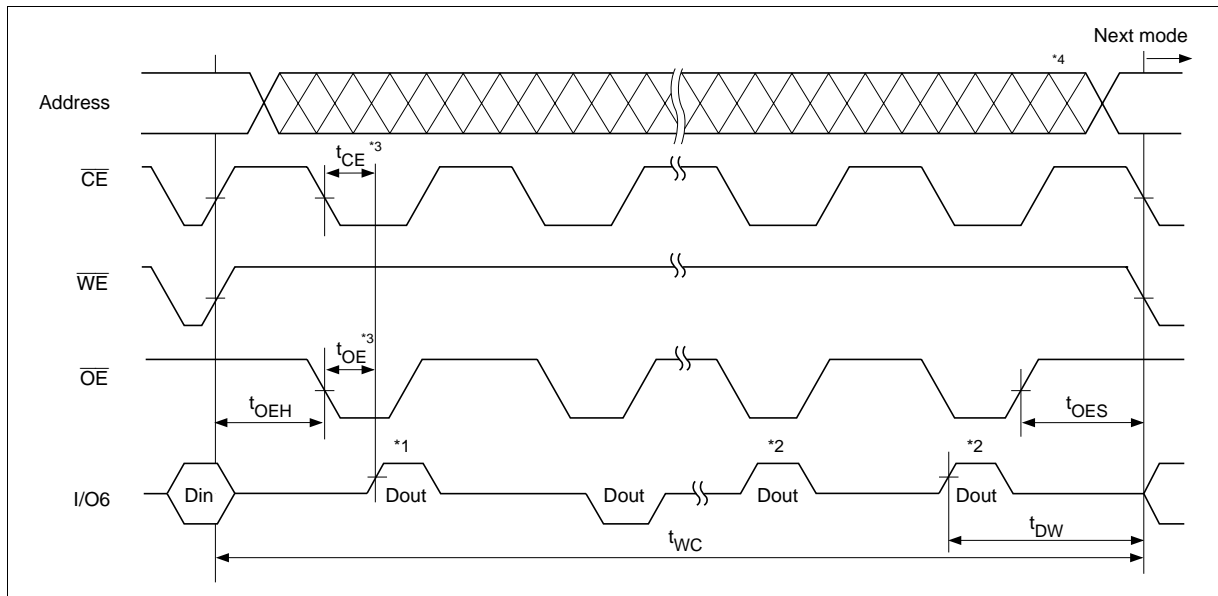


Toggle bit

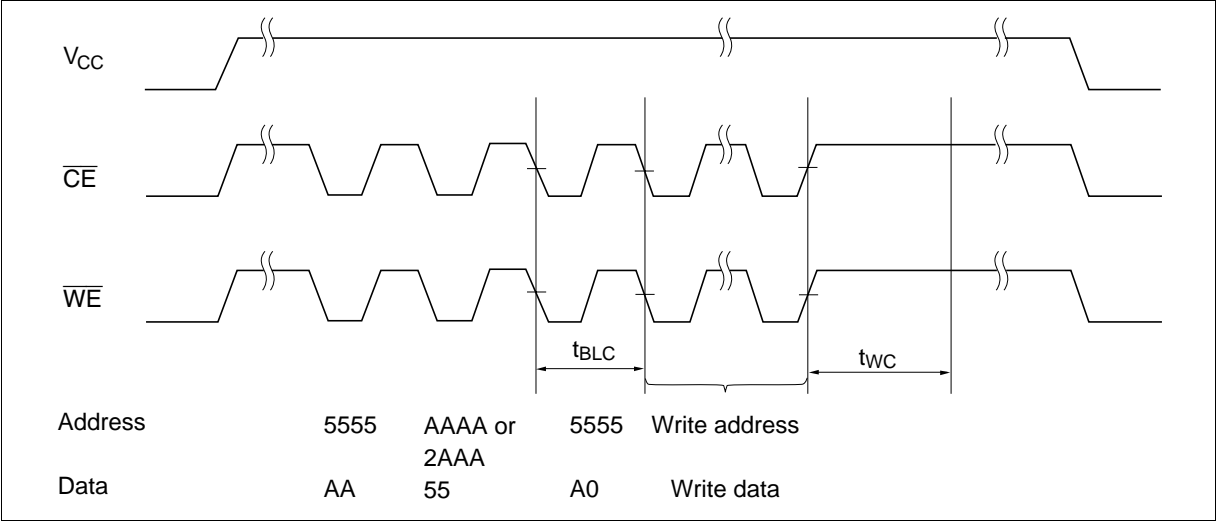
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from “1” to “0” (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

- Notes:
1. I/O6 beginning state is “1”.
 2. I/O6 ending state will vary.
 3. See AC read characteristics.
 4. Any location can be used, but the address must be fixed.

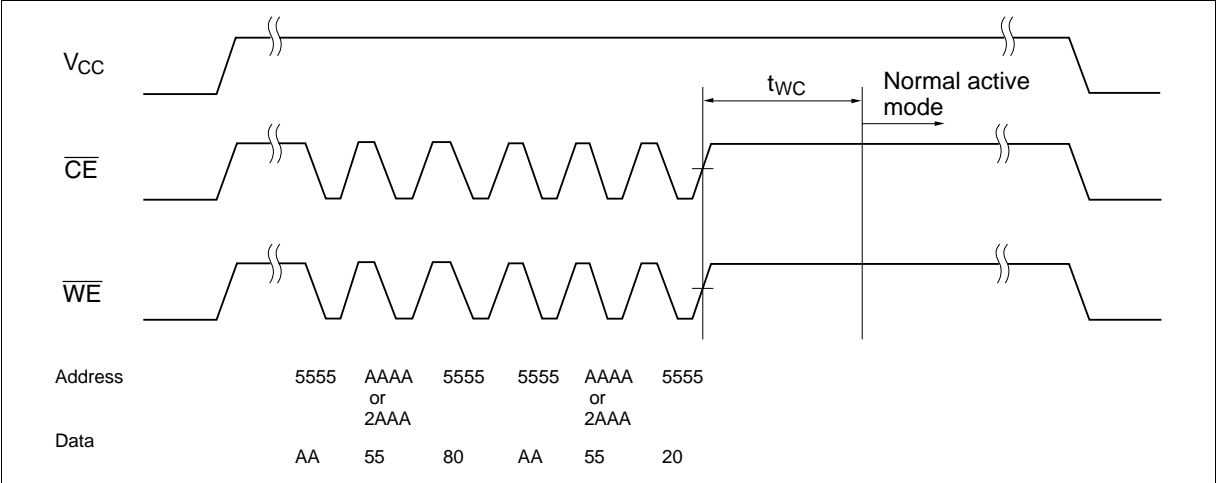
Toggle bit Waveform



Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 128 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 μ s from the preceding falling edge of \overline{WE} or \overline{CE} . When \overline{CE} or \overline{WE} is kept high for 100 μ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

Data Polling

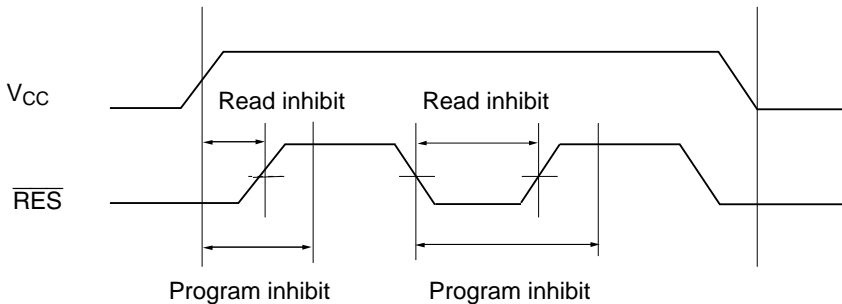
Data polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/Busy Signal

RDY/Busy signal also allows status of the EEPROM to be determined. The RDY/Busy signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of write cycle, the RDY/Busy signal changes state to high impedance.

\overline{RES} Signal

When \overline{RES} is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping \overline{RES} low when V_{CC} is switched. \overline{RES} should be high during read and programming because it doesn't provide a latch function.



\overline{WE} , \overline{CE} Pin Operation

During a write cycle, addresses are latched by the falling edge of \overline{WE} or \overline{CE} , and data is latched by the rising edge of \overline{WE} or \overline{CE} .

Write/Erase Endurance and Data Retention Time

The endurance is 10^4 cycles in case of the page programming and 10^3 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

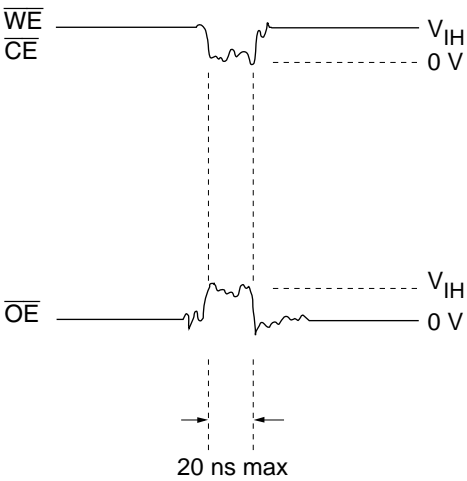
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20 ns or less in program mode.

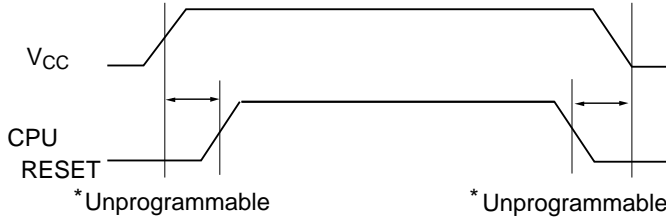
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

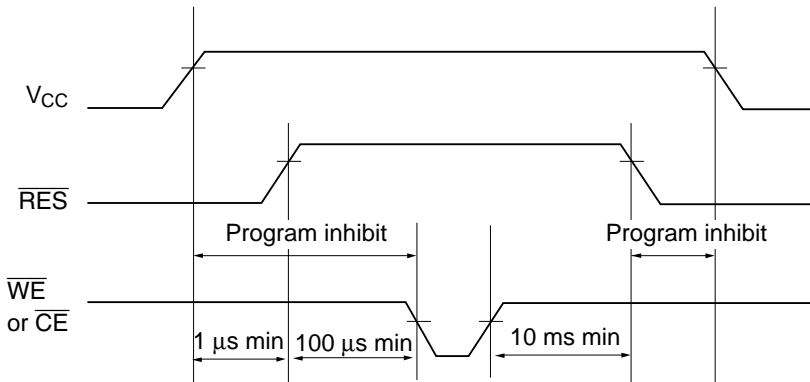
Note: The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.



(1) Protection by \overline{RES}

The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's RES pin. RES should be kept V_{SS} level during V_{CC} on/off.

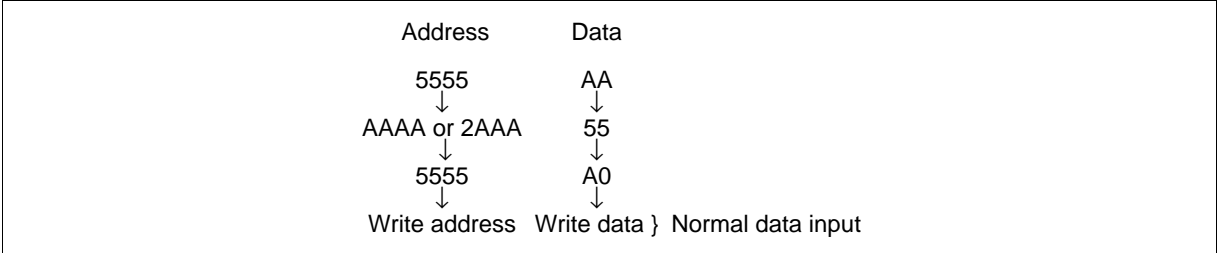
The EEPROM brakes off programming operation when RES becomes low, programming operation doesn't finish correctly in case that RES falls low during programming operation. RES should be kept high for 10 ms after the last data input.



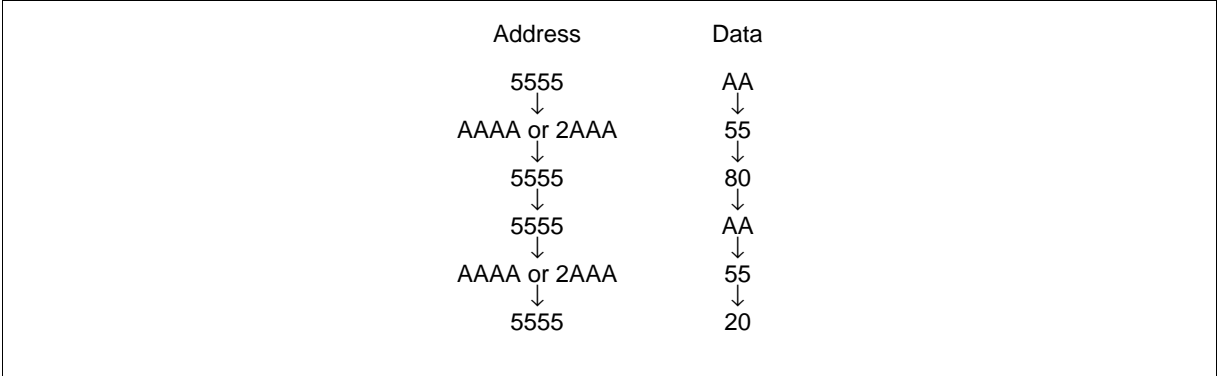
HN58C1001 Series

3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.



The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data can not be written.

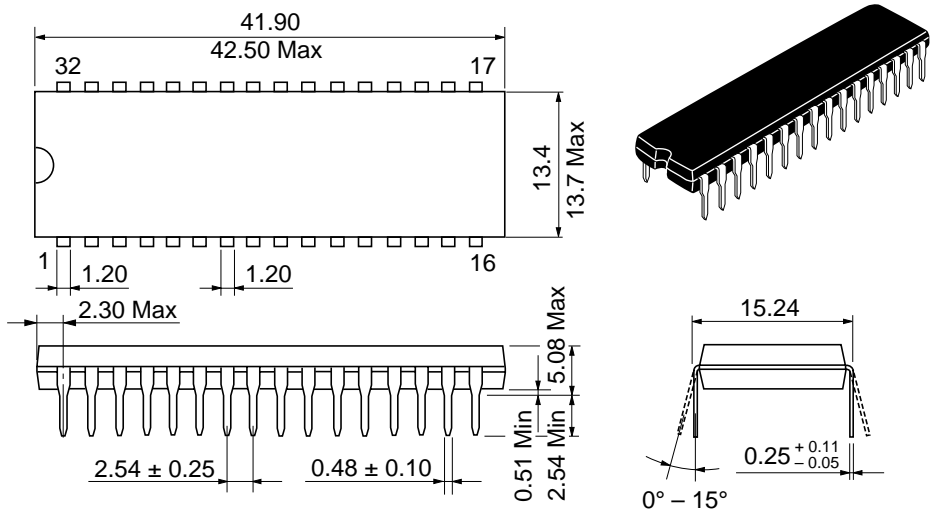


The software data protection is not enabled at the shipment.
Note: There are some differences between Hitachi's and other company's for enable/disable sequence of software data protection. If there are any questions , please contact with Hitachi sales offices.

Package Dimensions

HN58C1001P Series (DP-32)

Unit: mm

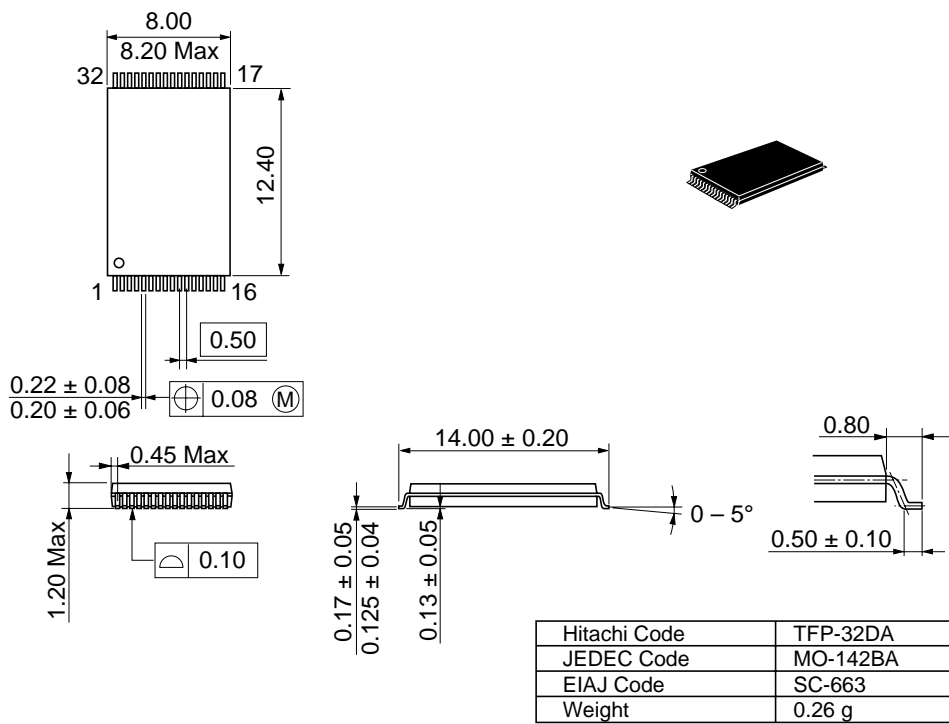


Hitachi Code	DP-32
JEDEC Code	—
EIAJ Code	SC-613
Weight	5.1 g

Package Dimensions (cont.)

HN58C1001T Series (TFP-32DA)

Unit: mm



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jul. 11, 1991	Initial issue	K. Furusawa	T. Wada
1.0	Jan. 10, 1992	<p>Recommended DC Operating Conditions</p> <p>Addition of V_H</p> <p>DC Characteristics</p> <p>I_{CC3} max: 40 mA to 50 mA</p> <p>I_{CC3} test: Cycle = 200 ns to Cycle = 150 ns</p> <p>V_{IH} max: $V_{CC} + 1$ V to $V_{CC} + 0.3$ V</p> <p>V_H min: $V_{CC} - 1.0$ V to $V_{CC} - 0.5$ V</p> <p>AC Characteristics</p> <p>Change of Test Conditions</p> <p>Reference level: 1.8 V to 2.0 V</p> <p>t_{DL} min: 200 ns to 300 ns</p> <p>t_{BLC} min: 0.35 μs to 0.55 μs</p> <p>t_{WP}/t_{CW} min: 150 ns to 250 ns</p> <p>t_{CS}/t_{CH} to t_{WS}/t_{WH} (\overline{CE} Controlled)</p> <p>Functional Description</p> <p>Deletion of Write Protection (2)</p> <p>Data Protection 2:</p> <p>during programming because to during programming and read because unprogrammable, standby or readout state to unprogrammable state</p> <p>Deletion of protection of mistake</p> <p>by $\overline{CE} = V_{CC}$ or $\overline{OE} = \text{Low}$ or $\overline{WE} = V_{CC}$ level at V_{CC} on/off</p> <p>Software data protection</p> <p>Address: AAAA to AAAA or 2AAA</p> <p>Change of Timing Waveforms</p>	K. Furusawa	T. Wada
2.0	Jan. 21, 1993	<p>Deletion of HN58C1001-12</p> <p>AC Characteristics</p> <p>t_{DH} min: 0 ns to 10 ns</p> <p>Deletion of Mode Description</p> <p>Addition of Reset function</p> <p>Change of erase/write cycles in page mode: 10^5 to 10^4</p> <p>Change of erase/write cycles in byte mode: 10^4 to 10^3</p>	K. Furusawa	K. Furusawa
3.0	Apr. 23, 1993	Addition of Toggle Bit	M. Terasawa	K. Furusawa
4.0	Nov. 25, 1994	<p>Capacitance</p> <p>Addition of note 1</p> <p>AC Characteristics</p> <p>Write cycle: Addition of note 2,3</p> <p>Addition of t_{DW} min: 150 ns</p> <p>Page write timing waveform</p> <p>Addition of note 1</p>	M. Terasawa	T. Muto
5.0	May. 23, 1995	Deletion of HN58C1001R series (TFP-32DAR)	M. Terasawa	T. Muto

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Revision Record (cont.)

Rev.	Date	Contents of Modification	Drawn by	Approved by
6.0	Apr. 8, 1997	Change of format AC Characteristics Addition of note.6 Timing Waveforms Toggle bit Addition of note.3, 4 Functional Description Addition of CPU Reset timing waveform Data protection 3: Addition of note		
