
HB56T432D Series, HB56T433D Series

4,194,304-word $\times$ 32-bit High Density Dynamic RAM Module

HITACHI

ADE-203-733A (Z)

Rev.1.0

Feb. 27, 1997

Description

The HB56T432D is a $4\text{M} \times 32$ dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 8 pieces of 16-Mbit DRAM (HM5116400) sealed in TSOP package. The HB56T433D is a $4\text{M} \times 32$ dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 8 pieces of 16-Mbit DRAM (HM5117400) sealed in TSOP package. An outline of the HB56T432D, HB56T433D is 72-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56T432D, HB56T433D make high density mounting possible without surface mount technology. The HB56T432D, HB56T433D provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 72-pin Zig Zag Dual tabs socket type
 - Outline: 59.69 mm (Length) $\times$ 25.40 mm (Height) $\times$ 3.80 mm (Thickness)
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time: $t_{\text{RAC}} = 50/60/70$ ns (max)
 $t_{\text{CAC}} = 13/15/18$ ns (max)
- Low power dissipation
 - Active mode: 3.78/3.36/2.94 W (max) (HB56T432D Series)
4.20/3.78/3.36 W (max) (HB56T433D Series)
 - Standby mode (TTL): 84 mW (max)
(CMOS): 6.3 mW (max) (L-version)
- Fast page mode capability

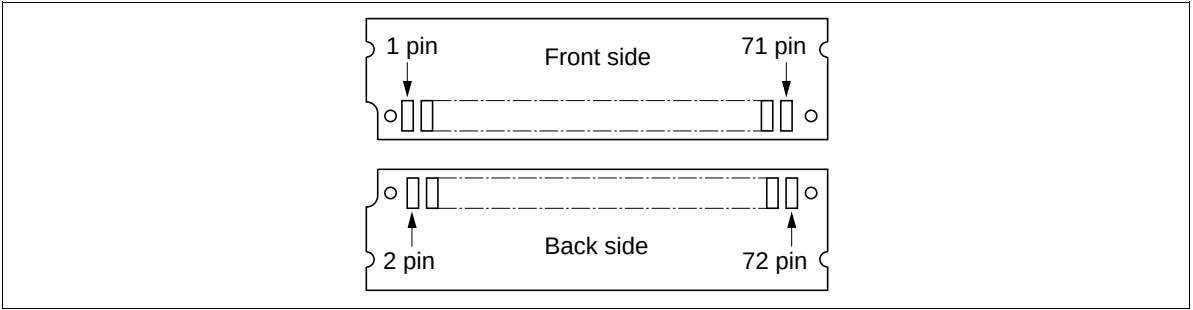
HB56T432D Series, HB56T433D Series

- Refresh period
 - 4096 refresh cycles: 64 ms (HB56T432D Series)
128 ms (L-version)
 - 2048 refresh cycles: 32 ms (HB56T433D Series)
128 ms (L-version)
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56T432D-5	50 ns	72-pin small outline DIMM	Gold
HB56T432D-6	60 ns		
HB56T432D-7	70 ns		
HB56T432D-5L	50 ns		
HB56T432D-6L	60 ns		
HB56T432D-7L	70 ns		
HB56T433D-5	50 ns		
HB56T433D-6	60 ns		
HB56T433D-7	70 ns		
HB56T433D-5L	50 ns		
HB56T433D-6L	60 ns		
HB56T433D-7L	70 ns		

Pin Arrangement



Pin Arrangement

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	37	DQ18	2	DQ0	38	DQ19
3	DQ1	39	V _{SS}	4	DQ2	40	CE0
5	DQ3	41	CE2	6	DQ4	42	CE3
7	DQ5	43	CE1	8	DQ6	44	RE0
9	DQ7	45	NC	10	V _{CC}	46	NC
11	PD1	47	WE	12	A0	48	NC
13	A1	49	DQ20	14	A2	50	DQ21
15	A3	51	DQ22	16	A4	52	DQ23
17	A5	53	DQ24	18	A6	54	DQ25
19	A10	55	NC	20	NC	56	DQ27
21	DQ9	57	DQ28	22	DQ10	58	DQ29
23	DQ11	59	DQ31	24	DQ12	60	DQ30
25	DQ13	61	V _{CC}	26	DQ14	62	DQ32
27	DQ15	63	DQ33	28	A7	64	DQ34
29	A11 (NC)* ¹	65	NC	30	V _{CC}	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	NC	69	PD5	34	RE2	70	PD6
35	DQ16	71	PD7	36	NC	72	V _{SS}

Note: 1. A11: HB56T432D, NC: HB56T433D

HB56T432D Series, HB56T433D Series

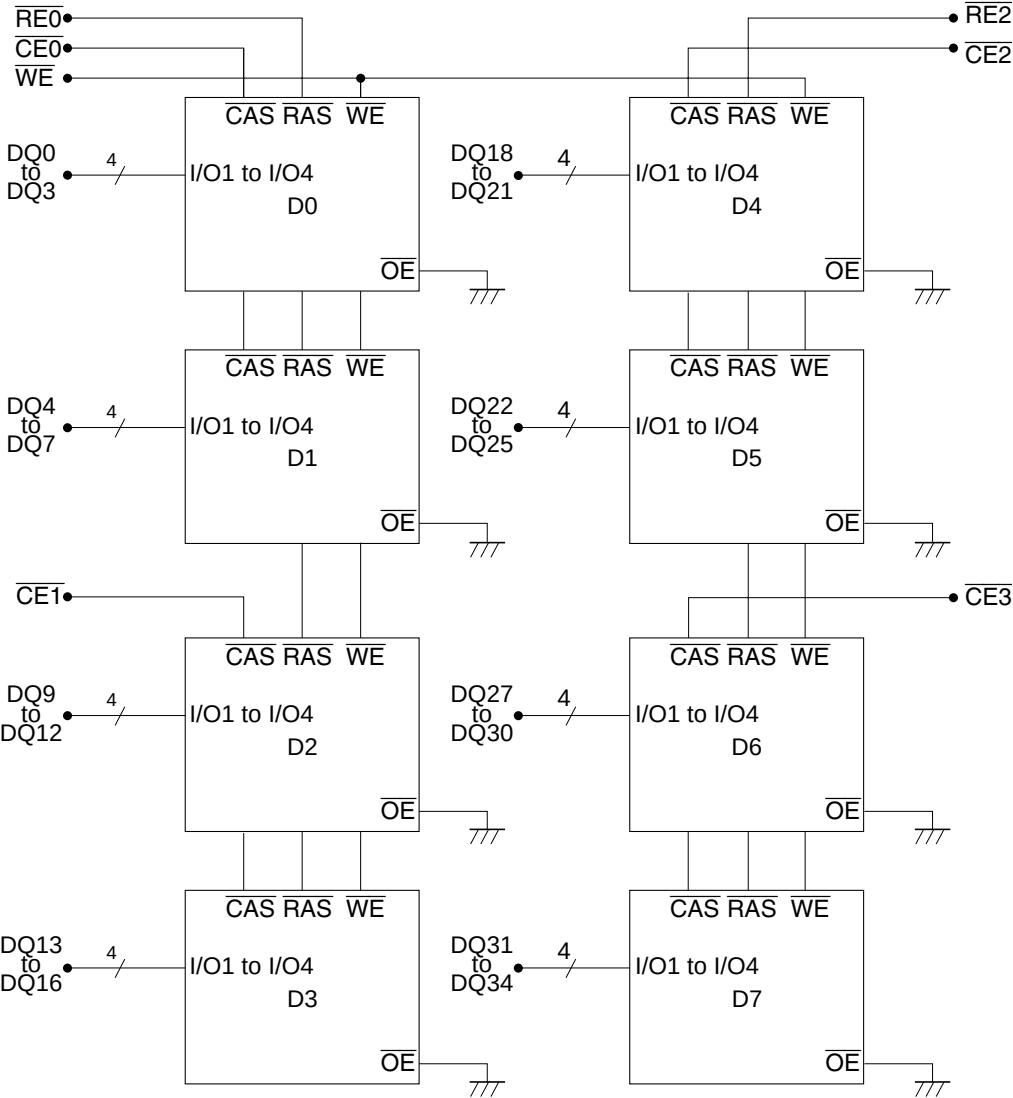
Pin Description

Pin name	Function
A0 to A11 (HB56T432D)	Address inputs: — Row address: A0 to A11 — Column address: A0 to A9 — Refresh address: A0 to A11
A0 to A10 (HB56T433D)	Address inputs: — Row address: A0 to A10 — Column address: A0 to A10 — Refresh address: A0 to A10
DQ0 to DQ7, DQ9 to DQ16, DQ18 to DQ25, DQ27 to DQ34	Data-in/Data-out
$\overline{RE0}$, $\overline{RE2}$	Row address strobe ($\overline{RAS}$)
$\overline{CE0}$ to $\overline{CE3}$	column address strobe ($\overline{CAS}$)
$\overline{WE}$	Read/Write enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD7	Presence detect
NC	No connection

Presence Detect Pin Arrangement

Pin No.	Pin name	Function		
		50 ns	60 ns	70 ns
11	PD1	NC	NC	NC
66	PD2	NC	NC	NC
67	PD3	V_{SS}	V_{SS}	V_{SS}
68	PD4	NC	NC	NC
69	PD5	V_{SS}	NC	V_{SS}
70	PD6	V_{SS}	NC	NC
71	PD7	NC	NC	NC

Block Diagram



A0 to An ● —————> D0 to D7
V_{CC} ● —————> D0 to D7
V_{SS} ● —————> D0 to D7

Note: D0 to D7: HM5116400 (HB56T432D)
HM5117400 (HB56T433D)

0.22 μF × 8 pcs

HB56T432D Series, HB56T433D Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _T	−1.0 to +7.0	V
Supply voltage relative to V _{SS}	V _{CC}	−1.0 to +7.0	V
Short circuit output current	I _{out}	50	mA
Power dissipation	P _t	8	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V _{SS}	0	0	0	V	
	V _{CC}	4.75	5.0	5.25	V	1
Input high voltage	V _{IH}	2.4	—	5.5	V	1
Input low voltage	V _{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56T432D)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	720	—	640	—	560	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	16	—	16	—	16	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z	
Standby current (L-version)	I _{CC2}	—	1.2	—	1.2	—	1.2	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	720	—	640	—	560	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	40	—	40	—	40	mA	RAS = V _{IH} , CAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	720	—	640	—	560	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	640	—	560	—	480	mA	t _{PC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I _{CC10}	—	2.8	—	2.8	—	2.8	mA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 31.3 μs t _{RAS} ≤ 0.3 μs	
Input leakage current	I _{LI}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I _{LO}	−10	10	−10	10	−10	10	μA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Address can be changed once or less while CAS = V_{IH}.

HB56T432D Series, HB56T433D Series

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) (HB56T433D)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	800	—	720	—	640	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	16	—	16	—	16	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z	
Standby current (L-version)	I _{CC2}	—	1.2	—	1.2	—	1.2	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	800	—	720	—	640	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	40	—	40	—	40	mA	RAS = V _{IH} , CAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	800	—	720	—	640	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	720	—	640	—	560	mA	t _{PC} = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I _{CC10}	—	2.8	—	2.8	—	2.8	mA	CMOS interface Dout = High-Z CBR refresh: t _{RC} = 62.5 μs t _{RAS} ≤ 0.3 μs	
Input leakage current	I _{LI}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I _{LO}	−10	10	−10	10	−10	10	μA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Address can be changed once or less while CAS = V_{IH}.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	68	pF	1
Input capacitance ($\overline{\text{WE}}$)	C_{I2}	—	76	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C_{I3}	—	29	pF	1
Input capacitance ($\overline{\text{RAS}}$)	C_{I4}	—	43	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

AC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$) ^{*1, *2, *17}
Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.4 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

HB56T432D Series, HB56T433D Series

Read, Write, and Refresh Cycles (Common parameters)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90	—	110	—	130	—	ns	
RAS precharge time	t _{RP}	30	—	40	—	50	—	ns	
CAS precharge time	t _{CP}	7	—	10	—	10	—	ns	
RAS pulse width	t _{RAS}	50	10000	60	10000	70	10000	ns	
CAS pulse width	t _{CAS}	13	10000	15	10000	18	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t _{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	7	—	10	—	15	—	ns	
RAS to CAS delay time	t _{RCD}	17	37	20	45	20	52	ns	3
RAS to column address delay time	t _{RAD}	12	25	15	30	15	35	ns	4
RAS hold time	t _{RSH}	13	—	15	—	18	—	ns	
CAS hold time	t _{CSH}	50	—	60	—	70	—	ns	
CAS to RAS precharge time	t _{CRP}	5	—	5	—	5	—	ns	
CAS delay time from Din	t _{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	5
Refresh period (HB56T432D: 4,096 cycles)	t _{REF}	—	64	—	64	—	64	ms	
Refresh period (HB56T432D: 4,096 cycles) (L-version)	t _{REF}	—	128	—	128	—	128	ms	
Refresh period (HB56T433D: 2,048 cycles)	t _{REF}	—	32	—	32	—	32	ms	
Refresh period (HB56T433D: 2,048 cycles) (L-version)	t _{REF}	—	128	—	128	—	128	ms	

Read Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	6, 7
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	18	ns	7, 8, 15
Access time from address	t_{AA}	—	25	—	30	—	35	ns	7, 9, 15
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	10
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	5	—	5	—	ns	10
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	25	—	30	—	35	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	11
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	

Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	12
Write command hold time	t_{WCH}	7	—	10	—	15	—	ns	
Write command pulse width	t_{WP}	7	—	10	—	10	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	13
Data-in hold time	t_{DH}	7	—	10	—	15	—	ns	13

HB56T432D Series, HB56T433D Series

Refresh Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CAS setup time (CBR refresh cycle)	t _{CSR}	5	—	5	—	5	—	ns	
CAS hold time (CBR refresh cycle)	t _{CHR}	7	—	10	—	10	—	ns	
WE setup time (CBR refresh cycle)	t _{WRP}	0	—	0	—	0	—	ns	
WE hold time (CBR refresh cycle)	t _{WRH}	7	—	10	—	10	—	ns	
RAS precharge to CAS hold time	t _{RPC}	5	—	5	—	5	—	ns	

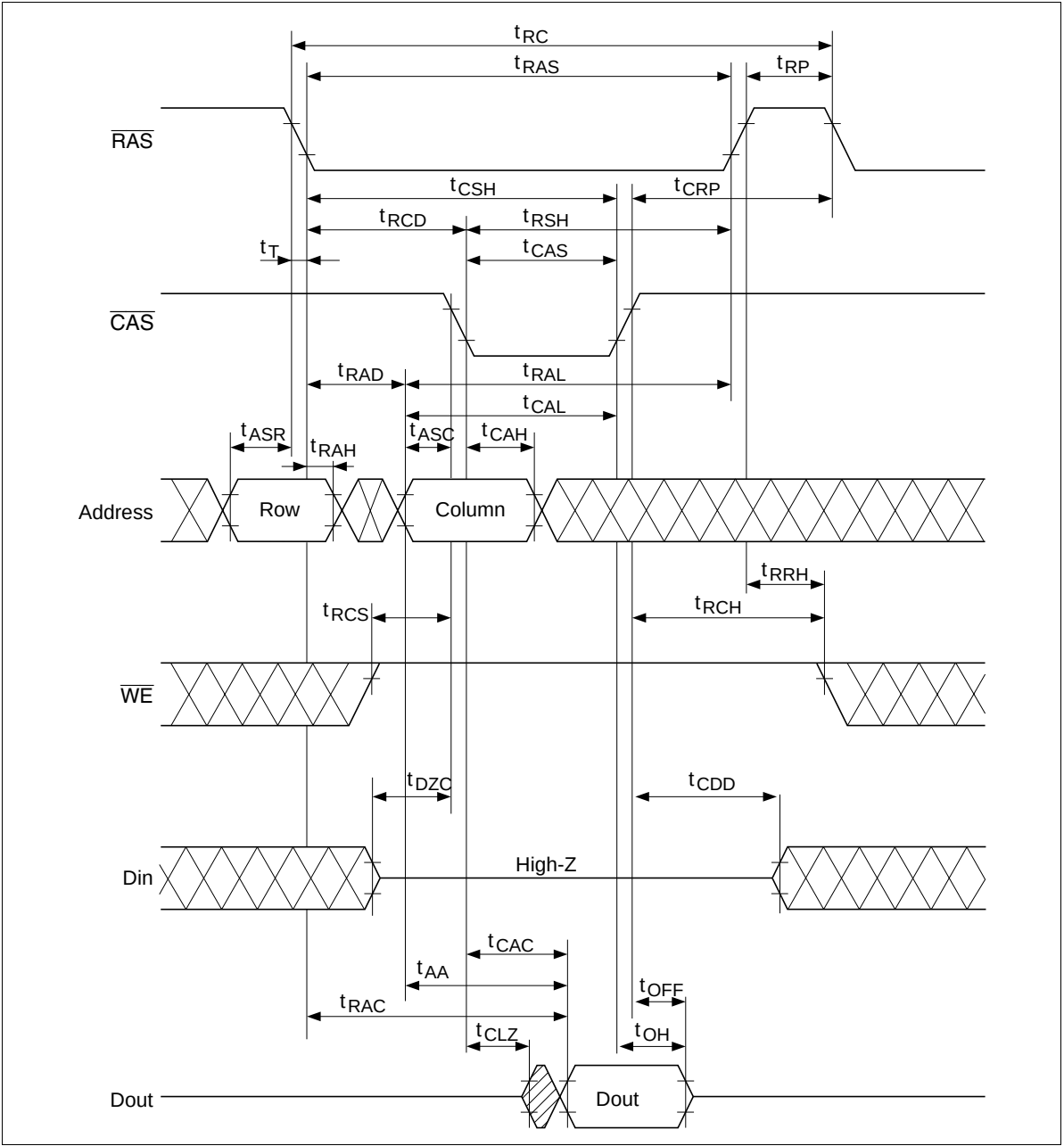
Fast Page Mode Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t _{PC}	35	—	40	—	45	—	ns	
Fast page mode RAS pulse width	t _{RASP}	—	100000	—	100000	—	100000	ns	14
Access time from CAS precharge	t _{CPA}	—	30	—	35	—	40	ns	7, 15
RAS hold time from CAS precharge	t _{CPRH}	30	—	35	—	40	—	ns	

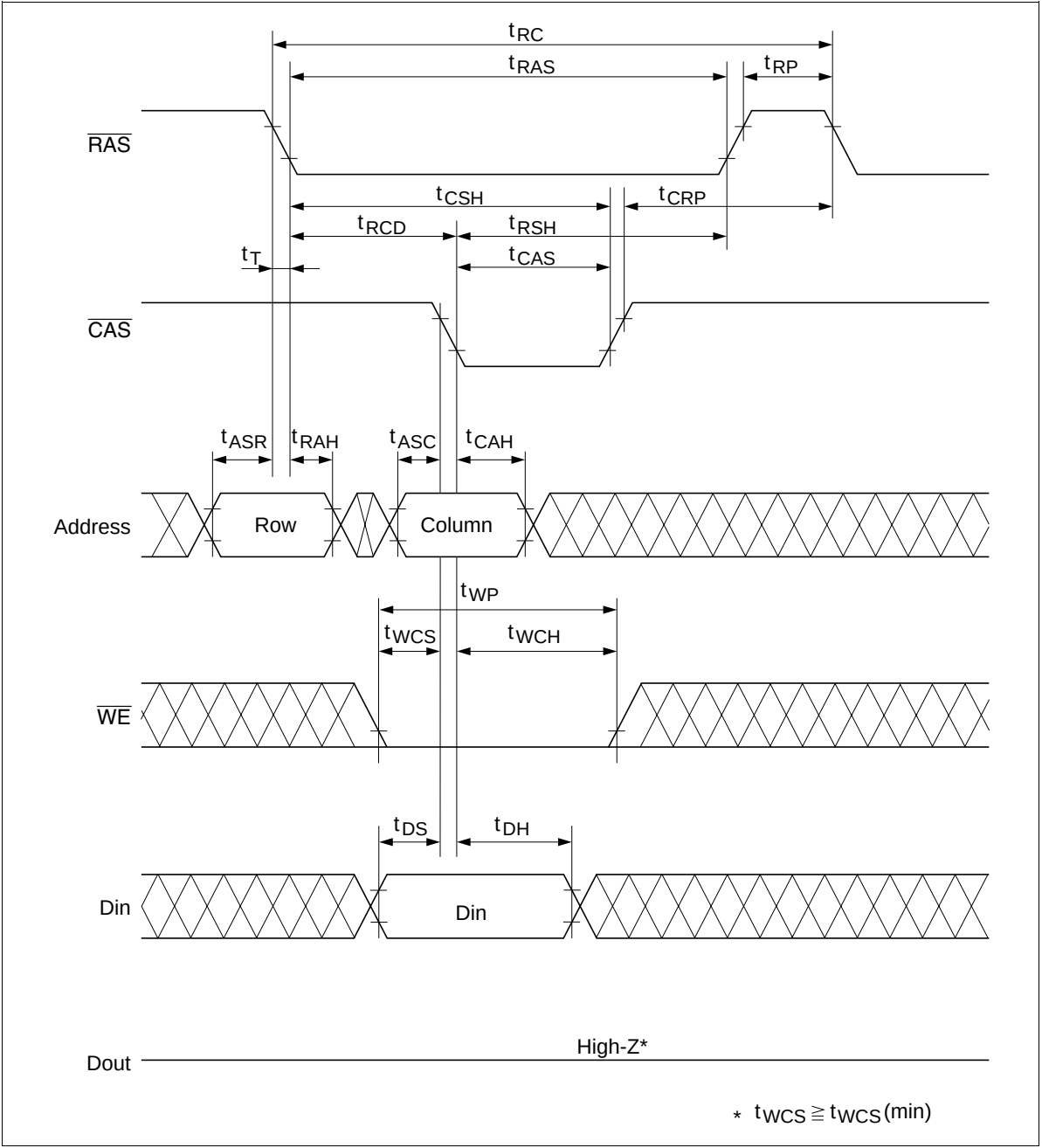
- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh cycle or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 6. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}$ (max) and $t_{\text{RAD}} \leq t_{\text{RAD}}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 7. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 8. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\geq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 9. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max) and $t_{\text{RCD}} + t_{\text{CAC}}$ (max) $\leq t_{\text{RAD}} + t_{\text{AA}}$ (max).
 10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 11. t_{OFF} (max) defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 12. Early write cycle only ($t_{\text{WCS}} \geq t_{\text{WCS}}$ (min)).
 13. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles.
 14. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in Fast page mode cycles.
 15. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 16. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}} / V_{\text{SS}}$ line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
 17. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 18. XXX: H or L (H: V_{IH} (min) $\leq V_{\text{IN}} \leq V_{\text{IH}}$ (max), L: V_{IL} (min) $\leq V_{\text{IN}} \leq V_{\text{IL}}$ (max))
 //////////////: Invalid Dout
 When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Timing Waveforms*18

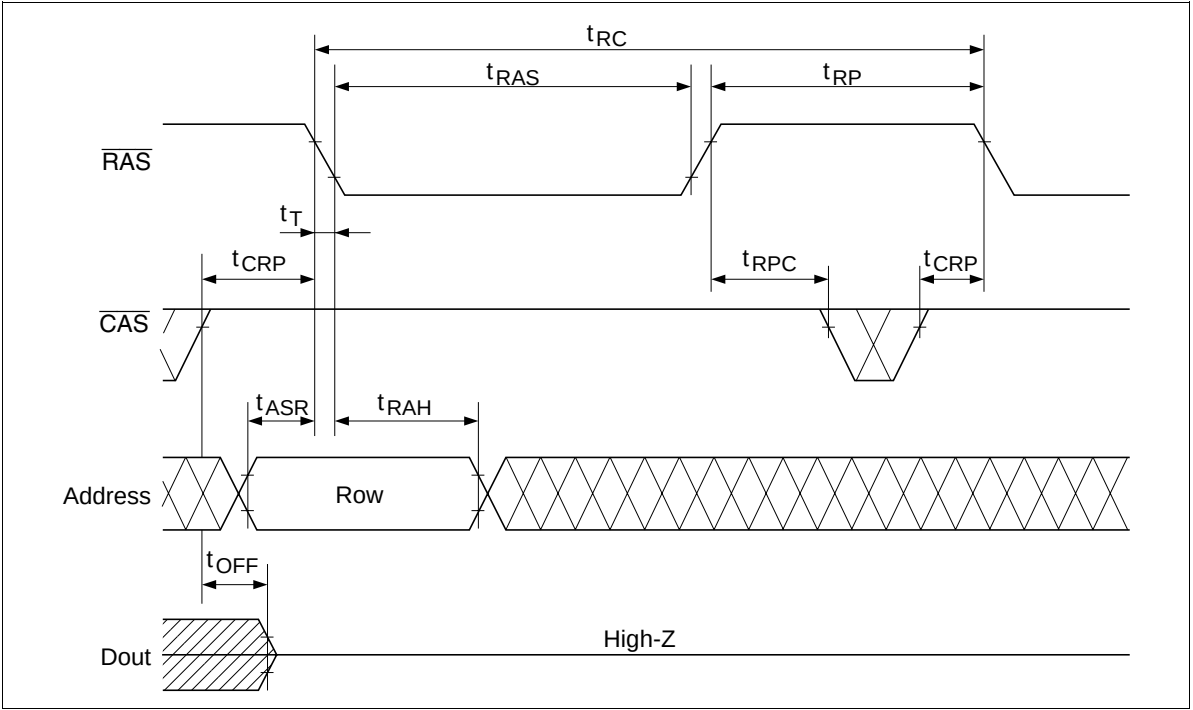
Read Cycle



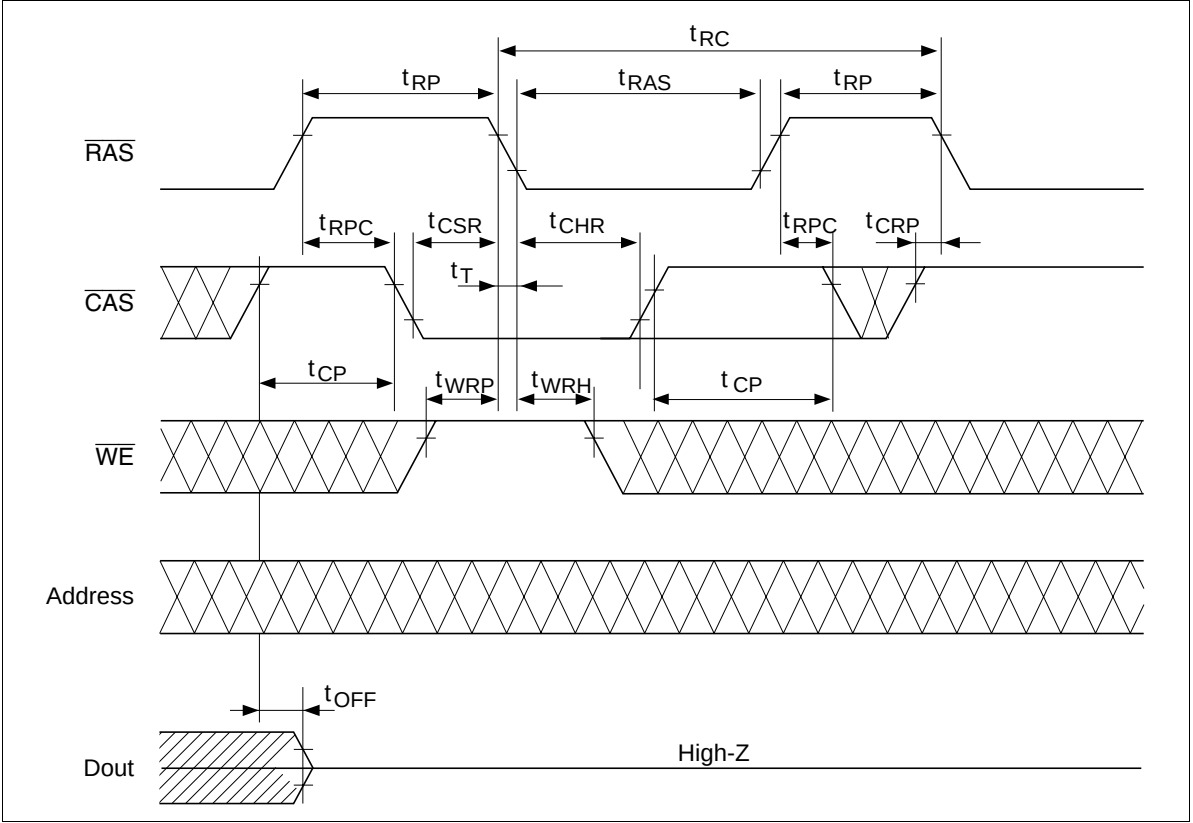
Early Write Cycle



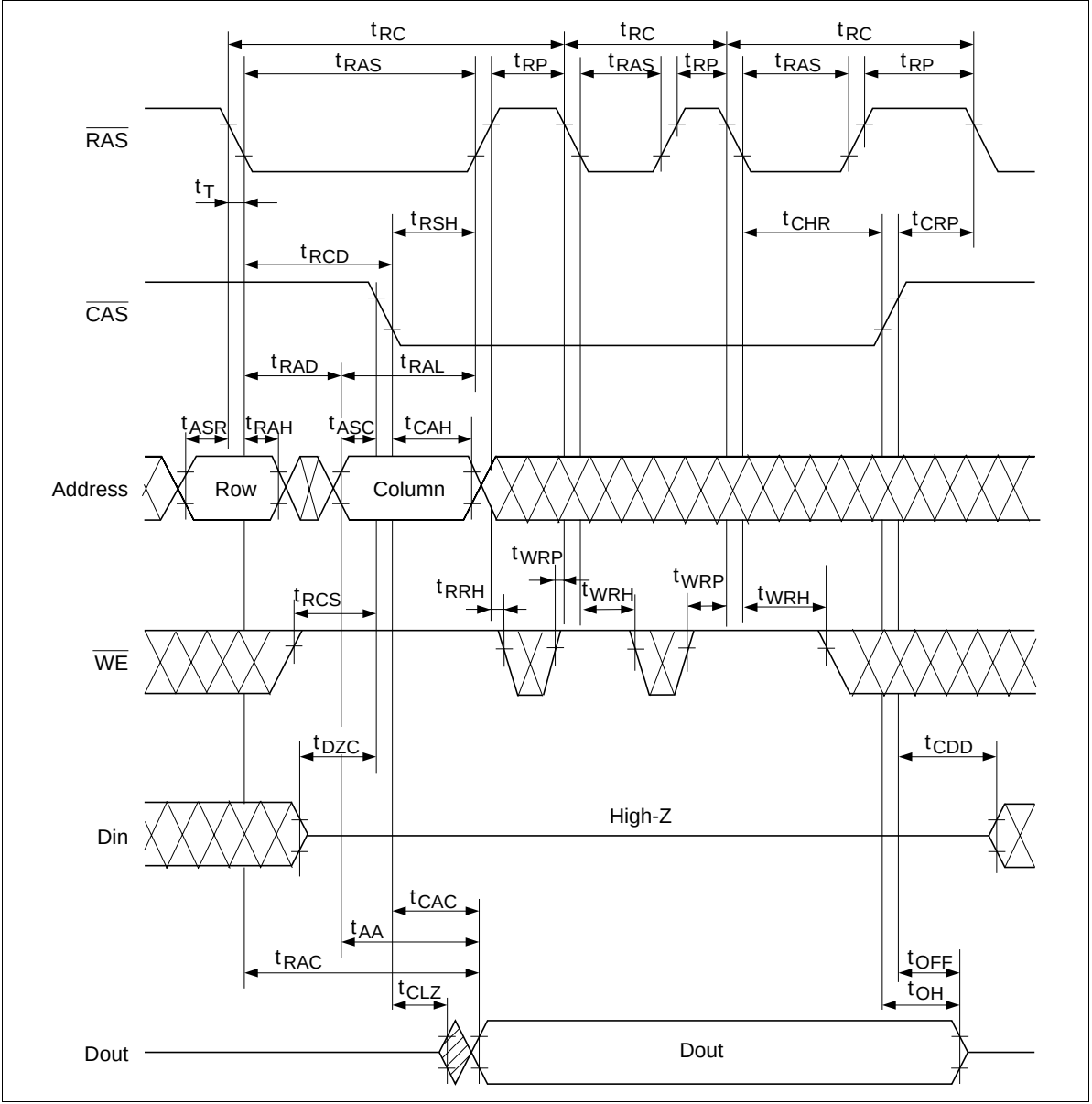
RAS-Only Refresh Cycle



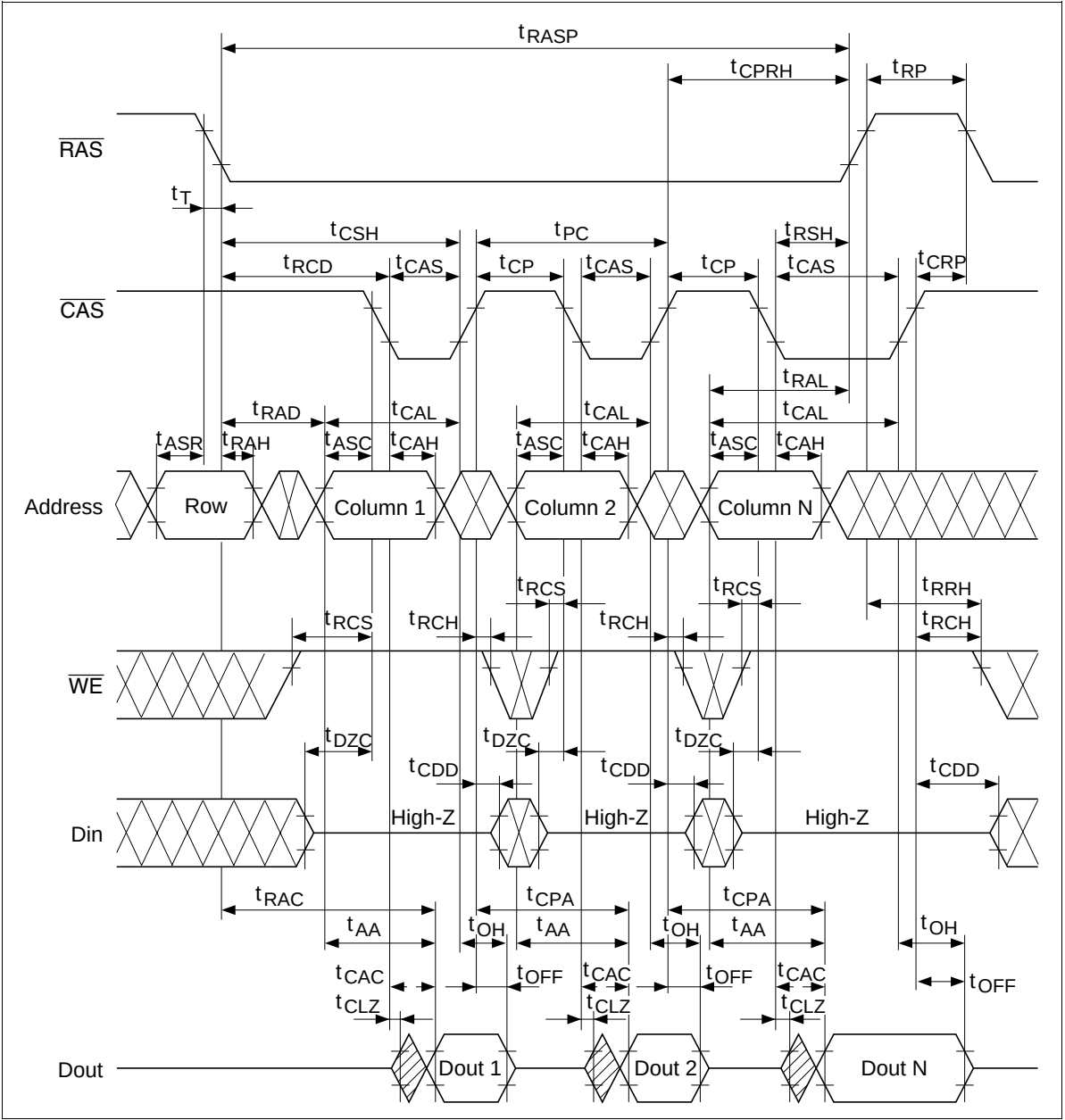
CAS-Before-RAS Refresh Cycle



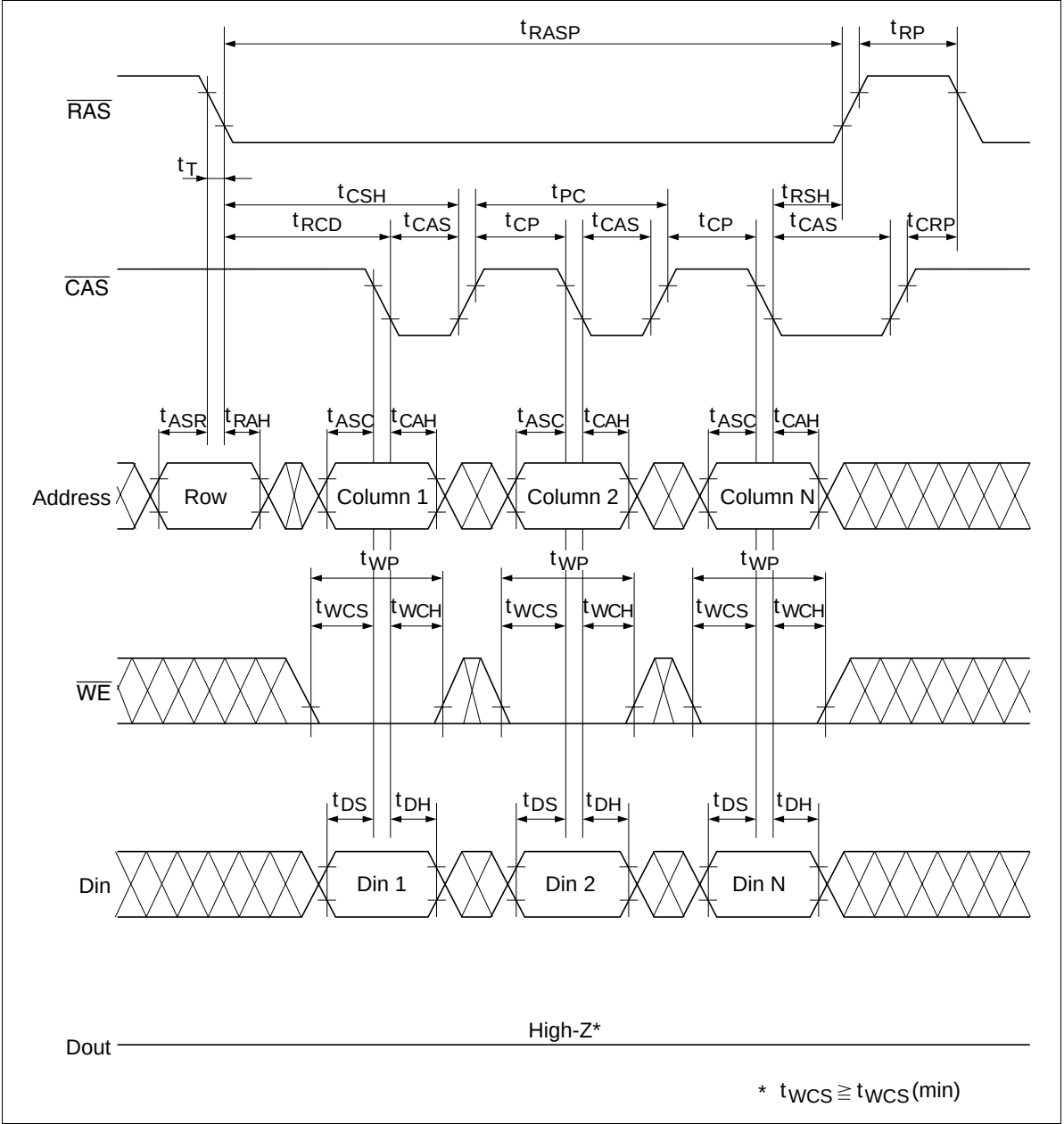
Hidden Refresh Cycle



Fast Page Mode Read Cycle

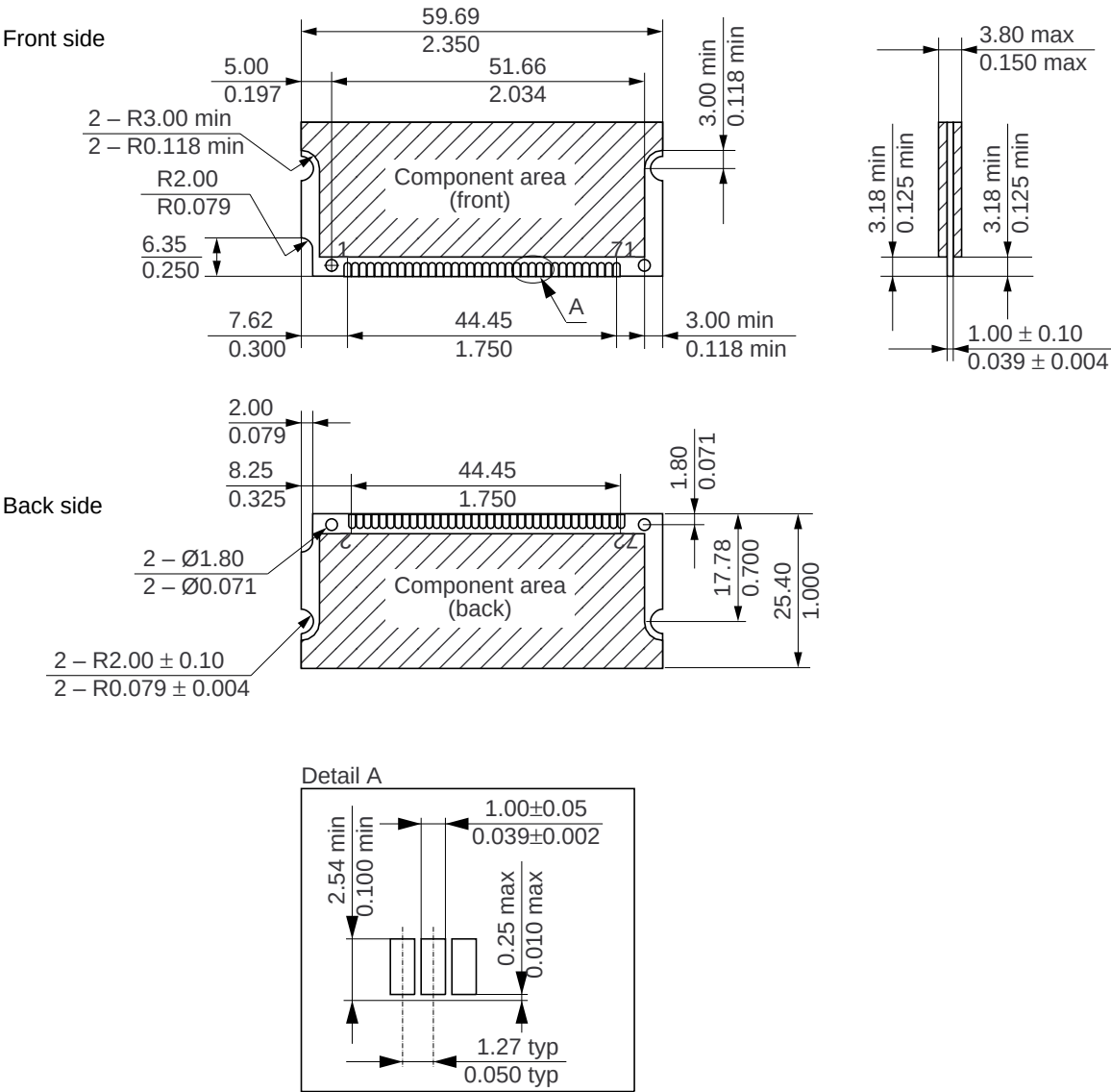


Fast Page Mode Early Write Cycle



Physical Outline

Unit : $\frac{\text{mm}}{\text{inch}}$



When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Feb. 27, 1997	Initial issue		
