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# HB56HW164DB Series, HB56HW165DB Series

1,048,576-word × 64-bit High Density Dynamic RAM Module

# HITACHI

ADE-203-699A (Z)

Rev.1.0

Dec. 27, 1996

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## Description

The HB56HW164DB is a 1M × 64 dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 4 pieces of 16-Mbit DRAM (HM51W16165) sealed in TSOP package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56HW165DB is a 1M × 64 dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 4 pieces of 16-Mbit DRAM (HM51W18165) sealed in TSOP package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56HW164DB, HB56HW165DB offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56HW164DB, HB56HW165DB is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB56HW164DB, HB56HW165DB make high density mounting possible without surface mount technology. The HB56HW164DB, HB56HW165DB provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

## Features

- 144-pin Zig Zag Dual tabs socket type
  - Outline: 67.60 mm (Length) × 25.40 mm (Height) × 3.80 mm (Thickness)
  - Lead pitch: 0.80 mm
- Single 3.3 V (±0.3 V) supply
- High speed
  - Access time:  $t_{\text{RAC}} = 60/70$  ns (max)  
 $t_{\text{CAC}} = 15/18$  ns (max)
- Low power dissipation
  - Active mode: 1.44/1.30 W (max) (HB56HW164DB Series)  
2.45/2.16 W (max) (HB56HW165DB Series)
  - Standby mode (TTL): 28.8 mW (max)  
(CMOS): 2.16 mW (max) (L-version)
- EDO page mode capability

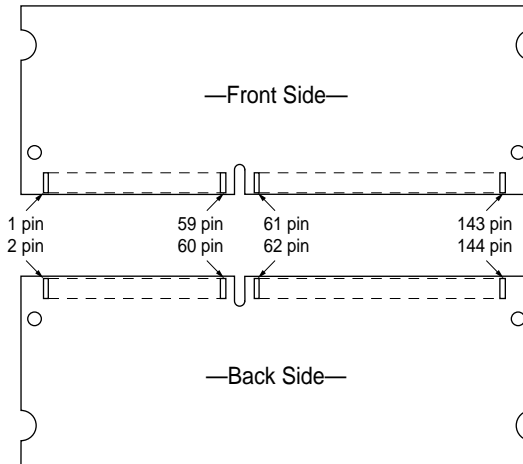
# HB56HW164DB Series, HB56HW165DB Series

- Refresh period
  - 4096 refresh cycles: 64 ms (HB56HW164DB Series)  
128 ms (L-version)
  - 1024 refresh cycles: 16 ms (HB56HW165DB Series)  
128 ms (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$ -only refresh
  - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh
  - Hidden refresh
  - Self refresh (L-version)

## Ordering Information

Type No.	Access time	Package	Contact pad
HB56HW164DB-6	60 ns	144-pin small outline DIMM	Gold
HB56HW164DB-7	70 ns		
HB56HW164DB-6L	60 ns		
HB56HW164DB-7L	70 ns		
HB56HW165DB-6	60 ns		
HB56HW165DB-7	70 ns		
HB56HW165DB-6L	60 ns		
HB56HW165DB-7L	70 ns		

## Pin Arrangement



# HB56HW164DB Series, HB56HW165DB Series

## Pin Arrangement

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V <sub>SS</sub>	73	$\overline{OE}$	2	V <sub>SS</sub>	74	NC
3	DQ0	75	V <sub>SS</sub>	4	DQ32	76	V <sub>SS</sub>
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	V <sub>CC</sub>	10	DQ35	82	V <sub>CC</sub>
11	V <sub>CC</sub>	83	DQ16	12	V <sub>CC</sub>	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	V <sub>SS</sub>	20	DQ39	92	V <sub>SS</sub>
21	V <sub>SS</sub>	93	DQ20	22	V <sub>SS</sub>	94	DQ52
23	$\overline{CE0}$	95	DQ21	24	$\overline{CE4}$	96	DQ53
25	$\overline{CE1}$	97	DQ22	26	$\overline{CE5}$	98	DQ54
27	V <sub>CC</sub>	99	DQ23	28	V <sub>CC</sub>	100	DQ55
29	A0	101	V <sub>CC</sub>	30	A3	102	V <sub>CC</sub>
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	A11 (NC)*2
35	V <sub>SS</sub>	107	V <sub>SS</sub>	36	V <sub>SS</sub>	108	V <sub>SS</sub>
37	DQ8	109	A9	38	DQ40	110	NC
39	DQ9	111	A10 (NC)*1	40	DQ41	112	NC
41	DQ10	113	V <sub>CC</sub>	42	DQ42	114	V <sub>CC</sub>
43	DQ11	115	$\overline{CE2}$	44	DQ43	116	$\overline{CE6}$
45	V <sub>CC</sub>	117	$\overline{CE3}$	46	V <sub>CC</sub>	118	$\overline{CE7}$
47	DQ12	119	V <sub>SS</sub>	48	DQ44	120	V <sub>SS</sub>
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V <sub>SS</sub>	127	DQ27	56	V <sub>SS</sub>	128	DQ59
57	NC	129	V <sub>CC</sub>	58	NC	130	V <sub>CC</sub>
59	NC	131	DQ28	60	NC	132	DQ60
61	NC	133	DQ29	62	NC	134	DQ61
63	V <sub>CC</sub>	135	DQ30	64	V <sub>CC</sub>	136	DQ62
65	NC	137	DQ31	66	NC	138	DQ63

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## Pin Arrangement (cont)

Front side				Back side			
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
67	$\overline{WE}$	139	$V_{SS}$	68	NC	140	$V_{SS}$
69	$\overline{RE0}$	141	SDA	70	NC	142	SCL
71	NC	143	$V_{CC}$	72	NC	144	$V_{CC}$

Notes: 1. A10: HB56HW164DB, NC: HB56HW165DB  
2. A11: HB56HW164DB, NC: HB56HW165DB

## Pin Description

Pin name	Function
A0 to A11 (HB56HW164DB)	Address inputs: <ul style="list-style-type: none"><li>— Row address: A0 to A11</li><li>— Column address: A0 to A7</li><li>— Refresh address: A0 to A11</li></ul>
A0 to A9 (HB56HW165DB)	Address inputs: <ul style="list-style-type: none"><li>— Row address: A0 to A9</li><li>— Column address: A0 to A9</li><li>— Refresh address: A0 to A9</li></ul>
DQ0 to DQ63	Data-in/Data-out
$\overline{RE0}$	Row address strobe ( $\overline{RAS}$ )
$\overline{CE0}$ to $\overline{CE7}$	column address strobe ( $\overline{CAS}$ )
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
$V_{CC}$	Power supply
$V_{SS}$	Ground
SDA	Serial data for PD
SCL	Serial clock for PD
NC	No connection

# HB56HW164DB Series, HB56HW165DB Series

## Serial PD Matrix (HB56HW164DB)\*<sup>1</sup>

Byte number	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comments
0	Number serial PD bytes	0	0	0	0	1	1	0	1	13
1	Serial memory	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type	0	0	0	0	0	0	1	0	EDO
3	Number of rows	0	0	0	0	1	1	0	0	12
4	Number of columns	0	0	0	0	1	0	0	0	8
5	Number of banks	0	0	0	0	0	0	0	1	1
6	Data width	0	1	0	0	0	0	0	0	64
7	Data width (continued)	0	0	0	0	0	0	0	0	0 (+)
8	Voltage interface	0	0	0	0	0	0	0	1	LVTTL (3.3V)
9	$\overline{\text{RAS}}$ access time									
	60 ns	0	0	1	1	1	1	0	0	
	70 ns	0	1	0	0	0	1	1	0	
10	$\overline{\text{CAS}}$ access time									
	15 ns	0	0	0	0	1	1	1	1	
	18 ns	0	0	0	1	0	0	1	0	
11	Error detection/correction	0	0	0	0	0	0	0	0	None
12	Refresh period	0	0	0	0	0	0	0	0	Normal (15.625 $\mu\text{s}$ )
	Refresh period (L-version)	1	0	0	0	0	0	1	1	Self refresh (31.3 $\mu\text{s}$ )

Note: 1. Serial-PD data are not protected.

1: High level (serial data)

0: Low level (serial data)

# HB56HW164DB Series, HB56HW165DB Series

## Serial PD Matrix (HB56HW165DB)\*<sup>1</sup>

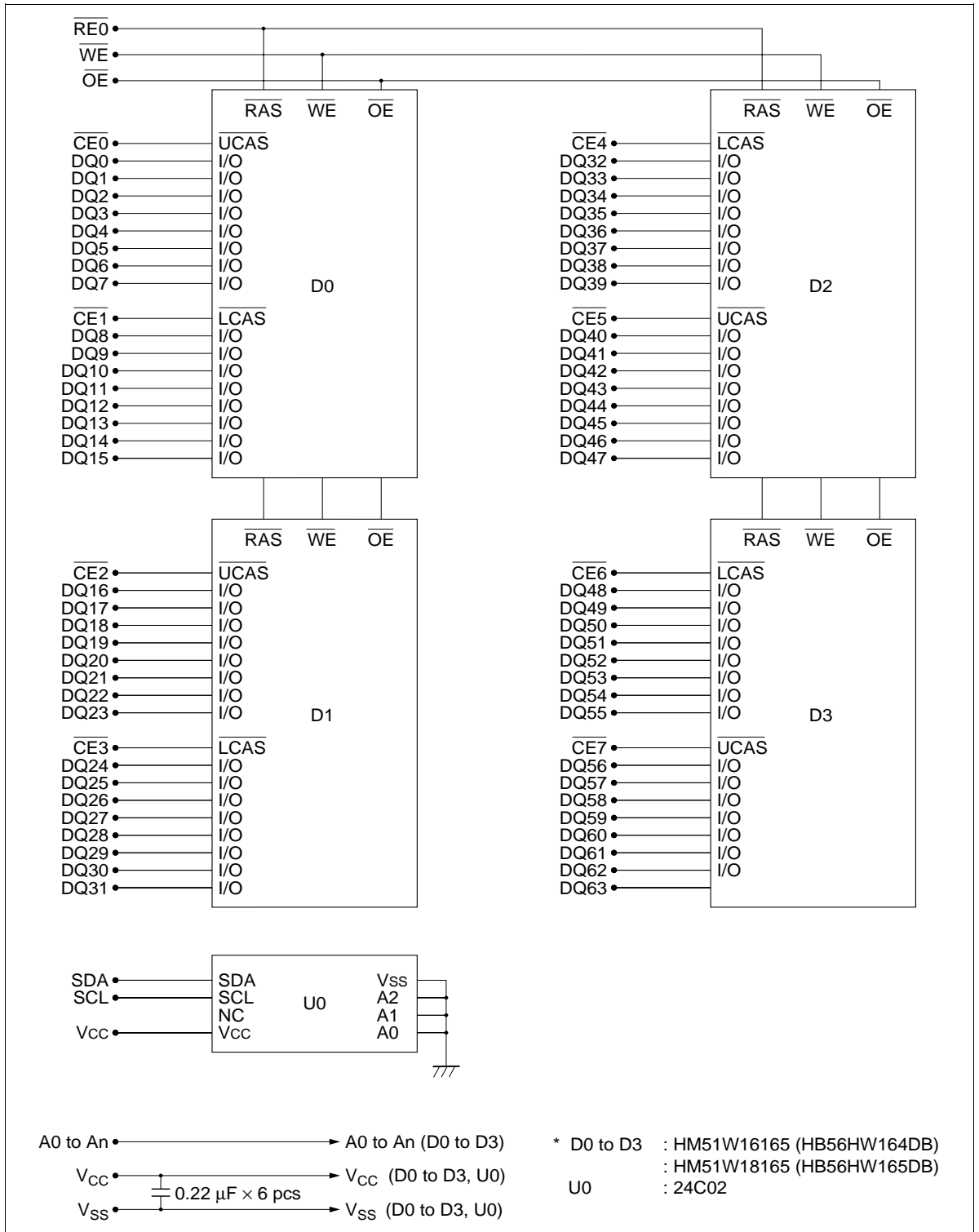
Byte number	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comments
0	Number serial PD bytes	0	0	0	0	1	1	0	1	13
1	Serial memory	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type	0	0	0	0	0	0	1	0	EDO
3	Number of rows	0	0	0	0	1	0	1	0	10
4	Number of columns	0	0	0	0	1	0	1	0	10
5	Number of banks	0	0	0	0	0	0	0	1	1
6	Data width	0	1	0	0	0	0	0	0	64
7	Data width (continued)	0	0	0	0	0	0	0	0	0 (+)
8	Voltage interface	0	0	0	0	0	0	0	1	LVTTL (3.3V)
9	$\overline{\text{RAS}}$ access time									
	60 ns	0	0	1	1	1	1	0	0	
	70 ns	0	1	0	0	0	1	1	0	
10	$\overline{\text{CAS}}$ access time									
	15 ns	0	0	0	0	1	1	1	1	
	18 ns	0	0	0	1	0	0	1	0	
11	Error detection/correction	0	0	0	0	0	0	0	0	None
12	Refresh period	0	0	0	0	0	0	0	0	Normal (15.625 $\mu\text{s}$ )
	Refresh period (L-version)	1	0	0	0	0	1	0	1	Self refresh (125 $\mu\text{s}$ )

Note: 1. Serial-PD data are not protected.

1: High level (serial data)

0: Low level (serial data)

## Block Diagram



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## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 to +4.6	V
Supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +4.6	V
Short circuit output current	$I_{out}$	50	mA
Power dissipation	$P_t$	4	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

## Recommended DC Operating Conditions ( $T_a = 0$ to $70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{SS}$	0	0	0	V	
	$V_{CC}$	3.0	3.3	3.6	V	1
Input high voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	$V_{IL}$	-0.3	—	0.8	V	1

Note: 1. All voltage referred to  $V_{SS}$ .

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**DC Characteristics** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ) (HB56HW164DB)

Parameter	Symbol	60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	$I_{CC1}$	—	400	—	360	mA	$t_{RC} = \text{min}$	1, 2
Standby current	$I_{CC2}$	—	8	—	8	mA	TTL interface $\overline{\text{RAS}}, \overline{\text{CAS}} = V_{IH}$ Dout = High-Z	
		—	4	—	4	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
Standby current (L-version)	$I_{CC2}$	—	0.6	—	0.6	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
$\overline{\text{RAS}}$ -only refresh current	$I_{CC3}$	—	400	—	360	mA	$t_{RC} = \text{min}$	2
Standby current	$I_{CC5}$	—	20	—	20	mA	$\overline{\text{RAS}} = V_{IH}$ , $\overline{\text{CAS}} = V_{IL}$ Dout = enable	1
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	$I_{CC6}$	—	400	—	360	mA	$t_{RC} = \text{min}$	
EDO page mode current	$I_{CC7}$	—	520	—	460	mA	$t_{HPC} = \text{min}$	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	$I_{CC10}$	—	1.6	—	1.6	mA	CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 31.3 \mu\text{s}$ $t_{RAS} \leq 0.3 \mu\text{s}$	4
Self refresh mode current (L-version)	$I_{CC11}$	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \leq 0.2 \text{ V}$ Dout = High-Z	
Input leakage current	$I_{LI}$	-10	10	-10	10	$\mu\text{A}$	$0 \text{ V} \leq V_{in} \leq 4.6 \text{ V}$	
Output leakage current	$I_{LO}$	-10	10	-10	10	$\mu\text{A}$	$0 \text{ V} \leq V_{out} \leq 4.6 \text{ V}$ Dout = disable	
Output high voltage	$V_{OH}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	High Iout = -2 mA	
Output low voltage	$V_{OL}$	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1.  $I_{CC}$  depends on output load condition when the device is selected,  $I_{CC}$  max is specified at the output open condition.

2. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .

4.  $V_{IH} \geq V_{CC} - 0.2 \text{ V}$ ,  $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$

# HB56HW164DB Series, HB56HW165DB Series

DC Characteristics (Ta = 0 to 70°C, V<sub>CC</sub> = 3.3 V ± 0.3V, V<sub>SS</sub> = 0 V) (HB56HW165DB)

Parameter	Symbol	60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I <sub>CC1</sub>	—	680	—	600	mA	t <sub>RC</sub> = min	1, 2
Standby current	I <sub>CC2</sub>	—	8	—	8	mA	TTL interface RAS, CAS = V <sub>IH</sub> Dout = High-Z	
		—	4	—	4	mA	CMOS interface RAS, CAS ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z	
Standby current (L-version)	I <sub>CC2</sub>	—	0.6	—	0.6	mA	CMOS interface RAS, CAS ≥ V <sub>CC</sub> - 0.2 V Dout = High-Z	
RAS-only refresh current	I <sub>CC3</sub>	—	680	—	600	mA	t <sub>RC</sub> = min	2
Standby current	I <sub>CC5</sub>	—	20	—	20	mA	RAS = V <sub>IH</sub> , CAS = V <sub>IL</sub> Dout = enable	1
CAS-before-RAS refresh current	I <sub>CC6</sub>	—	680	—	600	mA	t <sub>RC</sub> = min	
EDO page mode current	I <sub>CC7</sub>	—	740	—	660	mA	t <sub>HPC</sub> = min	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I <sub>CC10</sub>	—	1.6	—	1.6	mA	CMOS interface Dout = High-Z CBR refresh: t <sub>RC</sub> = 125 μs t <sub>RAS</sub> ≤ 0.3 μs	4
Self refresh mode current (L-version)	I <sub>CC11</sub>	—	1	—	1	mA	CMOS interface RAS, CAS ≤ 0.2 V Dout = High-Z	
Input leakage current	I <sub>LI</sub>	-10	10	-10	10	μA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I <sub>LO</sub>	-10	10	-10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V <sub>OH</sub>	2.4	V <sub>CC</sub>	2.4	V <sub>CC</sub>	V	High Iout = -2 mA	
Output low voltage	V <sub>OL</sub>	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I<sub>CC</sub> depends on output load condition when the device is selected, I<sub>CC</sub> max is specified at the output open condition.

2. Address can be changed once or less while RAS = V<sub>IL</sub>.

3. Address can be changed once or less while CAS = V<sub>IH</sub>.

4. V<sub>IH</sub> ≥ V<sub>CC</sub> - 0.2 V, 0 V ≤ V<sub>IL</sub> ≤ 0.2 V

## HB56HW164DB Series, HB56HW165DB Series

**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ )

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	$C_{i1}$	—	40	pF	1
Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{i2}$	—	48	pF	1
Input capacitance ( $\overline{\text{CAS}}$ )	$C_{i3}$	—	22	pF	1
I/O capacitance (DQ)	$C_{i/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
2.  $\overline{\text{CAS}} = V_{IH}$  to disable Dout.

**AC Characteristics** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ) \*<sup>1</sup>, \*<sup>2</sup>, \*<sup>18</sup>, \*<sup>19</sup>

### Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate +  $C_L$  (100 pF) (Including scope and jig)

# HB56HW164DB Series, HB56HW165DB Series

## Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	$t_{RC}$	104	—	124	—	ns	
$\overline{RAS}$ precharge time	$t_{RP}$	40	—	50	—	ns	
$\overline{CAS}$ precharge time	$t_{CP}$	10	—	13	—	ns	
$\overline{RAS}$ pulse width	$t_{RAS}$	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	$t_{CAS}$	10	10000	13	10000	ns	
Row address setup time	$t_{ASR}$	0	—	0	—	ns	
Row address hold time	$t_{RAH}$	10	—	10	—	ns	
Column address setup time	$t_{ASC}$	0	—	0	—	ns	
Column address hold time	$t_{CAH}$	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$t_{RCD}$	20	45	20	52	ns	3
$\overline{RAS}$ to column address delay time	$t_{RAD}$	15	30	15	35	ns	4
$\overline{RAS}$ hold time	$t_{RSH}$	15	—	18	—	ns	
$\overline{CAS}$ hold time	$t_{CSH}$	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	$t_{CRP}$	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	$t_{OED}$	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	$t_{DZO}$	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	$t_{DZC}$	0	—	0	—	ns	6
Transition time (rise and fall)	$t_T$	2	50	2	50	ns	7
Refresh period (HB56HW164DB: 4,096 cycles)	$t_{REF}$	—	64	—	64	ms	
Refresh period (HB56HW164DB: 4,096 cycles) (L-version)	$t_{REF}$	—	128	—	128	ms	
Refresh period (HB56HW165DB: 1,024 cycles)	$t_{REF}$	—	16	—	16	ms	
Refresh period (HB56HW165DB: 1,024 cycles) (L-version)	$t_{REF}$	—	128	—	128	ms	

# HB56HW164DB Series, HB56HW165DB Series

## Read Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	$t_{\text{RAC}}$	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	$t_{\text{CAC}}$	—	15	—	18	ns	9, 10, 17
Access time from address	$t_{\text{AA}}$	—	30	—	35	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	$t_{\text{OEA}}$	—	15	—	18	ns	9, 21
Read command setup time	$t_{\text{RCS}}$	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	$t_{\text{RCH}}$	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	$t_{\text{RCHR}}$	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	$t_{\text{RRH}}$	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	$t_{\text{RAL}}$	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	$t_{\text{CAL}}$	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	$t_{\text{CLZ}}$	0	—	0	—	ns	
Output data hold time	$t_{\text{OH}}$	3	—	3	—	ns	22
Output data hold time from $\overline{\text{OE}}$	$t_{\text{OHO}}$	3	—	3	—	ns	
Output buffer turn-off time	$t_{\text{OFF}}$	—	15	—	15	ns	13, 22
Output buffer turn-off to $\overline{\text{OE}}$	$t_{\text{OEZ}}$	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	$t_{\text{CDD}}$	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	$t_{\text{OHR}}$	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{\text{RAS}}$	$t_{\text{OFR}}$	—	15	—	15	ns	22
Output buffer turn-off to $\overline{\text{WE}}$	$t_{\text{WEZ}}$	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	$t_{\text{WED}}$	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	$t_{\text{RDD}}$	15	—	18	—	ns	
$\overline{\text{RAS}}$ next $\overline{\text{CAS}}$ delay time	$t_{\text{RNCD}}$	60	—	70	—	ns	

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## Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	$t_{WCS}$	0	—	0	—	ns	14
Write command hold time	$t_{WCH}$	10	—	13	—	ns	
Write command pulse width	$t_{WP}$	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	$t_{RWL}$	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	$t_{CWL}$	10	—	13	—	ns	
Data-in setup time	$t_{DS}$	0	—	0	—	ns	15
Data-in hold time	$t_{DH}$	10	—	13	—	ns	15

## Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
Read-modify-write cycle time	$t_{RWC}$	136	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	$t_{RWD}$	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	$t_{CWD}$	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	$t_{AWD}$	49	—	57	—	ns	14
$\overline{OE}$ hold time $\overline{WE}$	$t_{OEH}$	15	—	18	—	ns	

## Refresh Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	$t_{CSR}$	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	$t_{CHR}$	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	$t_{RPC}$	0	—	0	—	ns	

# HB56HW164DB Series, HB56HW165DB Series

## EDO Page Mode Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode cycle time	$t_{HPC}$	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	$t_{RASP}$	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	$t_{CPA}$	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	$t_{CPRH}$	35	—	40	—	ns	
Output data hole time from $\overline{CAS}$ low	$t_{DOH}$	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time referred $\overline{OE}$	$t_{COL}$	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	$t_{COP}$	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	$t_{RCHC}$	35	—	40	—	ns	

## EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	$t_{HPRWC}$	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	$t_{CPW}$	54	—	62	—	ns	14

## Self Refresh Mode (L-version)

Parameter	Symbol	60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max		
$\overline{RAS}$ pulse width (Self refresh)	$t_{RASS}$	100	—	100	—	$\mu$ s	
$\overline{RAS}$ precharge time (Self refresh)	$t_{RPS}$	110	—	130	—	ns	
$\overline{CAS}$ hold time (Self refresh)	$t_{CHS}$	-50	—	-50	—	ns	

# HB56HW164DB Series, HB56HW165DB Series

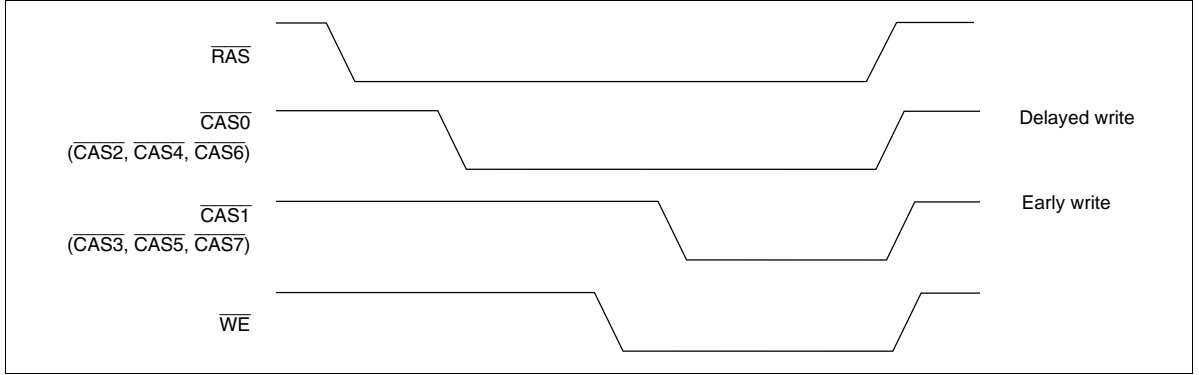
- Notes:
1. AC measurements assume  $t_T = 2 \text{ ns}$ .
  2. An initial pause of  $200 \mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$ -only refresh cycle or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles are required.
  3. Operation with the  $t_{\text{RCD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RCD}}$  (max) is specified as a reference point only; if  $t_{\text{RCD}} \geq t_{\text{RAD}} \text{ (max)} + t_{\text{AA}} \text{ (max)} - t_{\text{CAC}} \text{ (max)}$ , then access time is controlled exclusively by  $t_{\text{CAC}}$ .
  4. Operation with the  $t_{\text{RAD}}$  (max) limit insures that  $t_{\text{RAC}}$  (max) can be met,  $t_{\text{RAD}}$  (max) is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}$  (max) limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
  5. Either  $t_{\text{OED}}$  or  $t_{\text{CDD}}$  must be satisfied.
  6. Either  $t_{\text{DZO}}$  or  $t_{\text{DZC}}$  must be satisfied.
  7.  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}$  (min) and  $V_{\text{IL}}$  (max).
  8. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}} \text{ (max)}$  and  $t_{\text{RAD}} \leq t_{\text{RAD}} \text{ (max)}$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
  9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
  10. Assumes that  $t_{\text{RCD}} \geq t_{\text{RCD}} \text{ (max)}$  and  $t_{\text{RCD}} + t_{\text{CAC}} \text{ (max)} \geq t_{\text{RAD}} + t_{\text{AA}} \text{ (max)}$ .
  11. Assumes that  $t_{\text{RAD}} \geq t_{\text{RAD}} \text{ (max)}$  and  $t_{\text{RCD}} + t_{\text{CAC}} \text{ (max)} \leq t_{\text{RAD}} + t_{\text{AA}} \text{ (max)}$ .
  12. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
  13.  $t_{\text{OFF}} \text{ (max)}$  and  $t_{\text{OEZ}} \text{ (max)}$  define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
  14.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$ , and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}} \text{ (min)}$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{RWD}} \geq t_{\text{RWD}} \text{ (min)}$ ,  $t_{\text{CWD}} \geq t_{\text{CWD}} \text{ (min)}$ , and  $t_{\text{AWD}} \geq t_{\text{AWD}} \text{ (min)}$  or  $t_{\text{CWD}} \geq t_{\text{CWD}} \text{ (min)}$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}} \text{ (min)}$  and  $t_{\text{CPW}} \geq t_{\text{CPW}} \text{ (min)}$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
  15. These parameters are referred to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in delayed write or read-modify-write cycles.
  16.  $t_{\text{RASP}}$  defines  $\overline{\text{RAS}}$  pulse width in EDO page mode cycles.
  17. Access time is determined by the longest among  $t_{\text{AA}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{CPA}}$ .
  18. In delayed write or read-modify-write cycles,  $\overline{\text{OE}}$  must disable output buffer prior to applying data to the device. After  $\overline{\text{RAS}}$  is reset, if  $t_{\text{OEH}} \geq t_{\text{CWL}}$ , the DQ pin will remain open circuit (high impedance);  $t_{\text{OEH}} < t_{\text{OEH}}$ , invalid data will be out at each DQ.
  19. All the  $V_{\text{CC}}$  and  $V_{\text{SS}}$  pins shall be supplied with the same voltages.
  20.  $t_{\text{HPC}} \text{ (min)}$  can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode  $\overline{\text{RAS}}$  cycle (EDO page mode mix cycle (1), (2)), minimum value of  $\overline{\text{CAS}}$  cycle ( $t_{\text{CAS}} + t_{\text{CP}} + 2t_T$ ) becomes greater than the specified  $t_{\text{HPC}} \text{ (min)}$  value. The value of  $\overline{\text{CAS}}$  cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
  21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large  $V_{\text{CC}} / V_{\text{SS}}$  line noise, which causes to degrade  $V_{\text{IH}} \text{ min.} / V_{\text{IL}} \text{ max.}$  level.
  22. Data output turns off and becomes high impedance from later rising edge of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . Hold time and turn off time are specified by the timing specifications of later rising edge of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  between  $t_{\text{OHR}}$  and  $t_{\text{OH}}$ , and between  $t_{\text{OFR}}$  and  $t_{\text{OFF}}$ .

23. Please do not use  $t_{\text{RASS}}$  timing,  $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$ . During this period, the device is in transition state from normal operation mode to self refresh mode. If  $t_{\text{RASS}} \geq 100 \mu\text{s}$ , then  $\overline{\text{RAS}}$  precharge time should use  $t_{\text{RPS}}$  instead of  $t_{\text{RP}}$ .
24. If you use distributed CBR refresh mode with  $15.6 \mu\text{s}$  interval in normal read/write cycle, CBR refresh should be executed within  $15.6 \mu\text{s}$  immediately after exiting from and before entering into self refresh mode.
25. If you use  $\overline{\text{RAS}}$  only refresh or CBR burst refresh mode in normal read/write cycle, 4096 or 1024 cycles (4096 cycles: HB56HW164DB Series, 1024 cycles: HB56HW165DB Series) of distributed CBR refresh with  $15.6 \mu\text{s}$  interval should be executed within 64 or 16 ms (64 ms: HB56HW164DB Series, 16 ms: HB56HW165DB Series) immediately after exiting from and before entering into the self refresh mode.
26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
27. XXX: H or L (H:  $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$ , L:  $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$ )  
/////: Invalid Dout  
When the address, clock and input pins are not described on timing waveforms, their pins must be applied  $V_{\text{IH}}$  or  $V_{\text{IL}}$ .

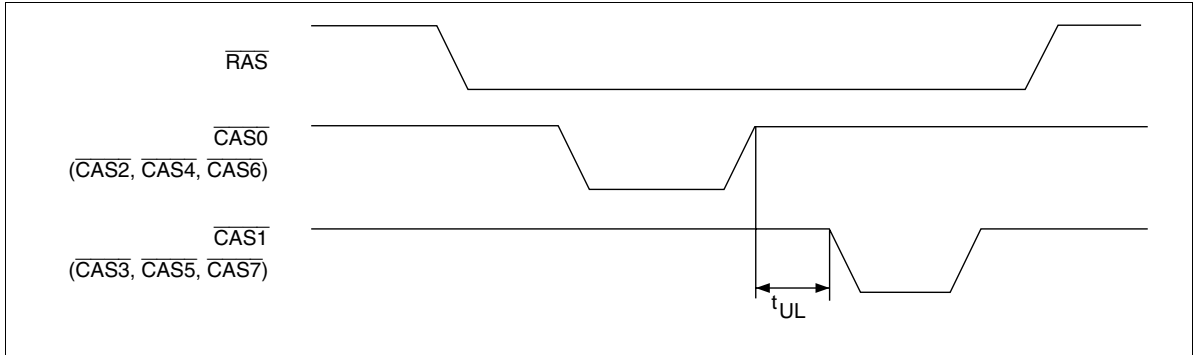
## Notes concerning $\overline{2CAS}$ control

Please do not separate the  $\overline{2CAS}$ s ( $\overline{CAS0}$  and  $\overline{CAS1}$  (or  $\overline{CAS2}$ ,  $\overline{CAS4}$ ,  $\overline{CAS6}$  and  $\overline{CAS3}$ ,  $\overline{CAS5}$ ,  $\overline{CAS7}$ )) operation timing intentionally. However skew between  $\overline{2CAS}$ s are allowed under the following conditions.

1. Each of the  $\overline{2CAS}$ s should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed: such as following.



3. Closely separated upper/lower byte control is not allowed. However when the condition ( $t_{CP} \leq t_{UL}$ ) is satisfied, page mode can be performed.

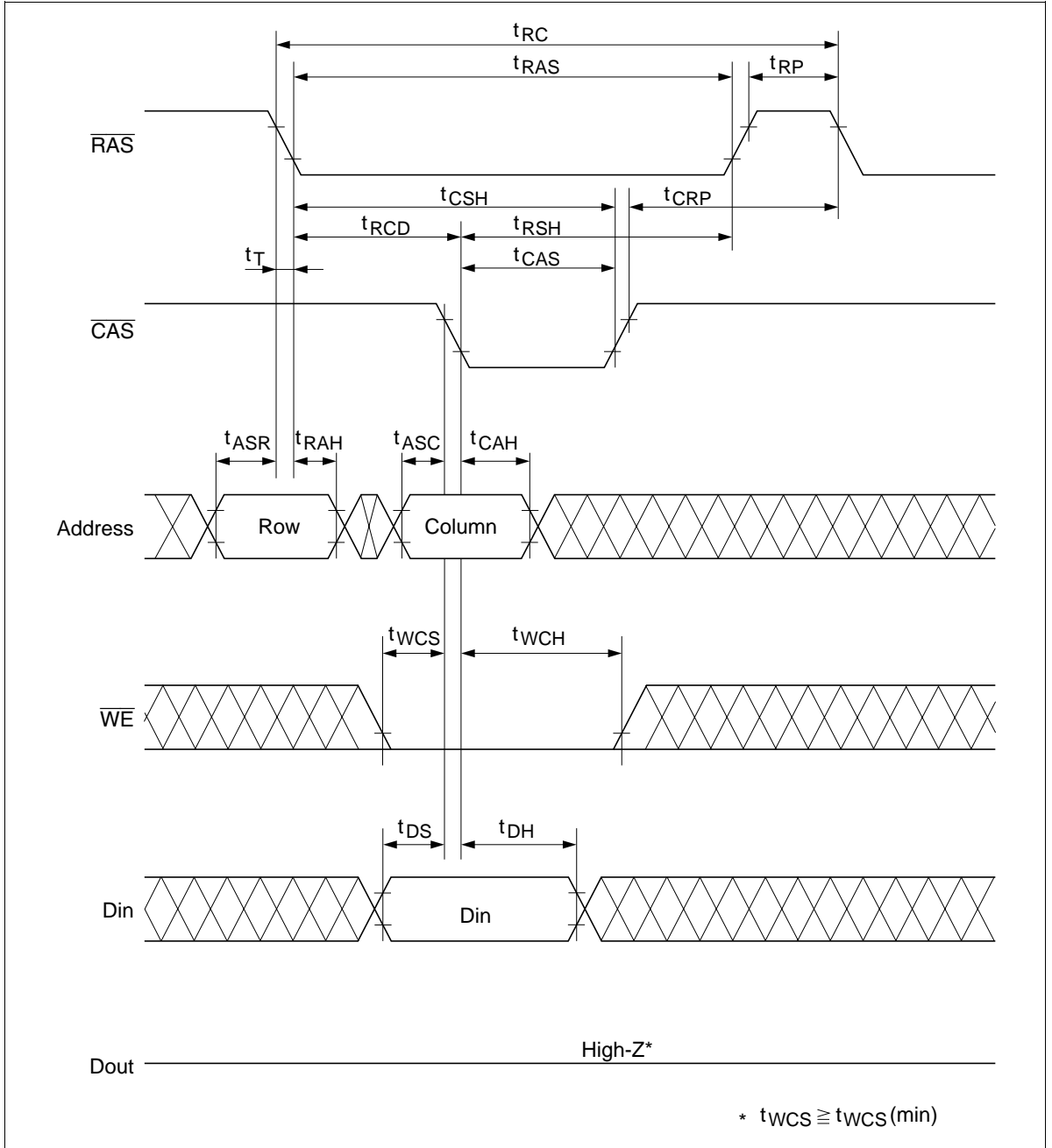


4. Byte control operation by remaining  $\overline{CAS0}$  ( $\overline{CAS2}$ ,  $\overline{CAS4}$ ,  $\overline{CAS6}$ ) or  $\overline{CAS1}$  ( $\overline{CAS3}$ ,  $\overline{CAS5}$ ,  $\overline{CAS7}$ ) high is guaranteed.

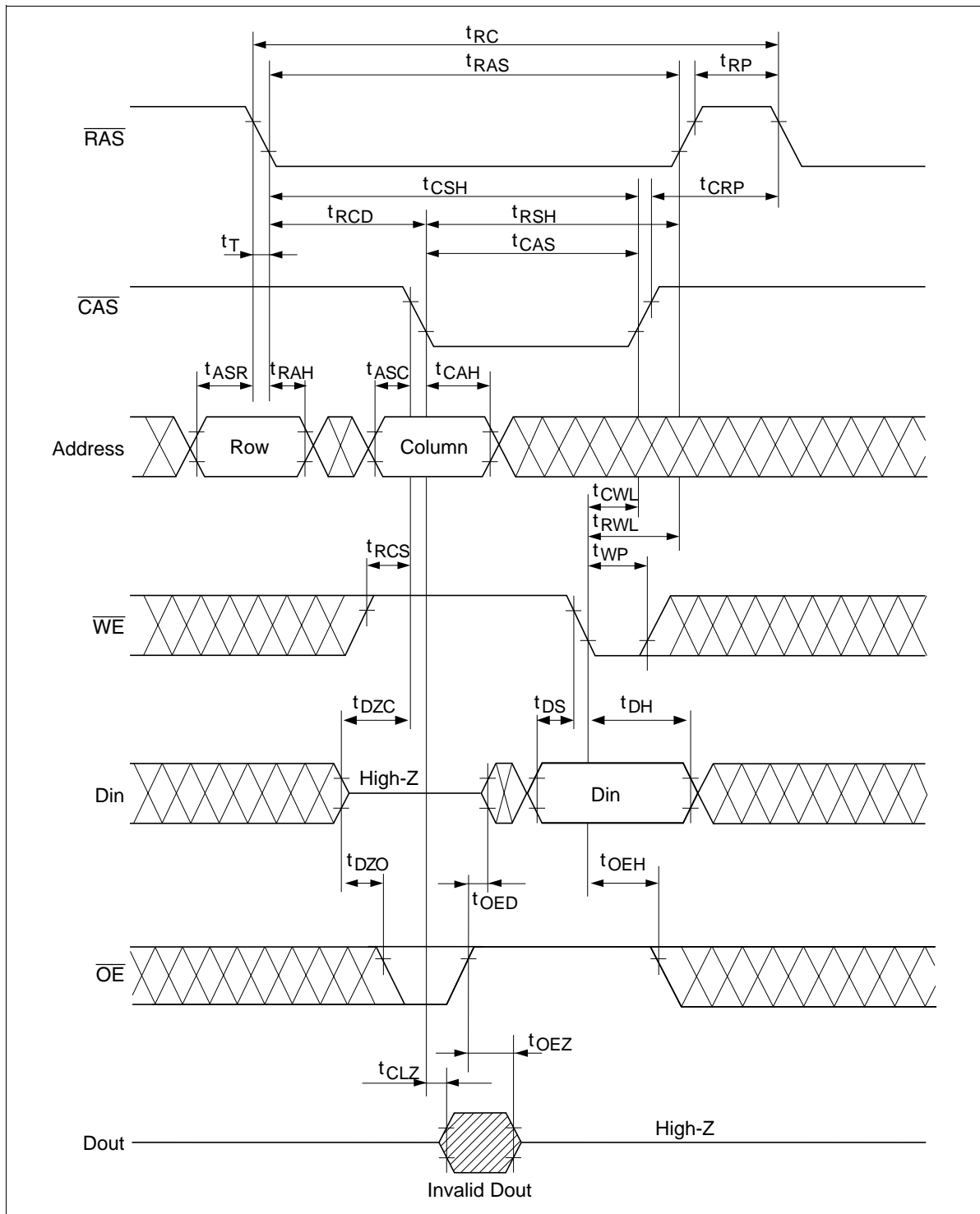


# HB56HW164DB Series, HB56HW165DB Series

## Early Write Cycle

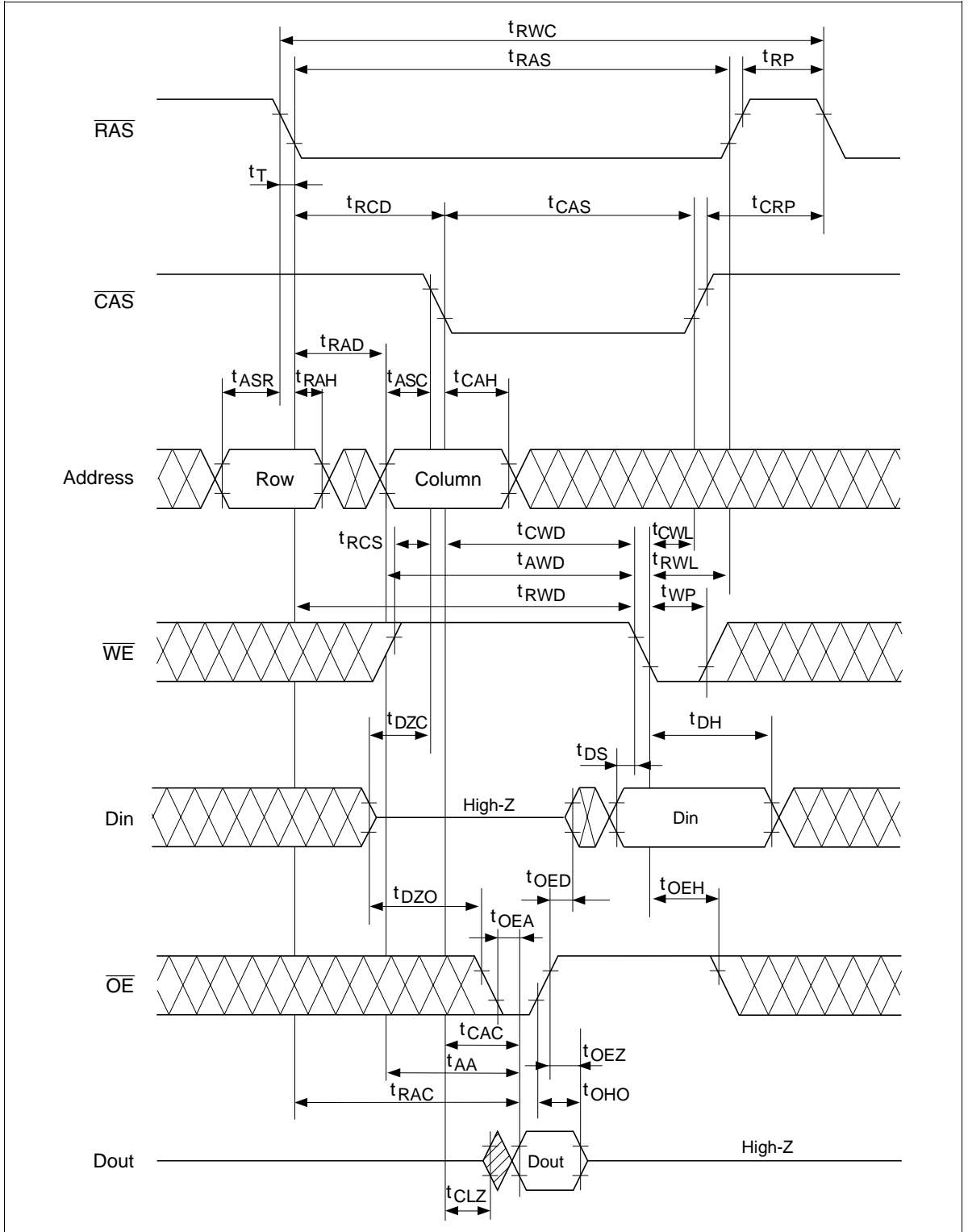


## Delayed Write Cycle\*18

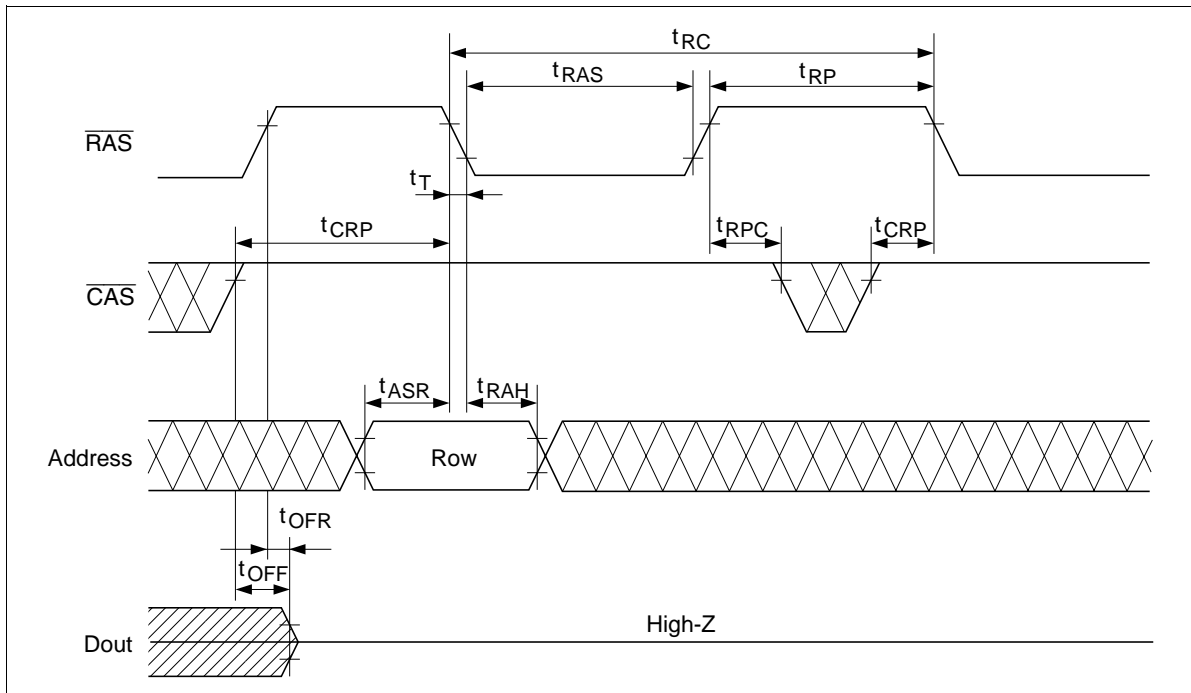


# HB56HW164DB Series, HB56HW165DB Series

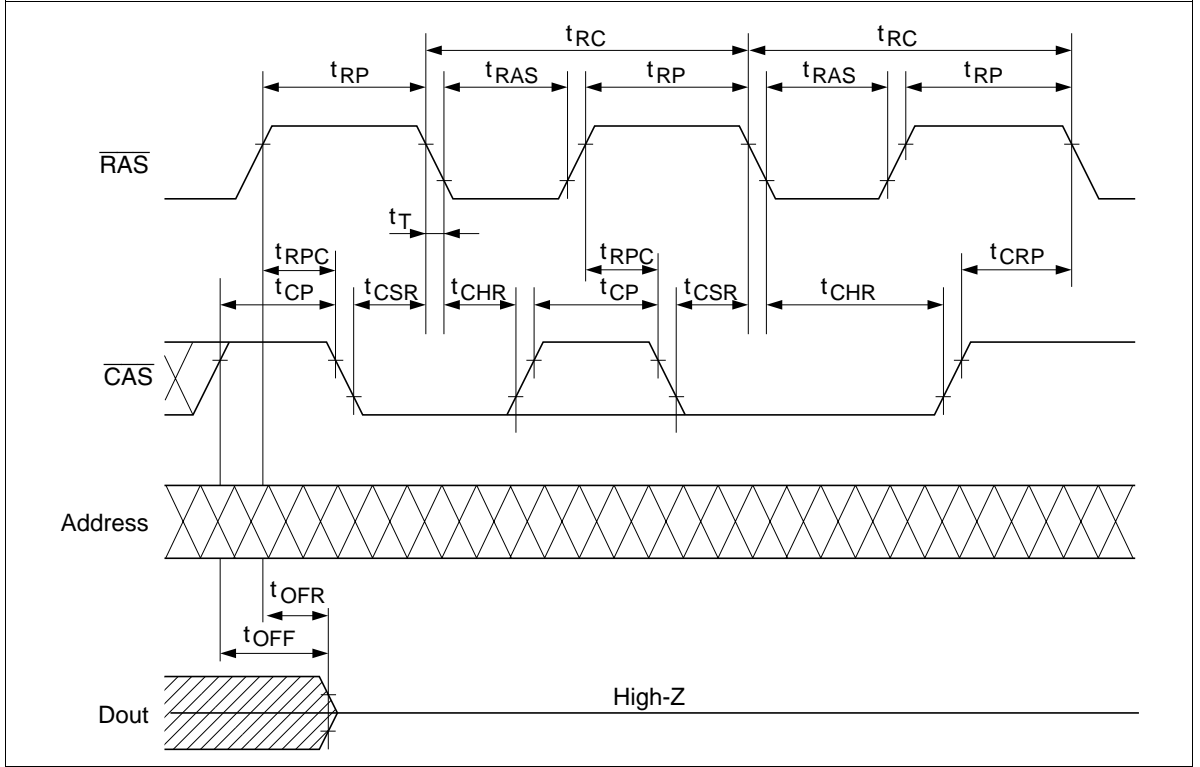
## Read-Modify-Write Cycle\*18



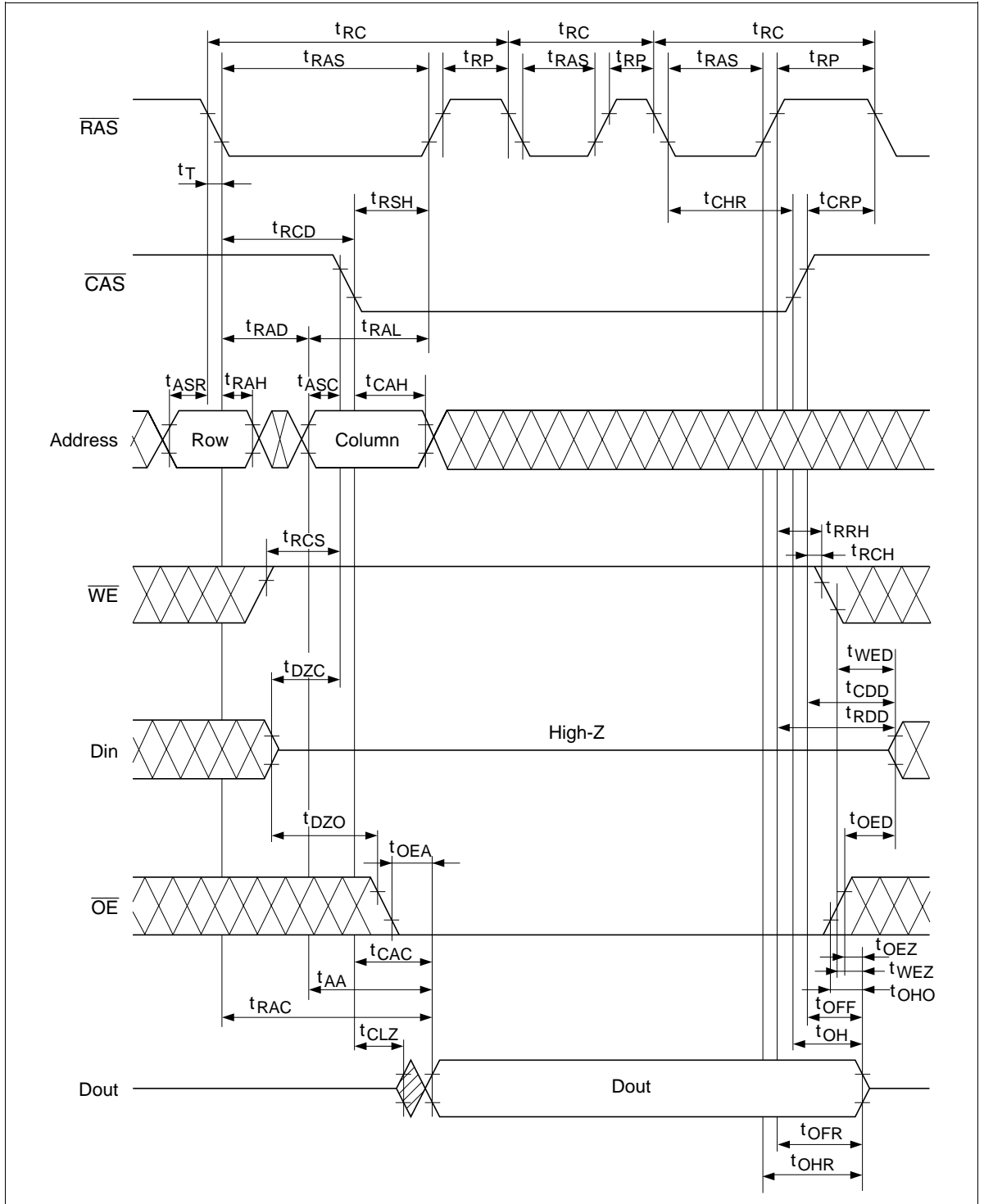
RAS-Only Refresh Cycle



**$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh Cycle**

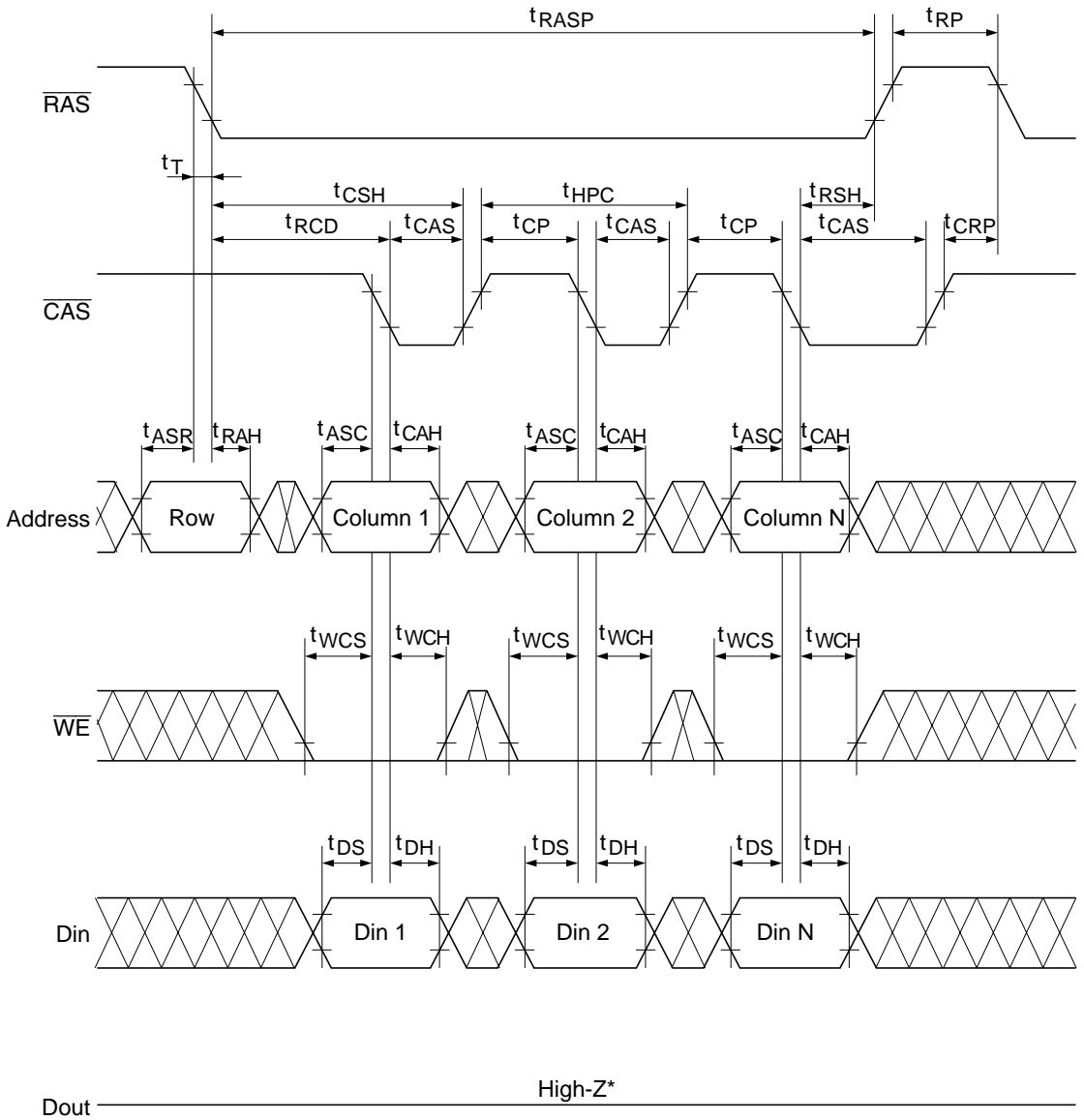


## Hidden Refresh Cycle





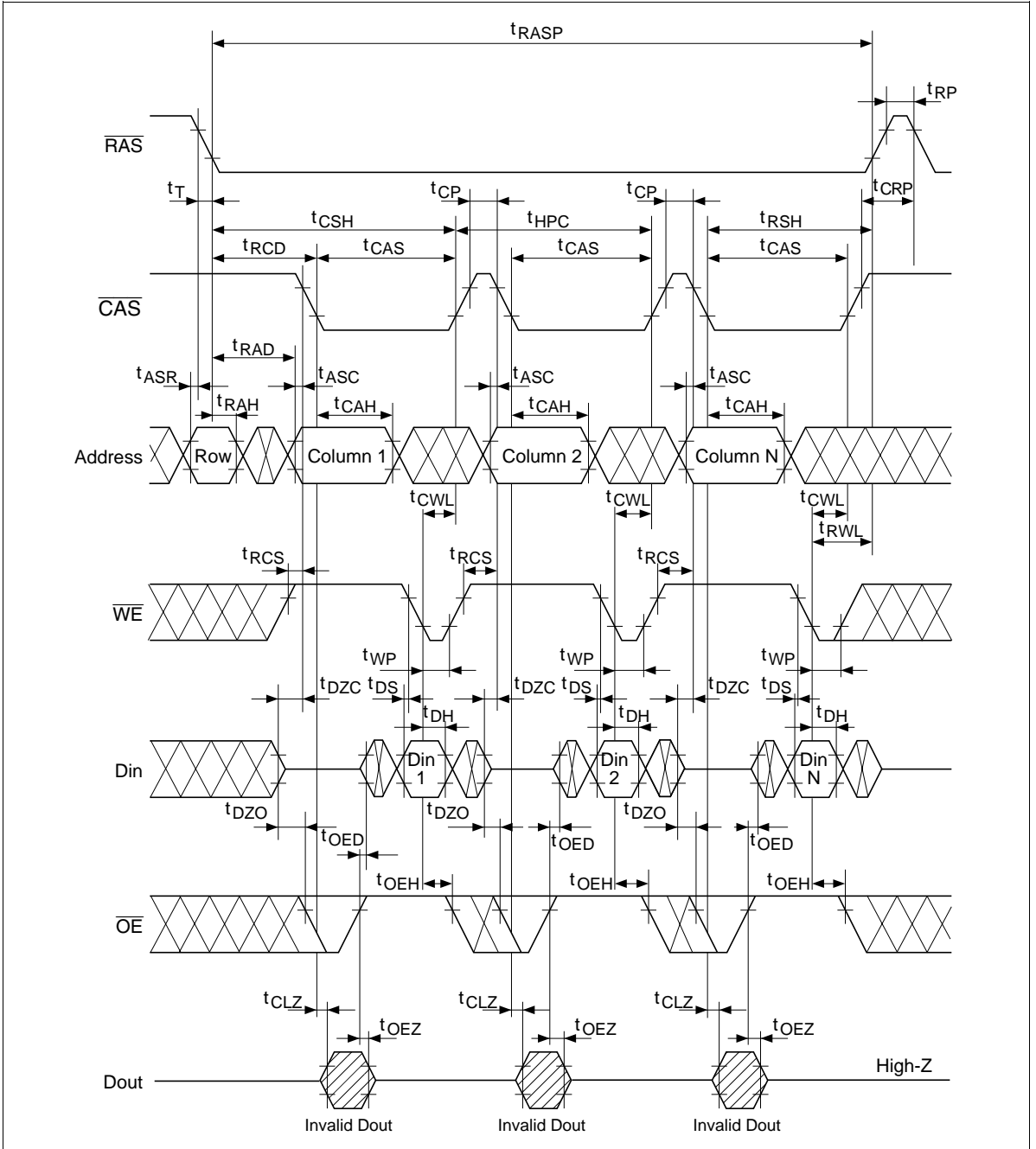
## EDO Page Mode Early Write Cycle



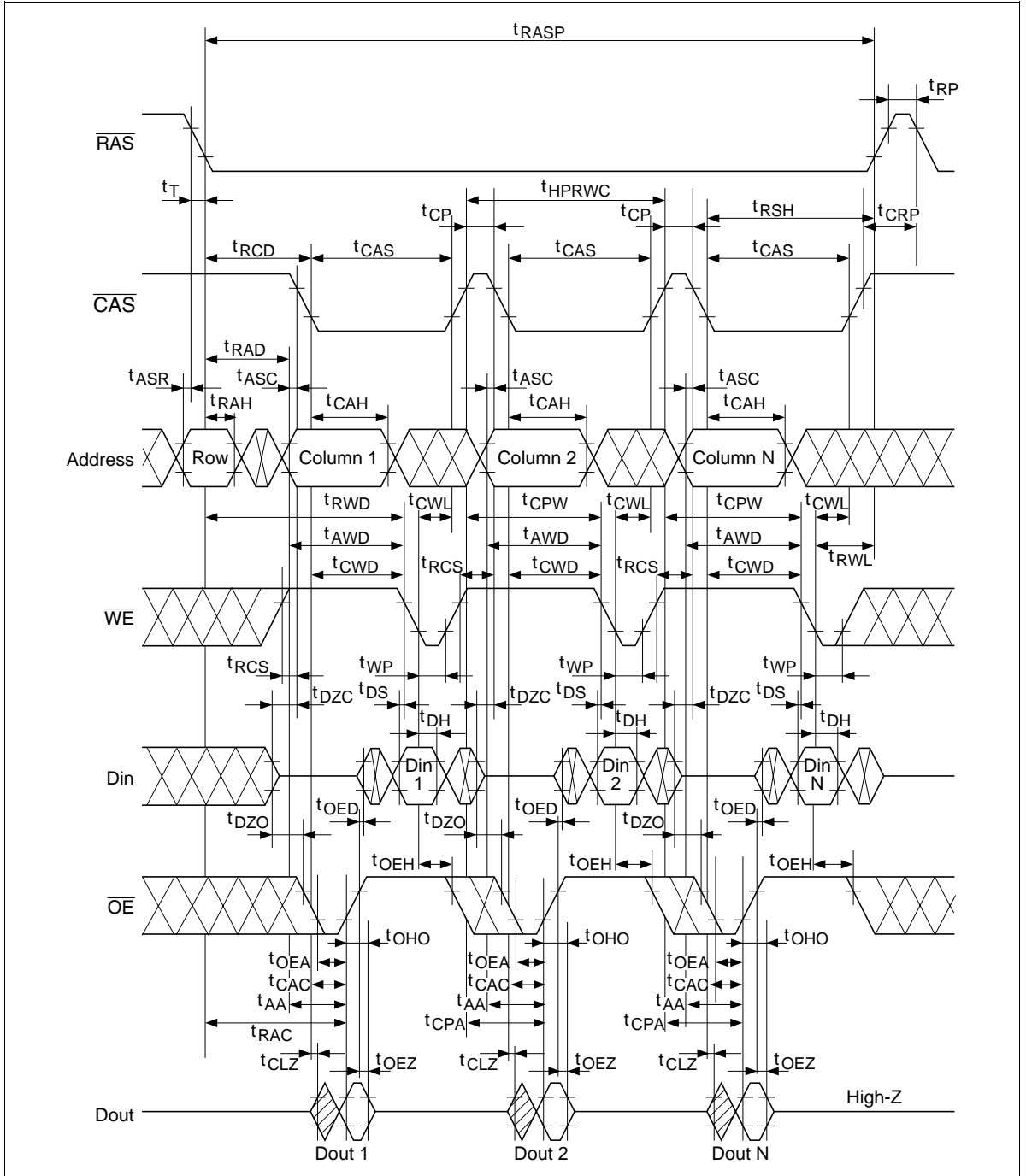
\*  $t_{WCS} \geq t_{WCS}(\min)$

# HB56HW164DB Series, HB56HW165DB Series

## EDO Page Mode Delayed Write Cycle\*18

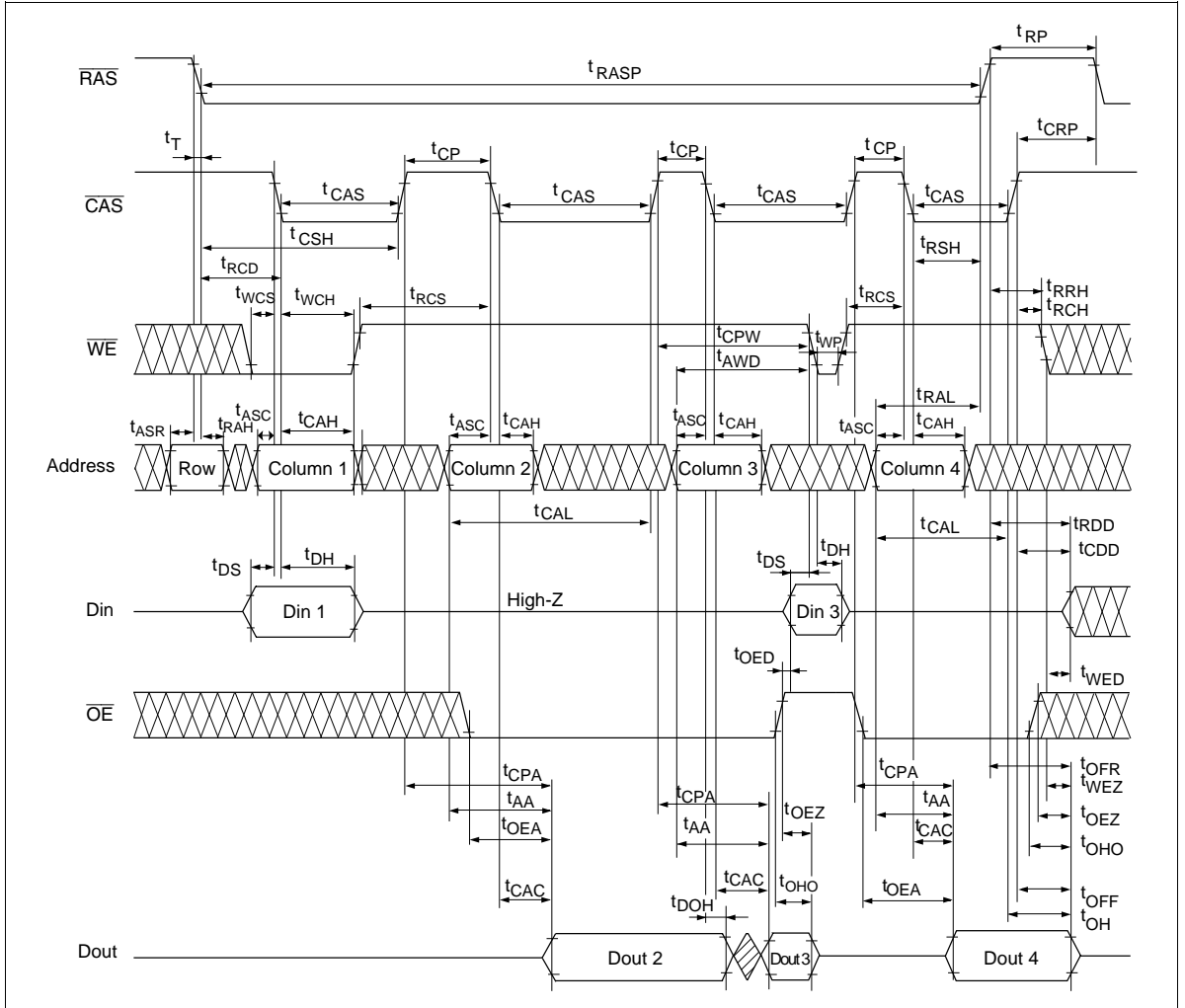


## EDO Page Mode Read-Modify-Write Cycle\*18



# HB56HW164DB Series, HB56HW165DB Series

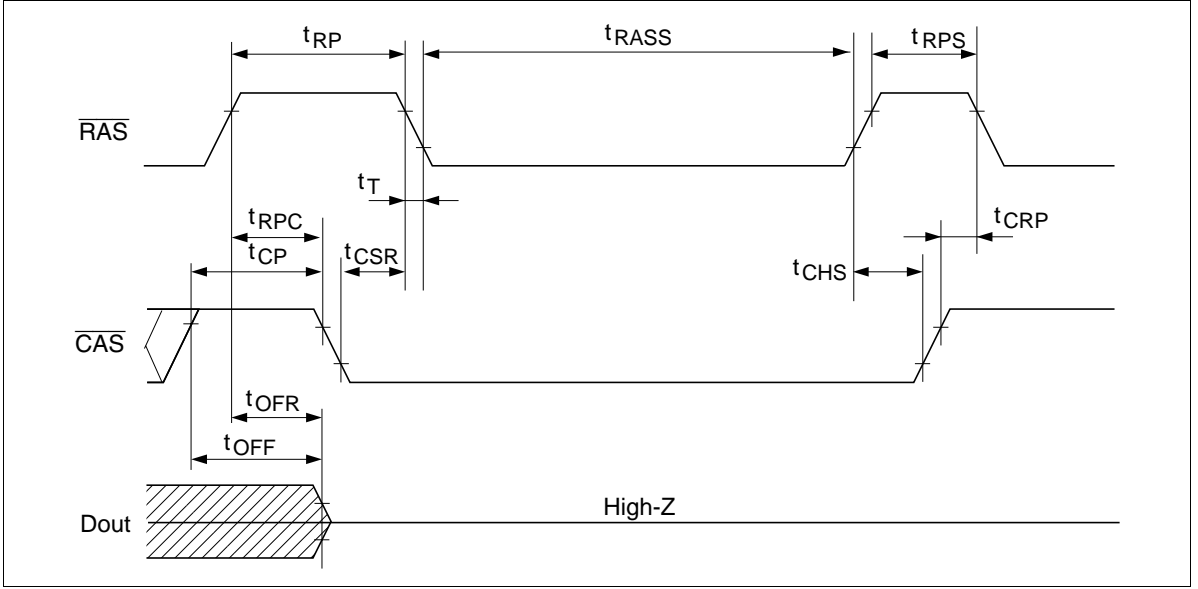
## EDO Page Mode Mix Cycle (1)





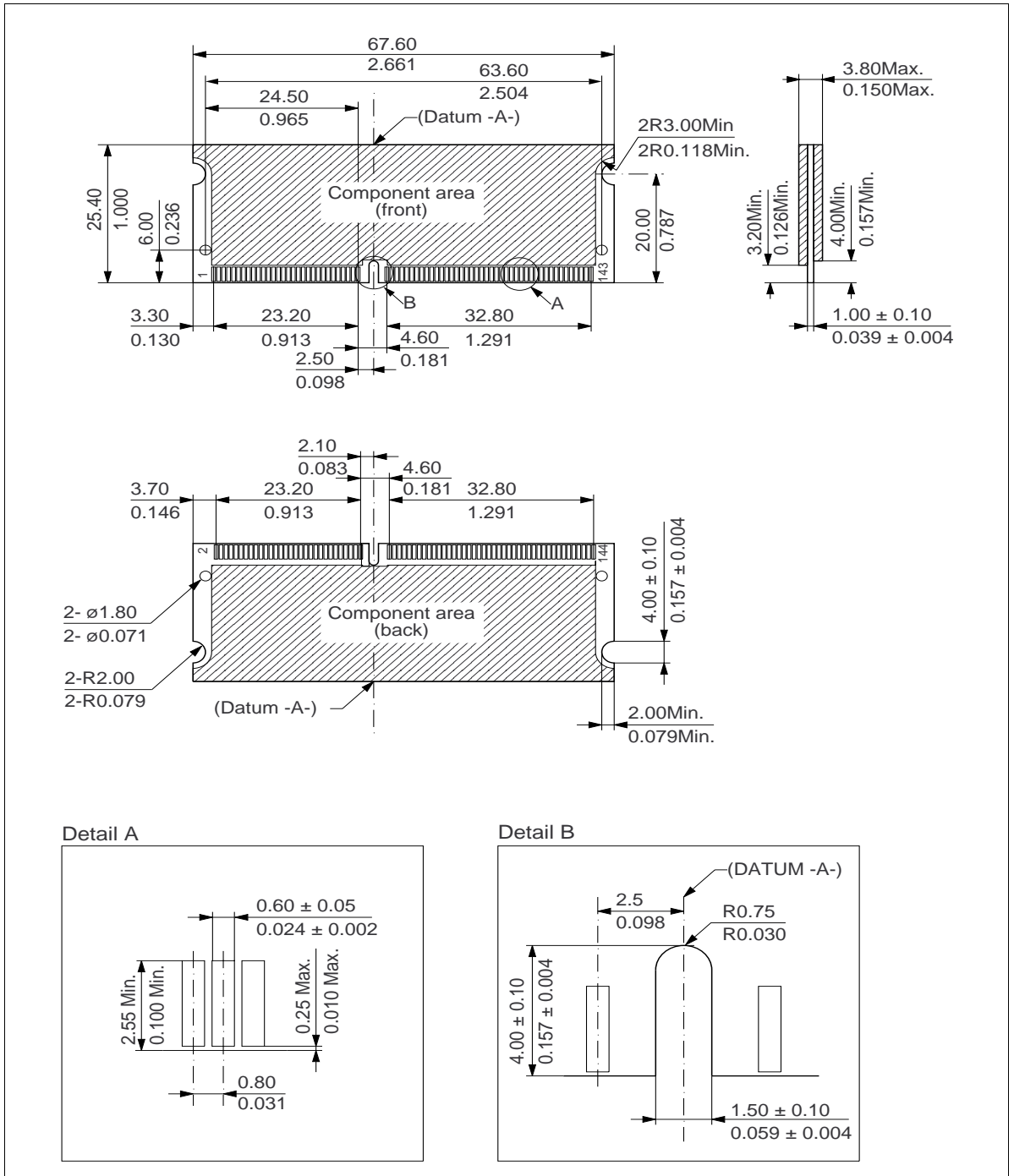
# HB56HW164DB Series, HB56HW165DB Series

## Self Refresh Cycle (L-version) \* 23, 24, 25, 26



Physical Outline

Unit: mm/inch



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**Revision Record**

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1.0	Dec. 27, 1996	Initial issue		

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