HB56H164EJN-6B/7B

1,048,576-word × 64-bit High Density Dynamic RAM Module
168-pin JEDEC Standard Outline Unbufferd 8 byte DIMM

HITACHI

ADE-203-552A(Z)
Rev. 1.0
Feb. 21, 1996

Description

The HB56H164EJN belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications.

The HB56H164EJN is a 1M × 64 dynamic RAM module, mounted 4 pieces of 16-Mbit DRAM (HM5118165BJ) sealed in SOJ package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56H164EJN offers Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56H164EJN is 168-pin socket type package (dual lead out). Therefore, the HB56H164EJN makes high density mounting possible without surface mount technology. The HB56H164EJN provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ on the module board.

Features

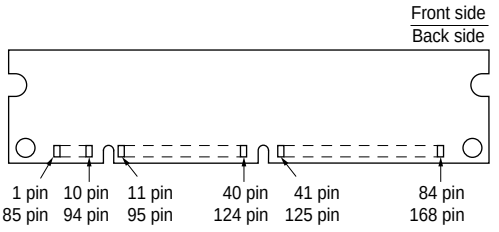
- 168-pin socket type package (Dual lead out)
  - — Lead pitch: 1.27 mm
- Single 5 V (±5%) supply
- High speed
  - — Access time: t_{RAC} = 60/70 ns (max)
- Access time: t_{CAC} = 15/18 ns (max)
- Low power dissipation
  - — Active mode: 3.6/3.2 W (max)
  - — Standby mode (TTL): 42 mW (max)
  - — Standby mode (CMOS): 21 mW (max)
- EDO page mode capability
- 1,024 refresh cycles: 16 ms
- 3 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
- TTL compatible

Hitachi semiconductor

Ordering Information

Type No.	Access time	Package	Contact pad
HB56H164EJN-6B	60 ns	168-pin dual lead out socket type	Gold
HB56H164EJN-7B	70 ns		

Pin Arrangement



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	13	DQ9	25	NC	37	A8
2	DQ0	14	DQ10	26	V_{CC}	38	NC
3	DQ1	15	DQ11	27	$\overline{WE0}$	39	NC
4	DQ2	16	DQ12	28	$\overline{CAS0}$	40	V_{CC}
5	DQ3	17	DQ13	29	$\overline{CAS1}$	41	V_{CC}
6	V_{CC}	18	V_{CC}	30	$\overline{RAS0}$	42	NC
7	DQ4	19	DQ14	31	$\overline{OE0}$	43	V_{SS}
8	DQ5	20	DQ15	32	V_{SS}	44	$\overline{OE2}$
9	DQ6	21	NC	33	A0	45	$\overline{RAS2}$
10	DQ7	22	NC	34	A2	46	$\overline{CAS2}$
11	DQ8	23	V_{SS}	35	A4	47	$\overline{CAS3}$
12	V_{SS}	24	NC	36	A6	48	$\overline{WE2}$

Pin Arrangement (cont)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
49	V_{CC}	79	NC	109	NC	139	DQ48
50	NC	80	NC	110	V_{CC}	140	DQ49
51	NC	81	NC	111	NC	141	DQ50
52	NC	82	SDA	112	$\overline{CAS4}$	142	DQ51
53	NC	83	SCL	113	$\overline{CAS5}$	143	V_{CC}
54	V_{SS}	84	V_{CC}	114	NC	144	DQ52
55	DQ16	85	V_{SS}	115	NC	145	NC
56	DQ17	86	DQ32	116	V_{SS}	146	NC
57	DQ18	87	DQ33	117	A1	147	NC
58	DQ19	88	DQ34	118	A3	148	V_{SS}
59	V_{CC}	89	DQ35	119	A5	149	DQ53
60	DQ20	90	V_{CC}	120	A7	150	DQ54
61	NC	91	DQ36	121	A9	151	DQ55
62	NC	92	DQ37	122	NC	152	V_{SS}
63	NC	93	DQ38	123	NC	153	DQ56
64	V_{SS}	94	DQ39	124	V_{CC}	154	DQ57
65	DQ21	95	DQ40	125	NC	155	DQ58
66	DQ22	96	V_{SS}	126	NC	156	DQ59
67	DQ23	97	DQ41	127	V_{SS}	157	V_{CC}
68	V_{SS}	98	DQ42	128	NC	158	DQ60
69	DQ24	99	DQ43	129	NC	159	DQ61
70	DQ25	100	DQ44	130	$\overline{CAS6}$	160	DQ62
71	DQ26	101	DQ45	131	$\overline{CAS7}$	161	DQ63
72	DQ27	102	V_{CC}	132	NC	162	V_{SS}
73	V_{CC}	103	DQ46	133	V_{CC}	163	NC
74	DQ28	104	DQ47	134	NC	164	NC
75	DQ29	105	NC	135	NC	165	SA0
76	DQ30	106	NC	136	NC	166	SA1
77	DQ31	107	V_{SS}	137	NC	167	SA2
78	V_{SS}	108	NC	138	V_{SS}	168	V_{CC}

Pin Description

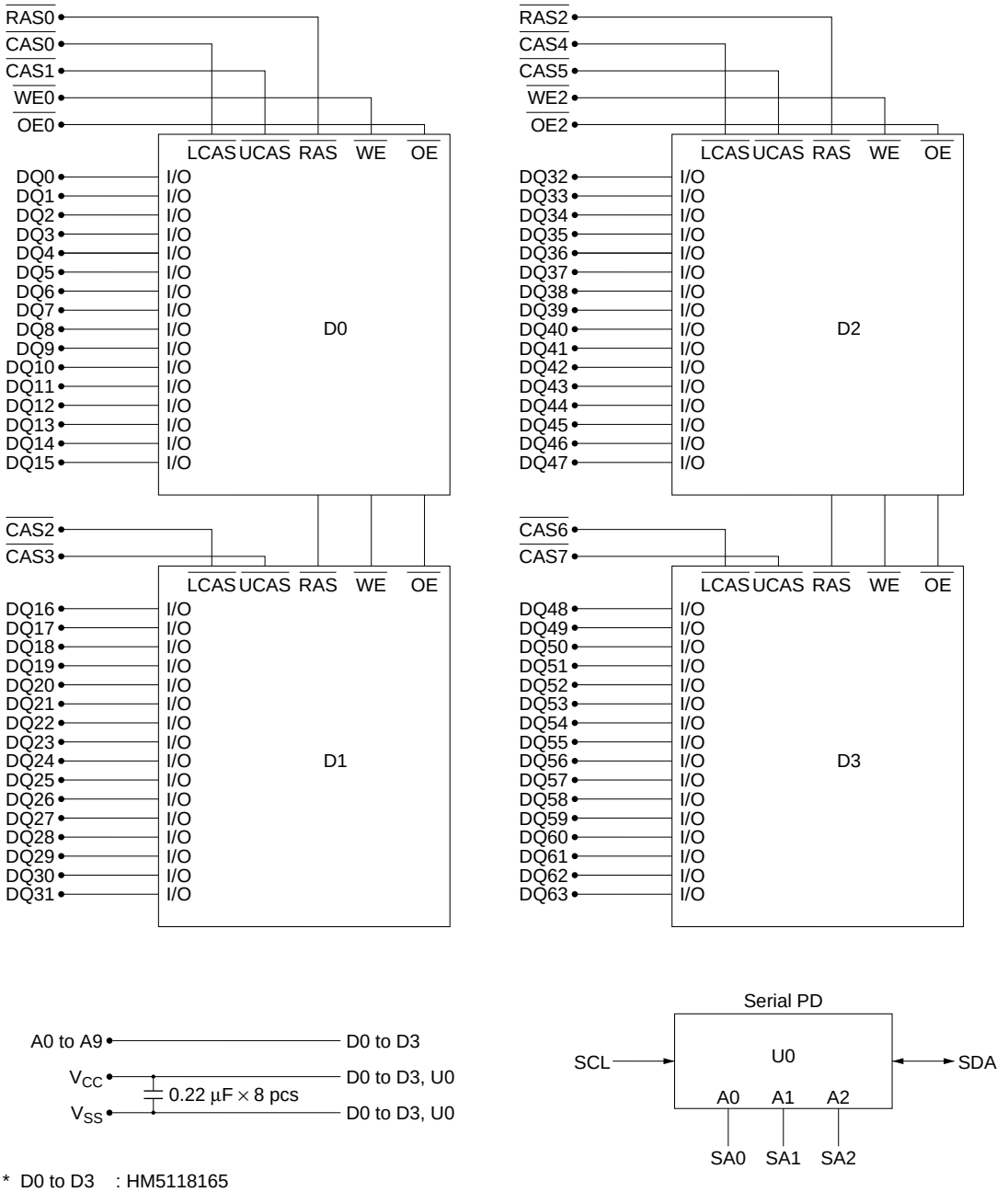
Pin Name	Function
A0 to A9	Address Input : A0 to A9 Row Address : A0 to A9 Column Address : A0 to A9 Refresh Address : A0 to A9
DQ0 to DQ63	Data-in/Data-out
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ to $\overline{CAS7}$	Column Address Strobe
$\overline{WE0}$, $\overline{WE2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
SDA	Serial Data for PD
SCL	Serial Clock for PD
SA0 to SA2	Serial Address for PD
V_{CC}	Power Supply
V_{SS}	Ground
NC	Non Connection

Serial PD Matrix

Byte Number	Function Described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Note
0	Number Serial PD Bytes	0	0	0	0	1	1	0	1	13
1	Serial Memorry	0	0	0	0	1	0	0	0	256 Bytes
2	Fundamental Memory Type	0	0	0	0	0	0	1	0	EDO
3	Number of Rows	0	0	0	0	1	0	1	0	10
4	Number of Columns	0	0	0	0	1	0	1	0	10
5	Number of Banks	0	0	0	0	0	0	0	1	1
6	Data Width	0	1	0	0	0	0	0	0	64
7	Data Width (continued)	0	0	0	0	0	0	0	0	0 (+)
8	Voltage Interface	0	0	0	0	0	0	0	0	5.0 Volt
9	$\overline{RAS}$ Access Time 60 ns	0	0	1	1	1	1	0	0	
	$\overline{RAS}$ Access Time 70 ns	0	1	0	0	0	1	1	0	
10	$\overline{CAS}$ Access Time 15 ns	0	0	0	0	1	1	1	1	
	$\overline{CAS}$ Access Time 18 ns	0	0	0	1	0	0	1	0	
11	Error Detection/Corraction	0	0	0	0	0	0	0	0	None-Parity
12	Refresh Period	0	0	0	0	0	0	0	0	Normal (15.625µs)

Note: Serial-PD Datas are not protected.
1: High Level (Serial Data)
0: Low Level (Serial Data)

Block Diagram



* D0 to D3 : HM5118165
U0 : 24C02

Note
1. The SDA pull-up resistor is required due to the open-drain/open-collecter output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inactive "High" state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit

Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	Pt	4	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		60 ns		70 ns				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test condition**	**Note**
Operating current	I_{CC1}	—	680	—	600	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	8	—	8	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	4	—	4	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	680	—	600	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	20	—	20	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	680	—	600	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	740	—	660	mA	t_{HPC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	40	pF	1
Input capacitance ($\overline{RAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	—	34	pF	1
Input capacitance ($\overline{CAS}$)	C_{I3}	—	27	pF	1
I/O capacitance (DQ)	$C_{I/O}$	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)[*1, *2, *18, *19]

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	15	—	18	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	48	—	58	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	ns	7
Refresh period (1,024 cycles)	t_{REF}	—	16	—	16	ms	

Read Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 17
Access time from $\overline{OE}$	t_{OEA}	—	15	—	18	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{RAS}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	5	—	5	—	ns	12
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{CAS}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	ns	
Output buffer turn-off time to $\overline{RAS}$	t_{OFR}	—	15	—	15	ns	
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	15	—	15	ns	
$\overline{WE}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	15	—	18	—	ns	

Write Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	ns	14
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	15
Data-in hold time	t_{DH}	10	—	13	—	ns	15

Read-Modify-Write Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	136	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	49	—	57	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	18	—	ns	

Refresh Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	ns	

EDO Page Mode Cycle

		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode cycle time	t_{HPC}	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	35	—	40	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time refferd $\overline{OE}$	t_{COL}	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Reas command hold time from $\overline{CAS}$ precharge	t_{RCHC}	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

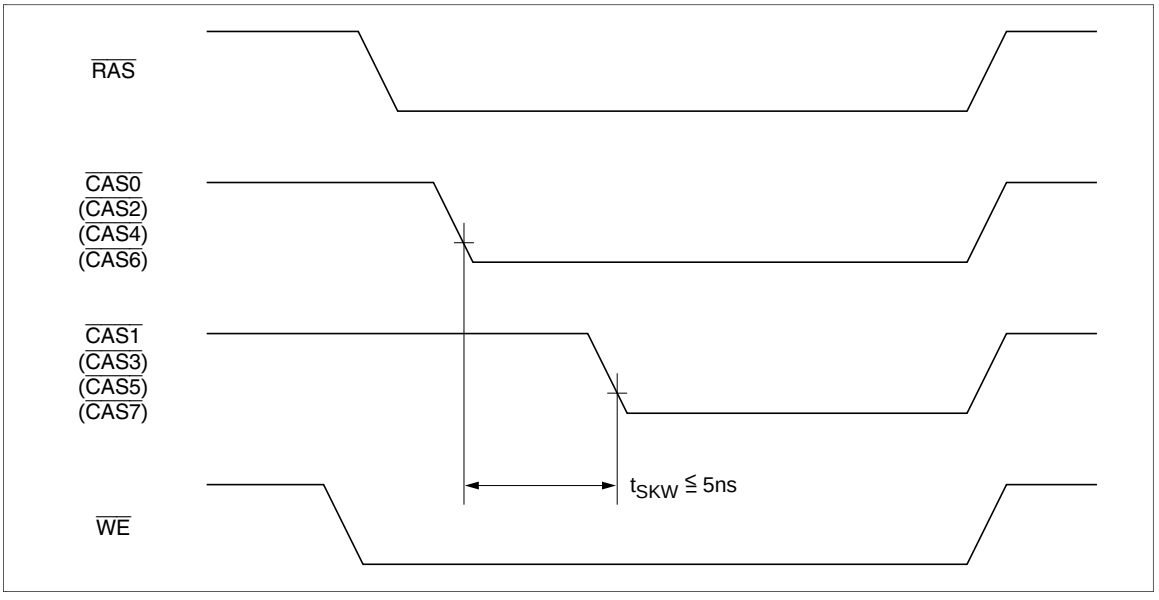
		60 ns		70 ns			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
EDO page mode read-modify-write cycle time	t_{HPRWC}	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	54	—	62	—	ns	14

Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RAD}$ (max) + t_{AA} (max) - t_{CAC} (max), then access time is controlled exclusively by t_{CAC}.
4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
5. Either t_{OED} or t_{CDD} must be satisfied.
6. Either t_{DZO} or t_{DZC} must be satisfied.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
8. Assumes that $t_{RCD} < t_{RCD}$ (max) and $t_{RAD} < t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
9. Measured with a load circuit equivalent to 1TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
13. t_{OFF} (max) and t_{OEZ} (max) is define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among t_{AA}, t_{CAC} or t_{CPA}.
18. In delayed write or read-modify-write cycle, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the DQ pin will remain open circuit (high impedance); if $t_{OEH} \leq t_{CWL}$, invalid data will be out at each DQ.
19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
21. When output buffers are enabeled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min / V_{IL} max level.

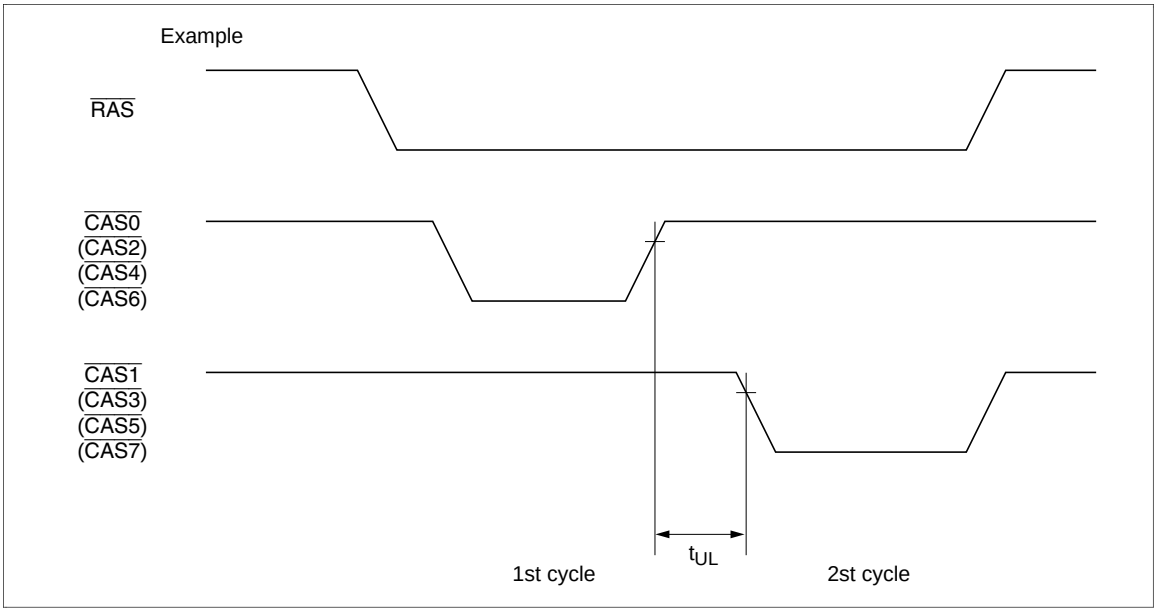
Notes concerning 2$\overline{CAS}$ control

(1) In one memory cycle, active both of 2$\overline{CAS}$s ($\overline{CAS0}$ and $\overline{CAS1}$ (or $\overline{CAS2}$, 4, 6 and $\overline{CAS3}$, 5, 7)) or only one of them or neither of them.

(2) To activate both of 2$\overline{CAS}$s in an early write cycle or a page mode early write cycle, please keep t_{SKW} (skew between $\overline{CAS0}$ and $\overline{CAS1}$ (or $\overline{CAS2}$, 4, 6 and $\overline{CAS3}$, 5, 7)) 5 ns or less.

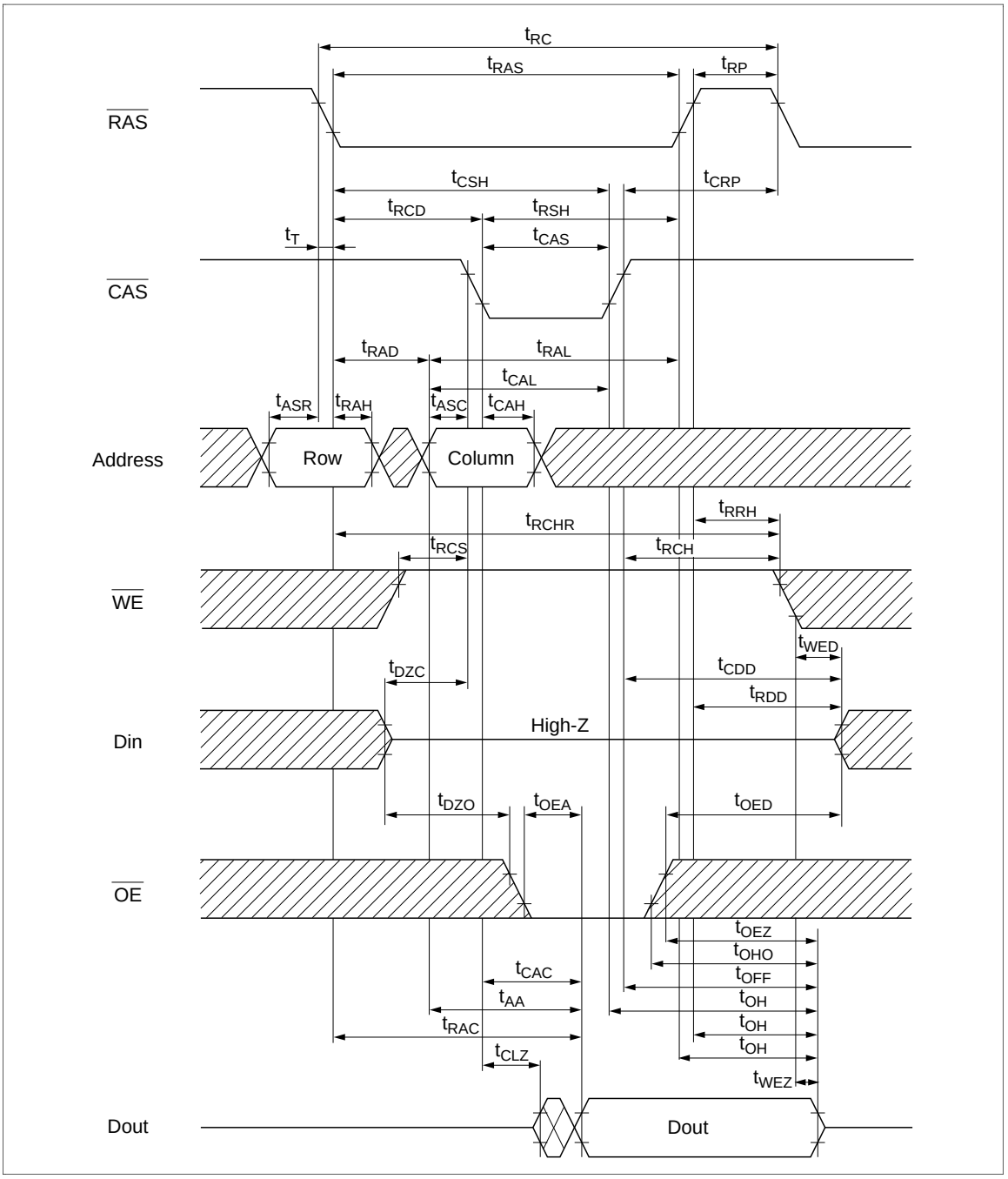


(3) If the different $\overline{CAS}$s are activated in the consecutive page cycles, t_{UL} the period that both $\overline{CAS}$s are high, should be keep t_{CP} spec (t_{CP} min ≤ t_{UL}).



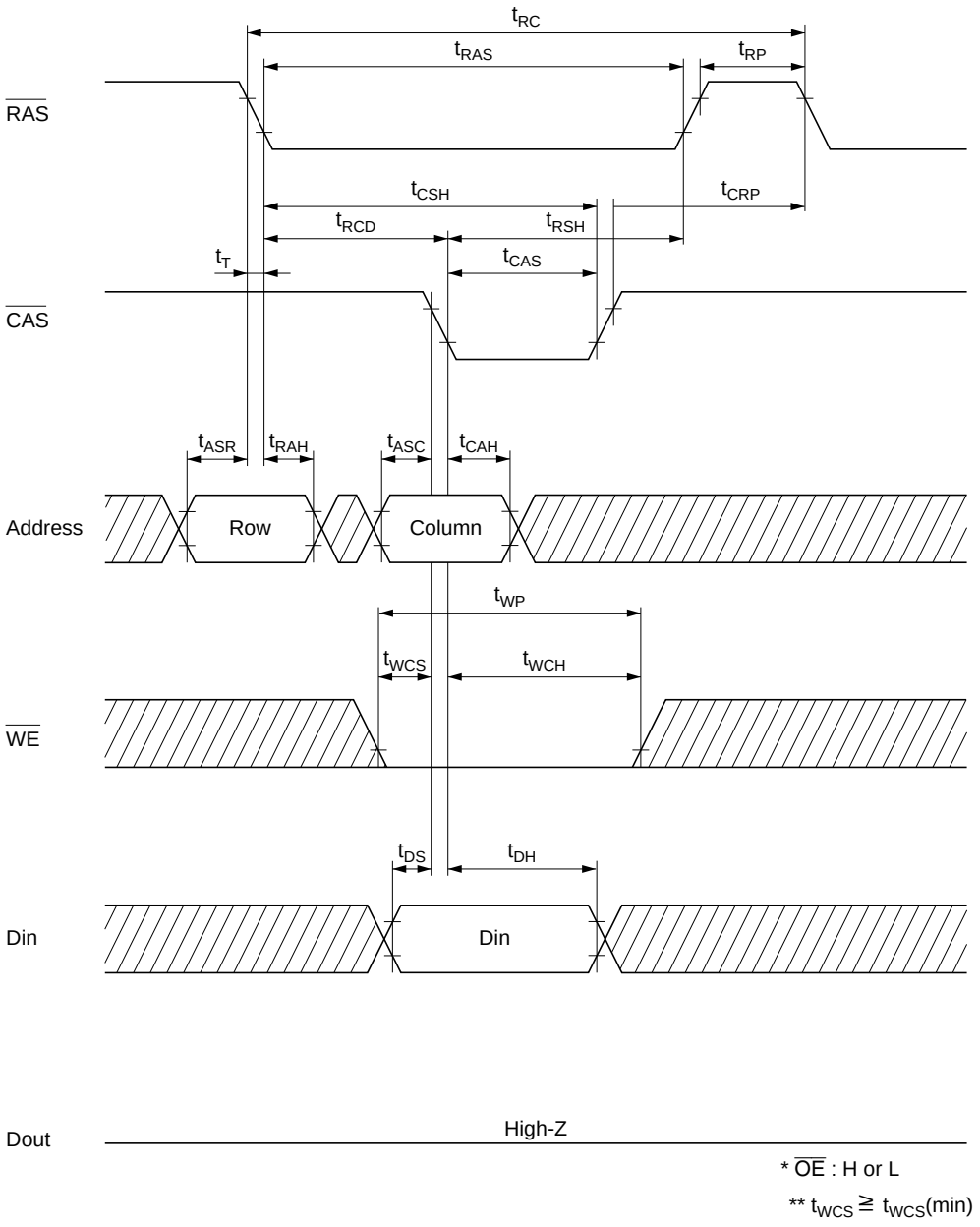
Timing Waveforms

Read Cycle



Note : H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))
Invalid Dout

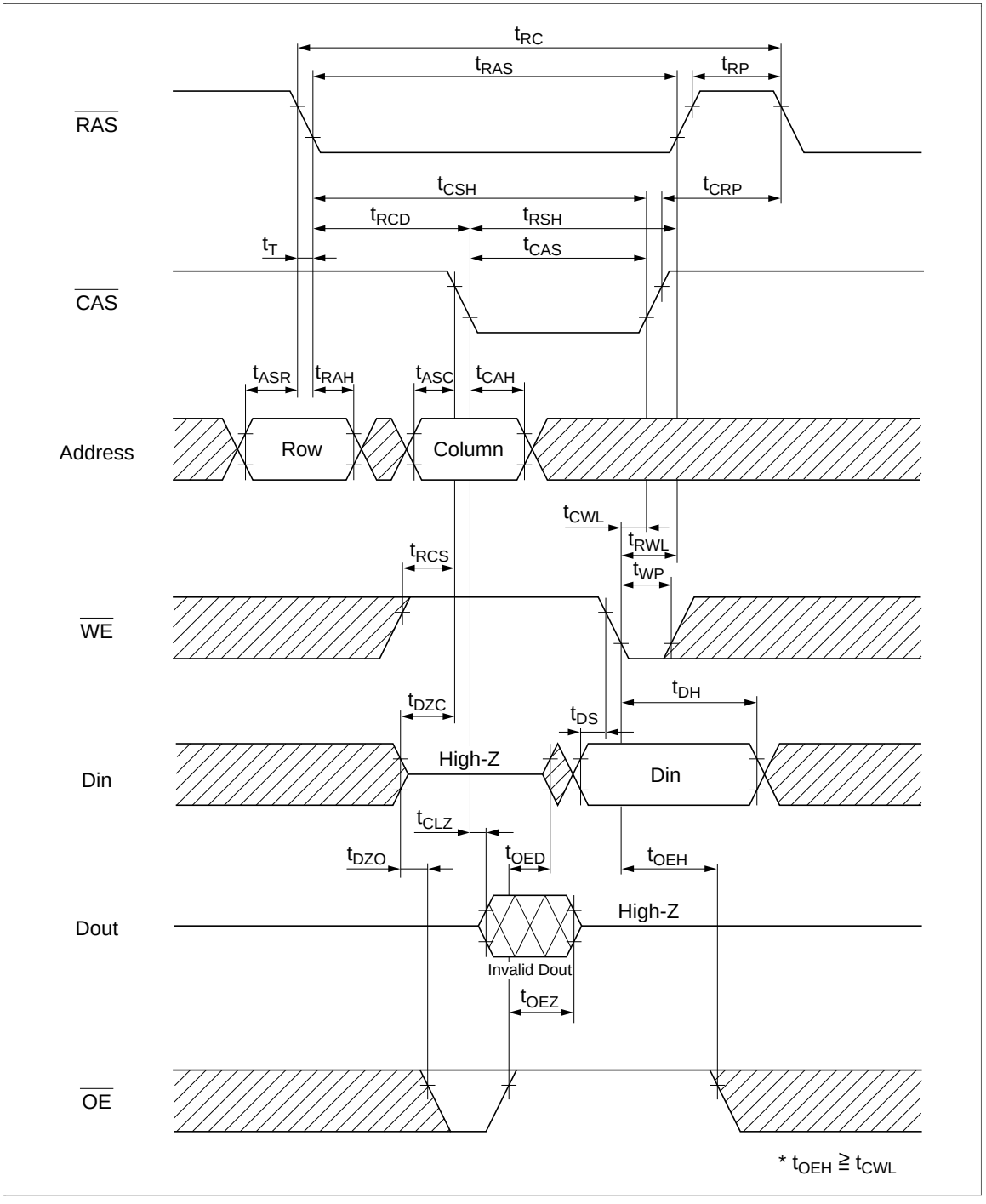
Early Write Cycle



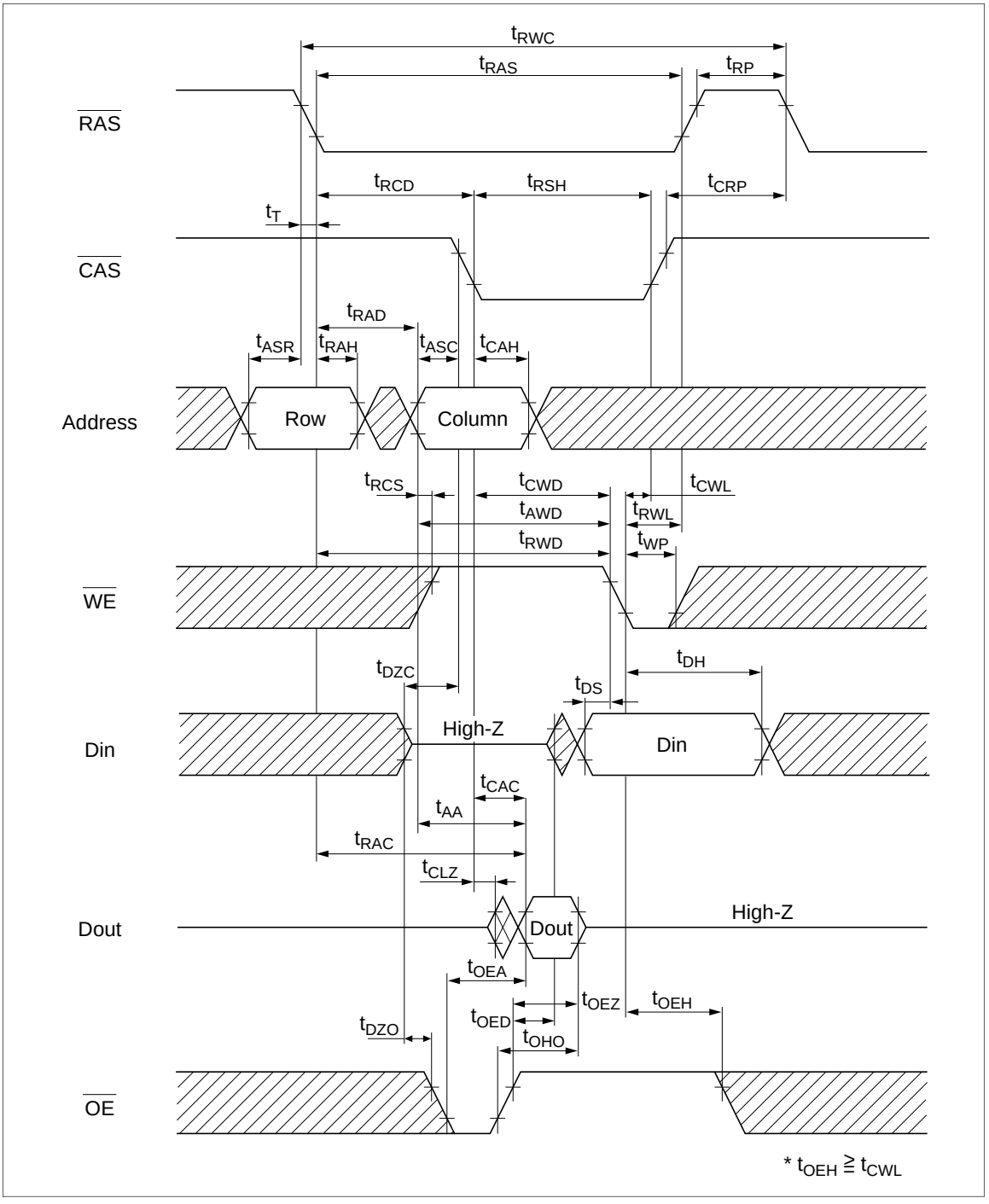
* $\overline{OE}$: H or L

** $t_{WCS} \geqq t_{WCS}(min)$

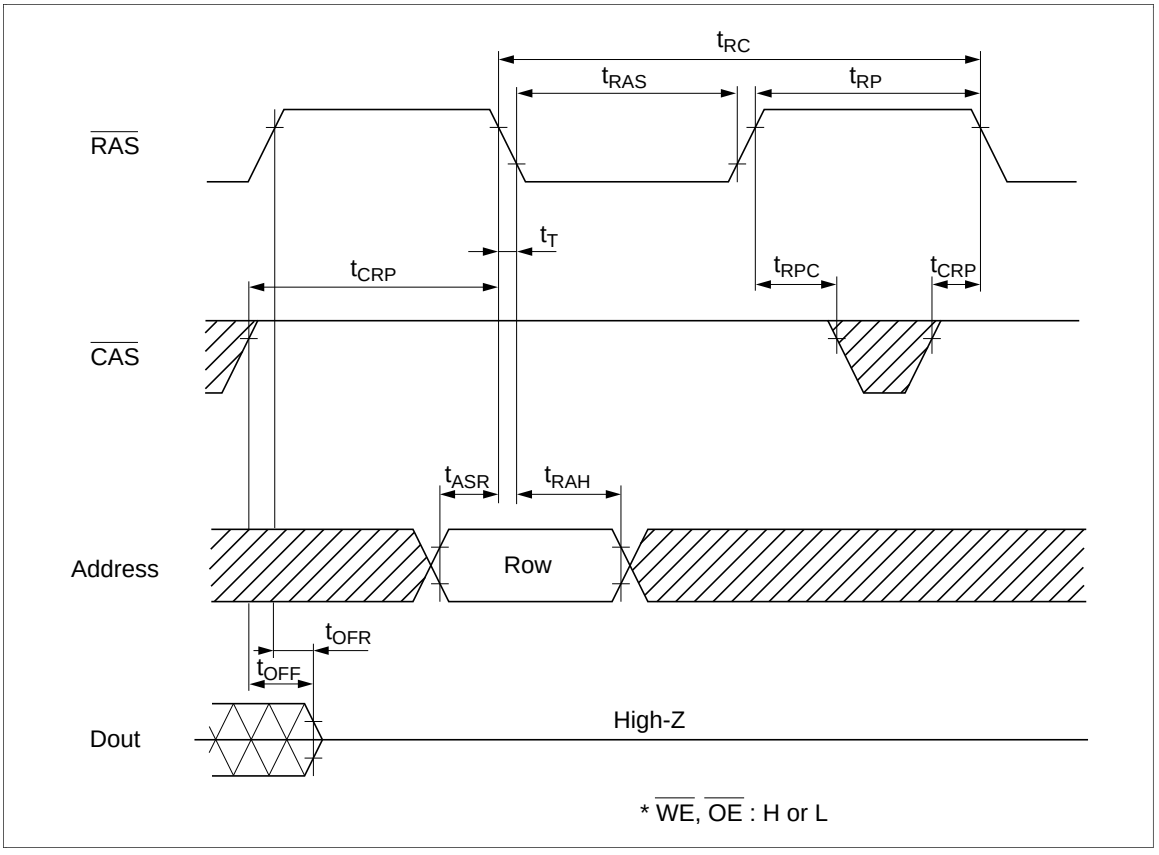
Delayd Write Cycle



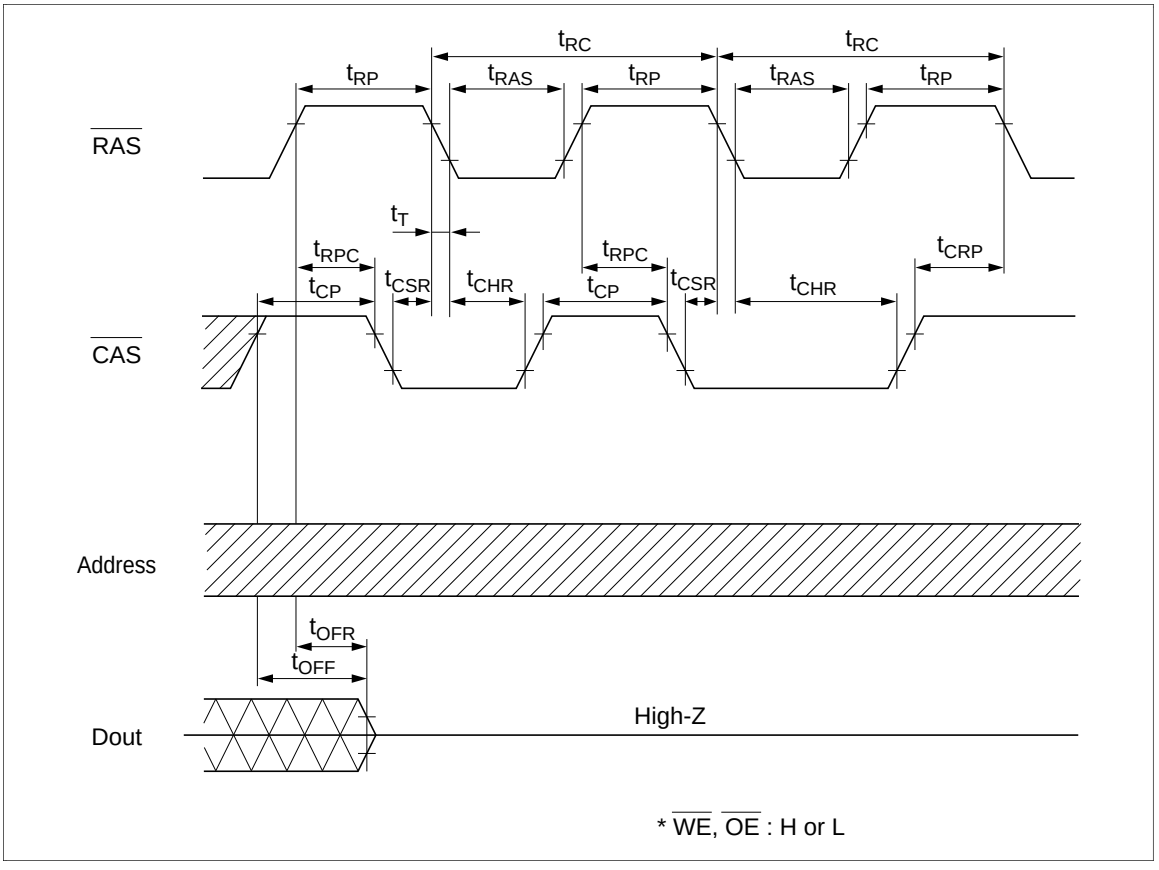
Read-Modify-Write Cycle



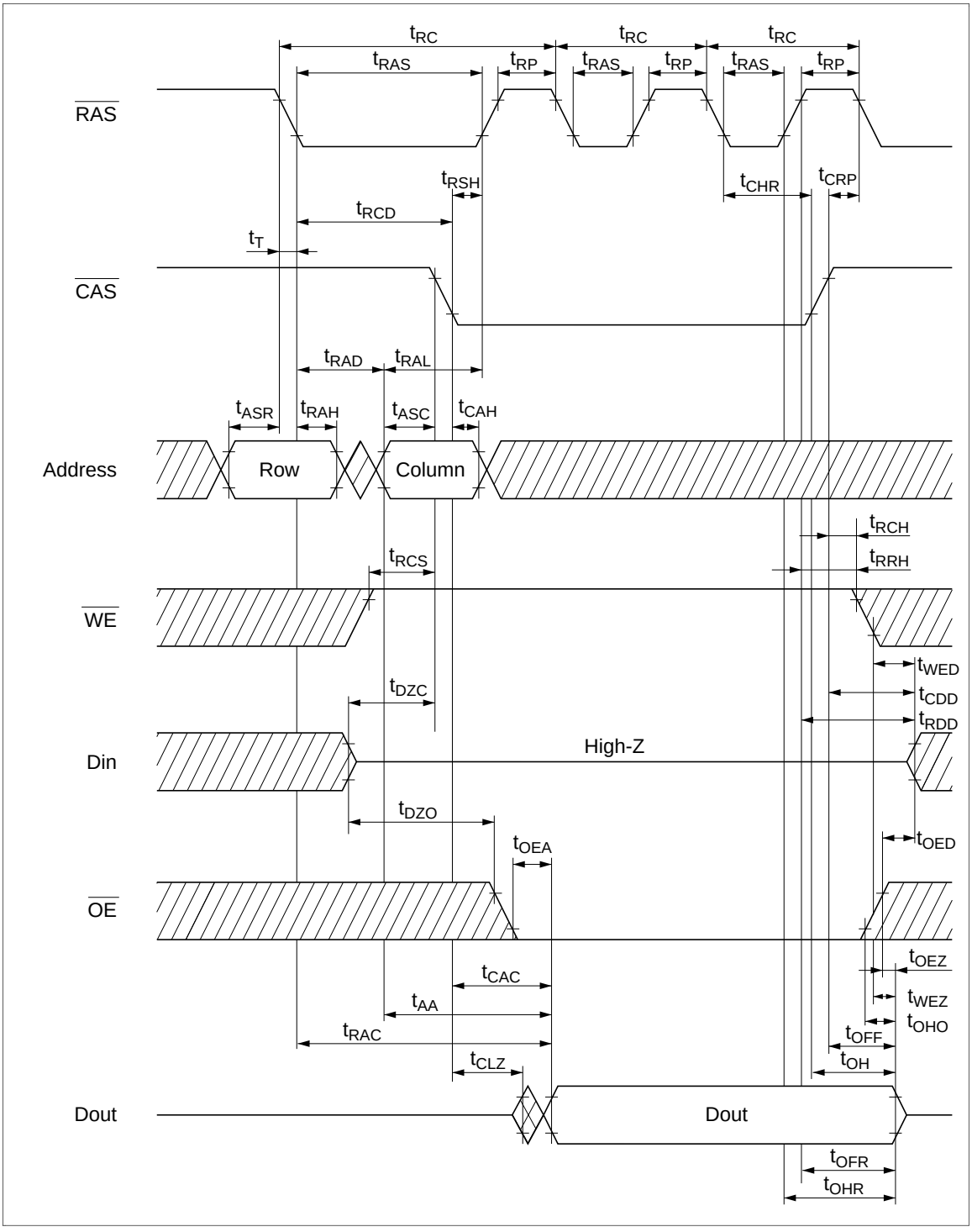
$\overline{\text{RAS}}$-Only Refresh Cycle



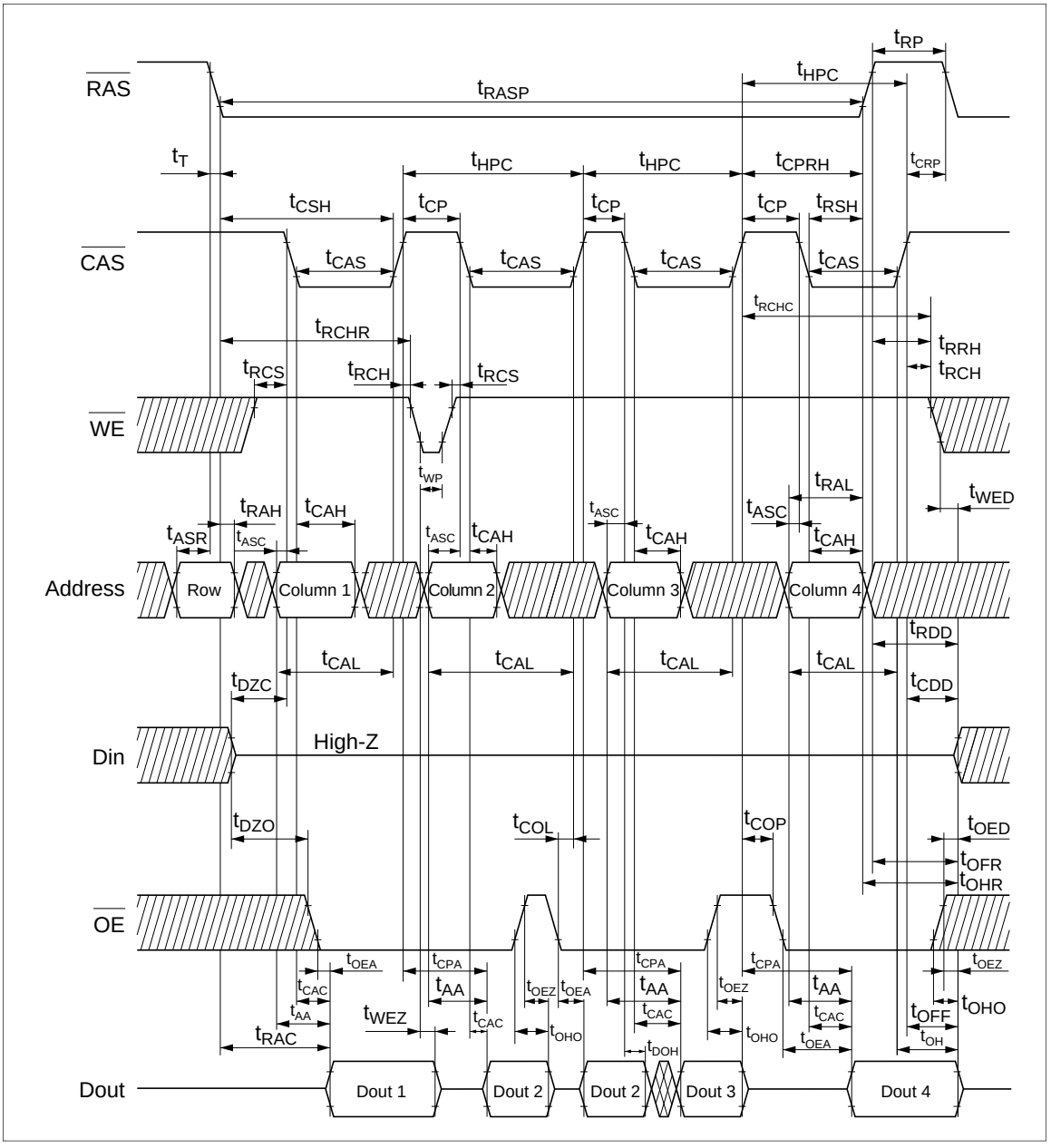
$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



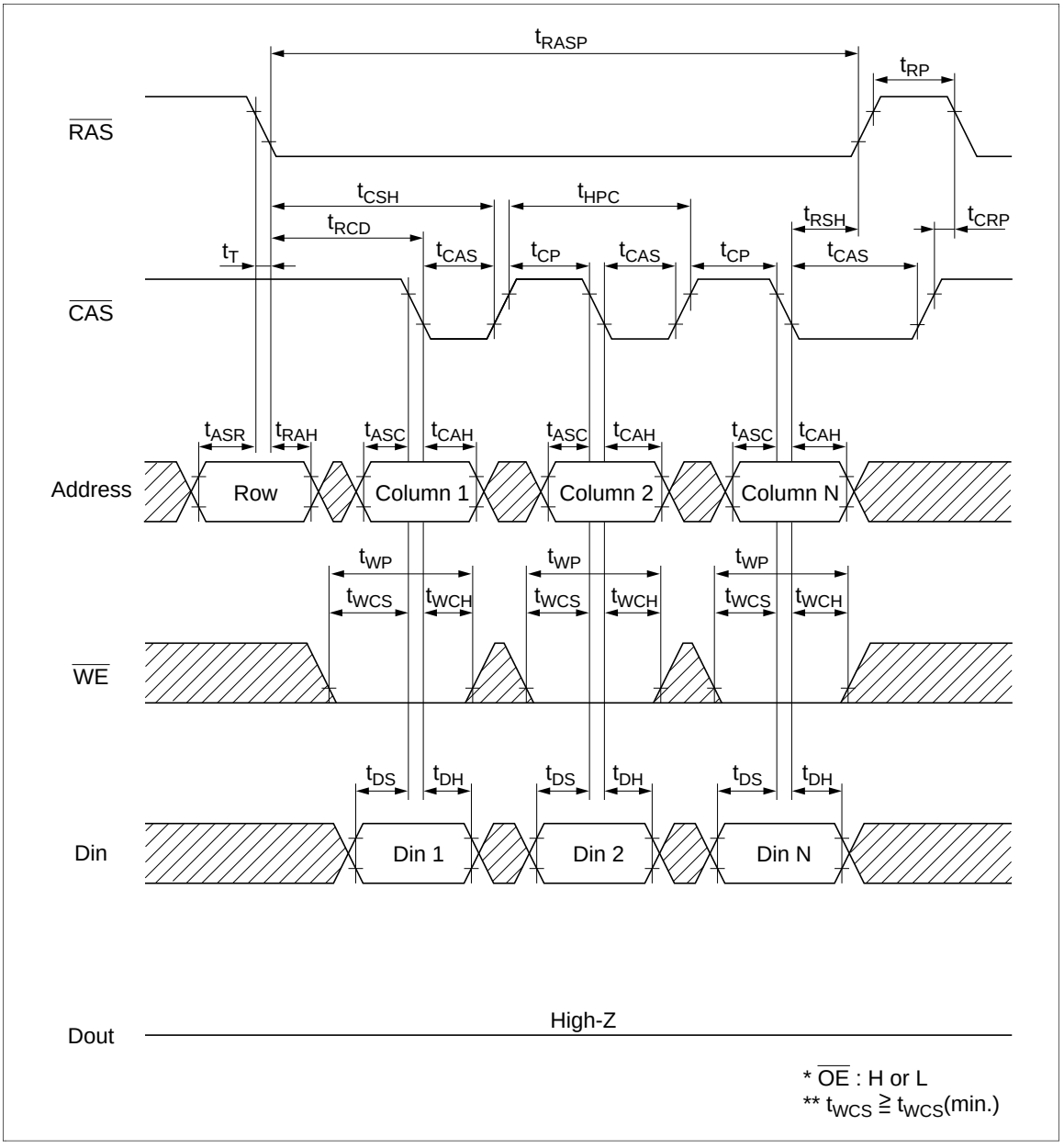
Hidden Refresh Cycle



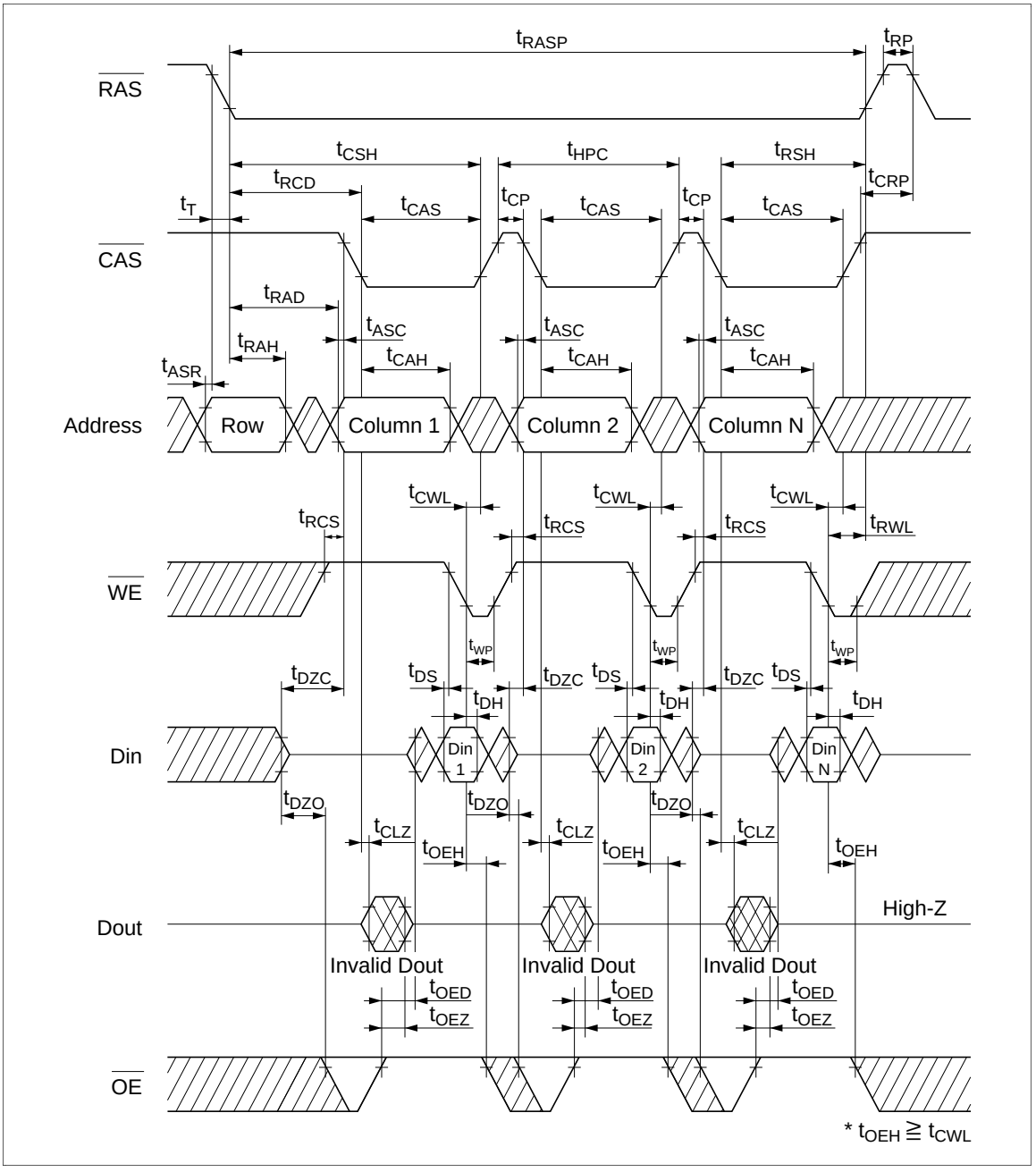
EDO Page Mode Read Cycle


RAS
CAS
WE
Address
Din
OE
Dout
Row
Column 1
Column 2
Column 3
Column 4
High-Z
Dout 1
Dout 2
Dout 2
Dout 3
Dout 4
tRP
tRASP
tHPC
tT
tCRP
tCSH
tCP
tCPRH
tRSH
tCAS
tRCHC
tRCHR
tRRH
tRCH
tRCS
tWP
tRAL
tWED
tRAH
tCAH
tASR
tASC
tRDD
tCAL
tDZC
tCDD
tDZO
tCOL
tCOP
tOED
tOFR
tOHR
tOEA
tCPA
tCAC
tAA
tOEZ
tWEZ
tOHO
tRAC
tDOH
tOFF
tOH

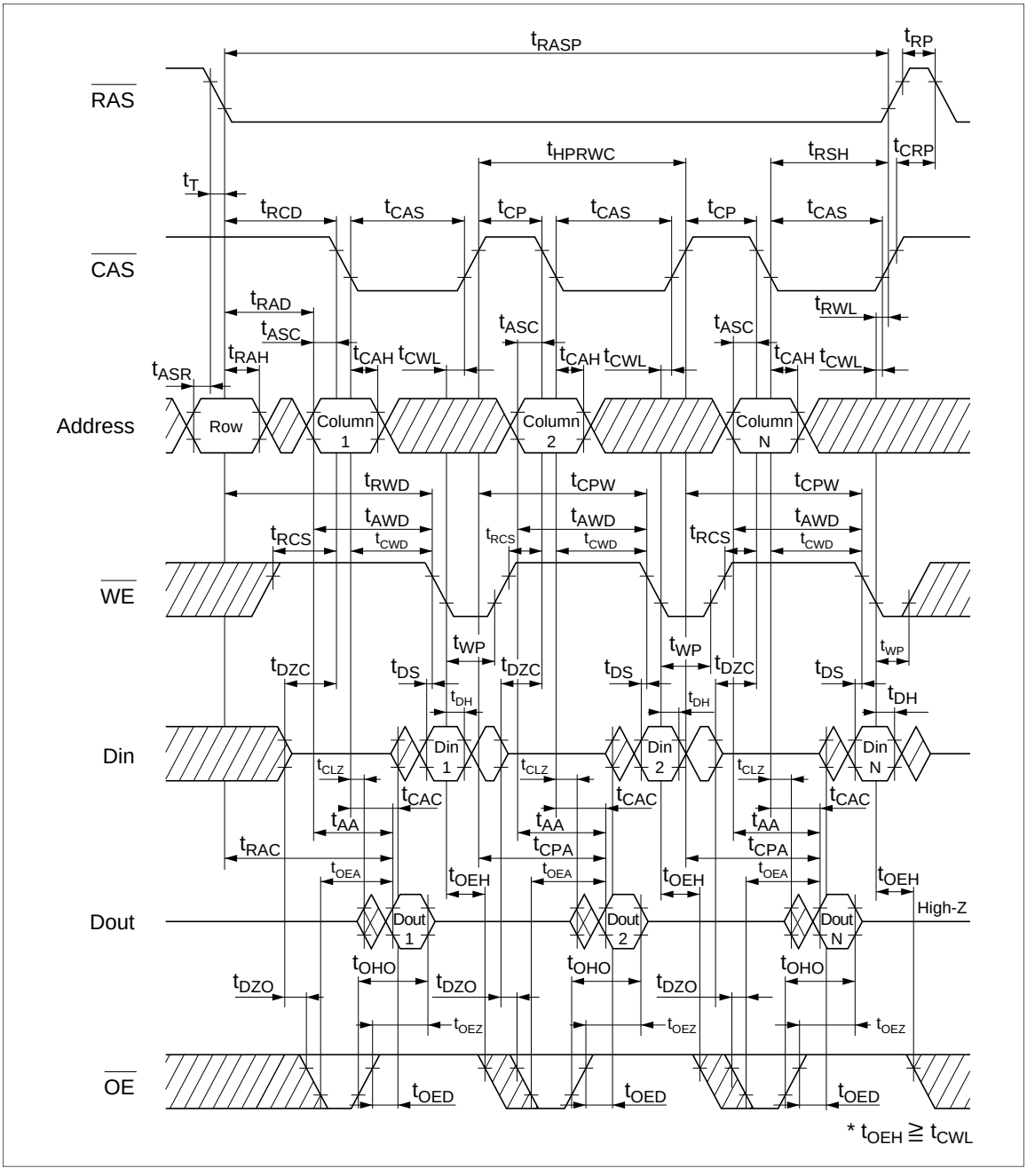
EDO Page Mode Eary Write Cycle



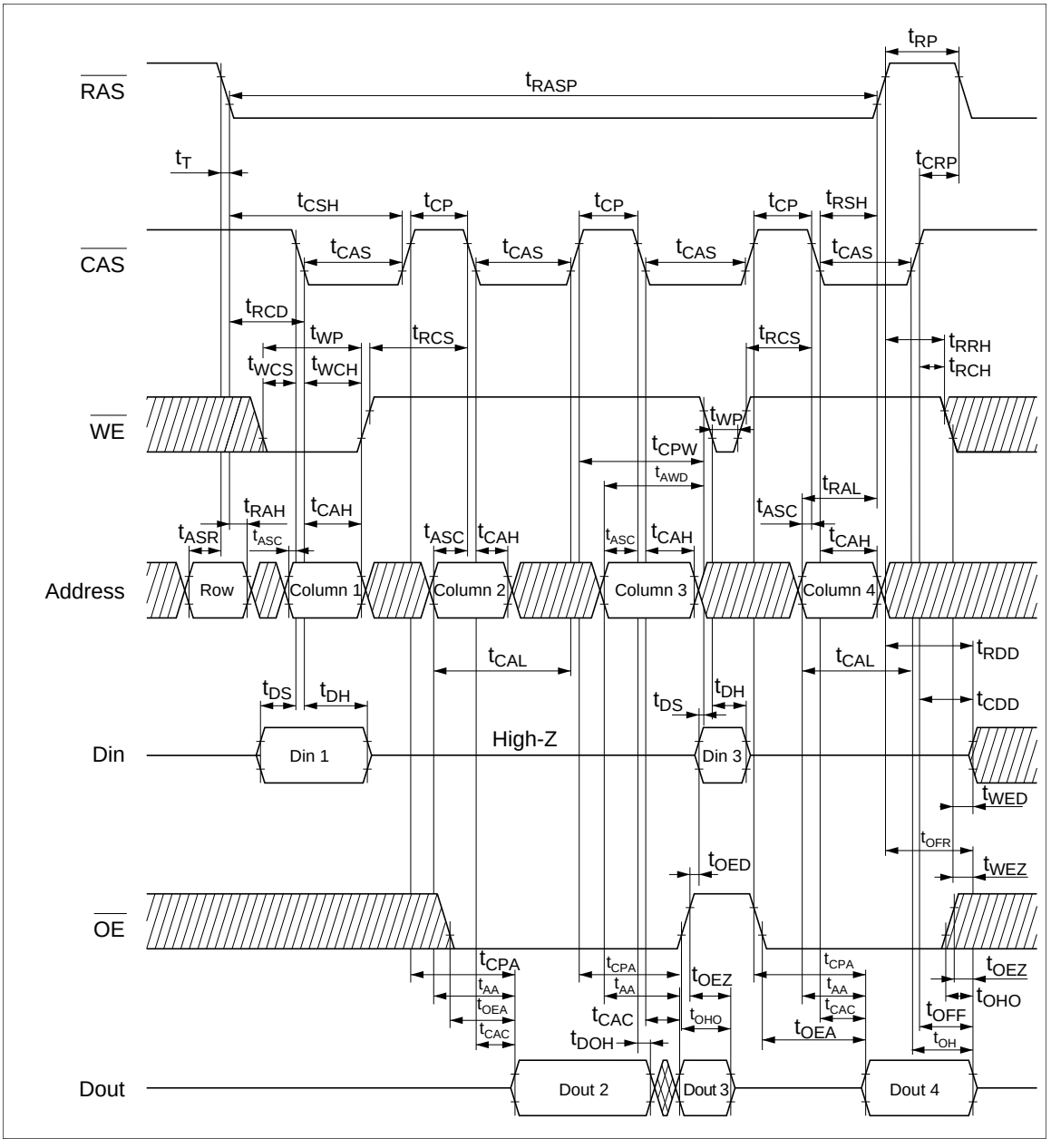
EDO Page Mode Delayed Write Cycle



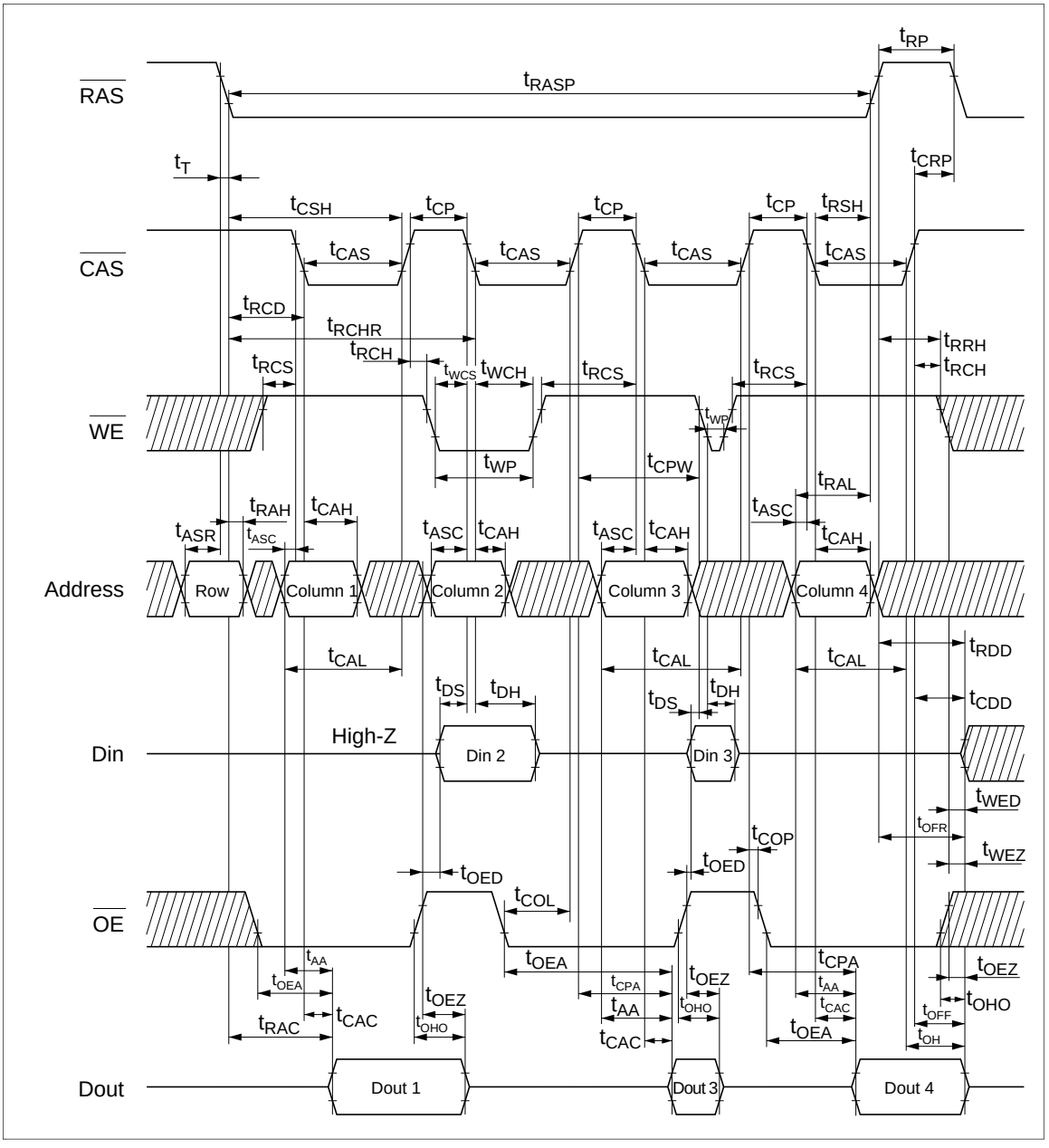
EDO Page Mode Read-Modify-Write Cycle



EDO Page Mode Mix Cycle (1)

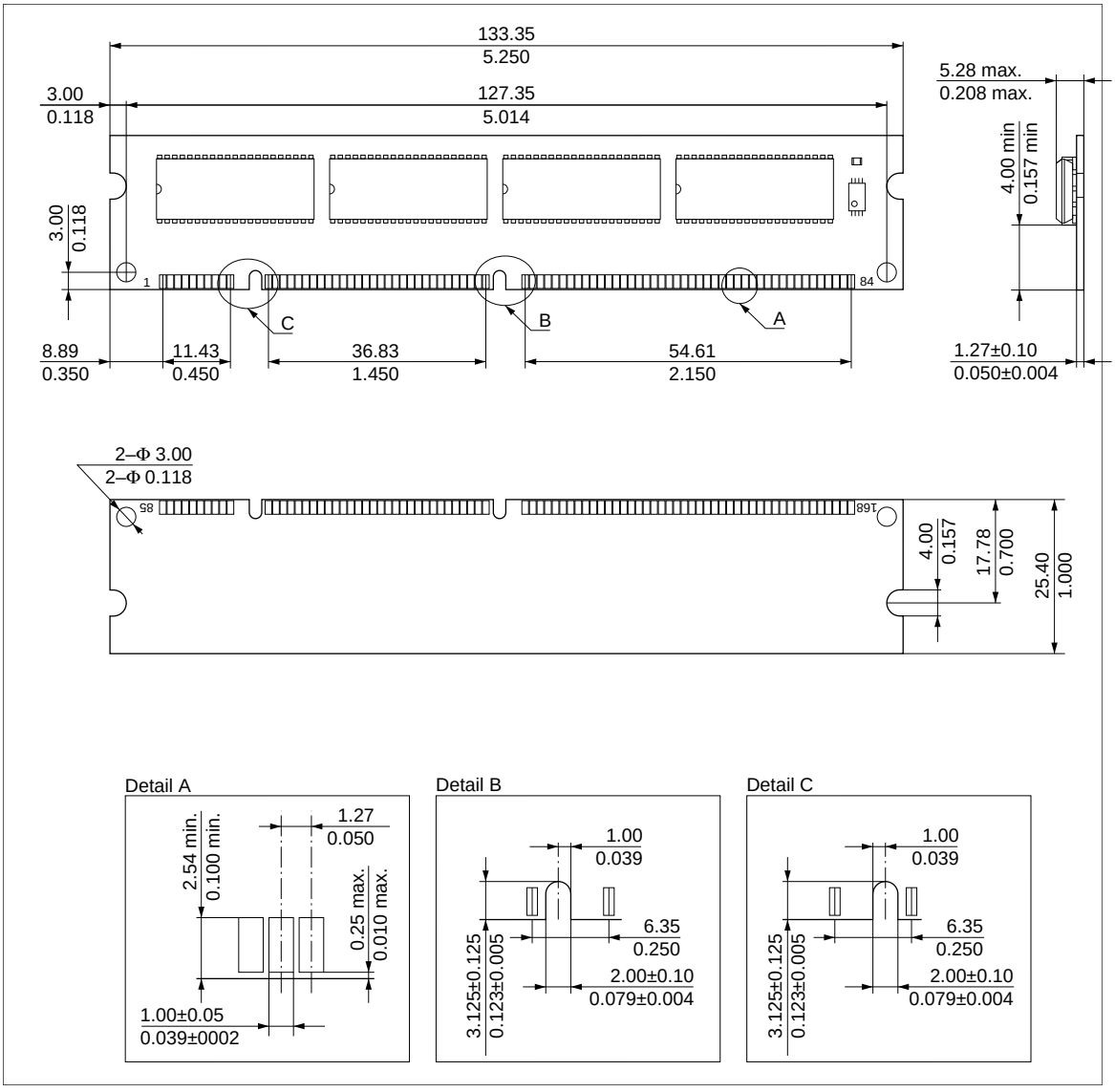


EDO Page Mode Mix Cycle (2)



Physical Outline

Unit: mm/inch



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Feb. 21, '96	Initial issue	S. Tsukui	K. Tsuneda