
HB56A472E-5/6/7

4,194,304-word $\times$ 72-bit High Density Dynamic RAM Module

HITACHI

ADE-203-744A (Z)

Rev. 1.0

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Description

The HB56A472E belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56A472E is a 4M $\times$ 72 dynamic RAM module, mounted 18 pieces of 16-Mbit DRAM (HM5116400) sealed in TSOP package and 2 piece of 16-bit BiCMOS line driver (74ABT16244) sealed in TSSOP package. An outline of the HB56A472E is 168-pin socket type package (dual lead out). Therefore, the HB56A472E makes high density mounting possible without surface mount technology. The HB56A472E provides common data inputs and outputs. Decoupling capacitors are mounted on the module board.

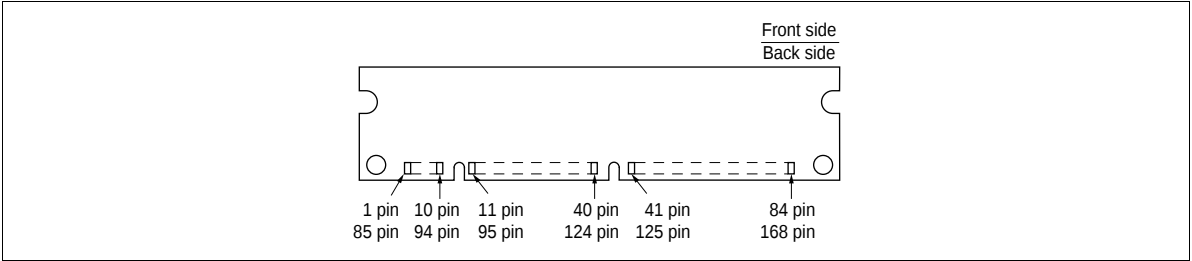
Features

- 168-pin socket type package (Dual lead out)
 - Outline: 133.35 mm (Length) $\times$ 25.40 mm (Height) $\times$ 4.00 mm (Thickness)
 - Lead pitch: 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time: $t_{\text{RAC}} = 50/60/70$ ns (max)
 $t_{\text{CAC}} = 18/20/23$ ns (max)
- Low power dissipation
 - Active mode: 8.84/7.90/6.95 W (max)
 - Standby mode (TTL): 525 mW (max)
(CMOS): 431 mW (max)
- Buffered input except $\overline{\text{RAS}}$ and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- JEDEC standard outline buffered 8-byte DIMM
- Fast page mode capability
- 4,096 refresh cycles: 64 ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56A472E-5	50 ns	168-pin dual lead out socket type	Gold
HB56A472E-6	60 ns		
HB56A472E-7	70 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ36	128	NC
3	DQ1	45	$\overline{\text{RE2}}$	87	DQ37	129	NC
4	DQ2	46	$\overline{\text{CE4}}$	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	V _{CC}	48	$\overline{\text{WE2}}$	90	V _{CC}	132	$\overline{\text{PDE}}$
7	DQ4	49	V _{CC}	91	DQ40	133	V _{CC}
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	V _{CC}	101	DQ49	143	V _{CC}
18	V _{CC}	60	DQ24	102	V _{CC}	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	V _{SS}	65	DQ25	107	V _{SS}	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	V _{CC}	68	V _{SS}	110	V _{CC}	152	V _{SS}
27	$\overline{\text{WE0}}$	69	DQ28	111	NC	153	DQ64
28	$\overline{\text{CE0}}$	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	$\overline{\text{RE0}}$	72	DQ31	114	NC	156	DQ67
31	$\overline{\text{OE0}}$	73	V _{CC}	115	NC	157	V _{CC}
32	V _{SS}	74	DQ32	116	V _{SS}	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70

HB56A472E-5/6/7

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	V _{CC}	82	PD7	124	V _{CC}	166	PD8
41	NC	83	ID0 (V _{SS})	125	NC	167	ID1 (V _{SS})
42	NC	84	V _{CC}	126	B0	168	V _{CC}

Pin Description

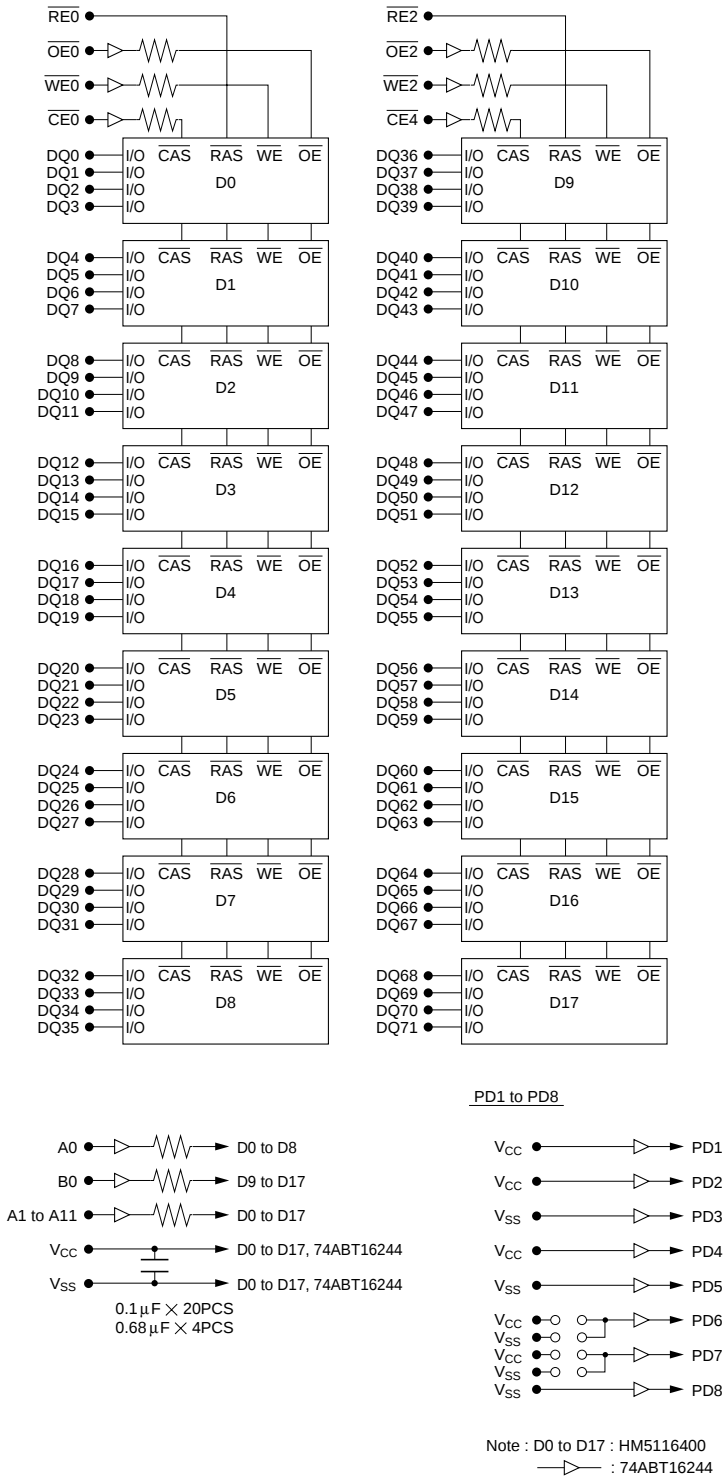
Pin name	Function
A0 to A11, B0	Address input — Row address : A0 to A11, B0 — Column address : A0 to A9, B0 — Refresh address : A0 to A11, B0
DQ0 to DQ71	Data-in/data-out
RE0, RE2	Row address strobe ($\overline{\text{RAS}}$)
CE0, CE4	Column address strobe ($\overline{\text{CAS}}$)
WE0, WE2	Read/Write enable
OE0, OE2	Output enable
V _{CC}	Power supply
V _{SS}	Ground
PD1 to PD8	Presence detect
ID0, ID1	ID bit
PDE	Presence detect enable
NC	No connection

Presence Detect Pin Assignment

Pin name	Pin No.	PDE = Low			PDE = High
		50 ns	60 ns	70 ns	All
PD1	79	1	1	1	High-Z
PD2	163	1	1	1	High-Z
PD3	80	0	0	0	High-Z
PD4	164	1	1	1	High-Z
PD5	81	0	0	0	High-Z
PD6	165	0	1	0	High-Z
PD7	82	0	1	1	High-Z
PD8	166	0	0	0	High-Z

Note: 1: High level (driver output)
0: Low level (driver output)

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	19	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−0.5	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	1684	—	1504	—	1324	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	100	—	100	—	100	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z	
		—	82	—	82	—	82	mA	CMOS interface RAS, CAS ≥ V _{CC} − 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	1684	—	1504	—	1324	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	154	—	154	—	154	mA	RAS = V _{IH} , CAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	1684	—	1504	—	1324	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	1504	—	1324	—	1144	mA	t _{PC} = min	1, 3
Input leakage current	I _{LI}	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 5.5 V	
Output leakage current	I _{LO}	−10	10	−10	10	−10	10	μA	0 V ≤ Vout ≤ 5.5 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while RAS = V_{IL}.
3. Address can be changed once or less while CAS = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	20	pF	1
Input capacitance (CAS, WE, OE)	C _{I2}	—	20	pF	1
Input capacitance (RAS)	C _{I3}	—	78	pF	1
I/O capacitance (DQ)	C _{I/O}	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. CAS = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) ^{*1, *2, *18, *19}

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.4 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90	—	110	—	130	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	7	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	13	10000	15	10000	18	10000	ns	
Row address setup time	t _{ASR}	5	—	5	—	5	—	ns	
Row address hold time	t _{RAH}	7	—	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	7	—	10	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	17	32	20	40	20	47	ns	3
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	12	20	15	25	15	30	ns	4
$\overline{\text{RAS}}$ hold time	t _{RSH}	18	—	20	—	23	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	50	—	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ to Din delay time	t _{OED}	18	—	20	—	23	—	ns	5
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ delay time from Din	t _{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	7
Refresh period (4,096 cycles)	t _{REF}	—	64	—	64	—	64	ms	

Read Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	18	—	20	—	23	ns	9, 10, 17
Access time from address	t_{AA}	—	30	—	35	—	40	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	18	—	20	—	23	ns	9, 20
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	25	—	30	—	35	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	2	—	2	—	2	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	18	—	20	—	20	ns	13
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	18	—	20	—	20	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	18	—	20	—	23	—	ns	5

Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	7	—	10	—	15	—	ns	
Write command pulse width	t_{WPP}	7	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	18	—	20	—	23	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	13	—	15	—	18	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	12	—	15	—	20	—	ns	15

Read-Modify-Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time t_{RWC}		131	—	155	—	181	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time t_{RWD}		73	—	85	—	98	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time t_{CWD}		36	—	40	—	46	—	ns	14
Column address to $\overline{WE}$ delay time t_{AWD}		48	—	55	—	63	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$ t_{OEh}		13	—	15	—	18	—	ns	

Refresh Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle) t_{CSR}		10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle) t_{CHR}		7	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle) t_{WRP}		5	—	5	—	5	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle) t_{WRH}		7	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time t_{RPC}		5	—	5	—	5	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time t_{PC}		35	—	40	—	45	—	ns	
Fast page mode $\overline{RAS}$ pulse width t_{RASP}		—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge t_{CPA}		—	35	—	40	—	45	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge t_{CPRH}		35	—	40	—	45	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode read-modify-write cycle time	t_{PRWC}	76	—	85	—	96	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	53	—	60	—	68	—	ns	14

- Notes:
1. AC measurements assume $t_r = 5$ ns.
 2. An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ -only refresh cycle or $\overline{CAS}$ -before- $\overline{RAS}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ -before- $\overline{RAS}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
 10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
 11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. t_{OFF} (max) and t_{OEZ} (max) is define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min) or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referred to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
 16. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
 17. Access time is determined by the longest among t_{AA} , t_{CAC} or t_{CPA} .
 18. In delayed write or read-modify-write cycle, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OE H} \geq t_{CWL}$, the DQ pin will remain open circuit (high impedance); if $t_{OE H} \leq t_{CWL}$, invalid data will be out at each DQ.
 19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 20. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally causes large V_{CC} / V_{SS} line noise, which causes to degrade V_{IH} min / V_{IL} max level.

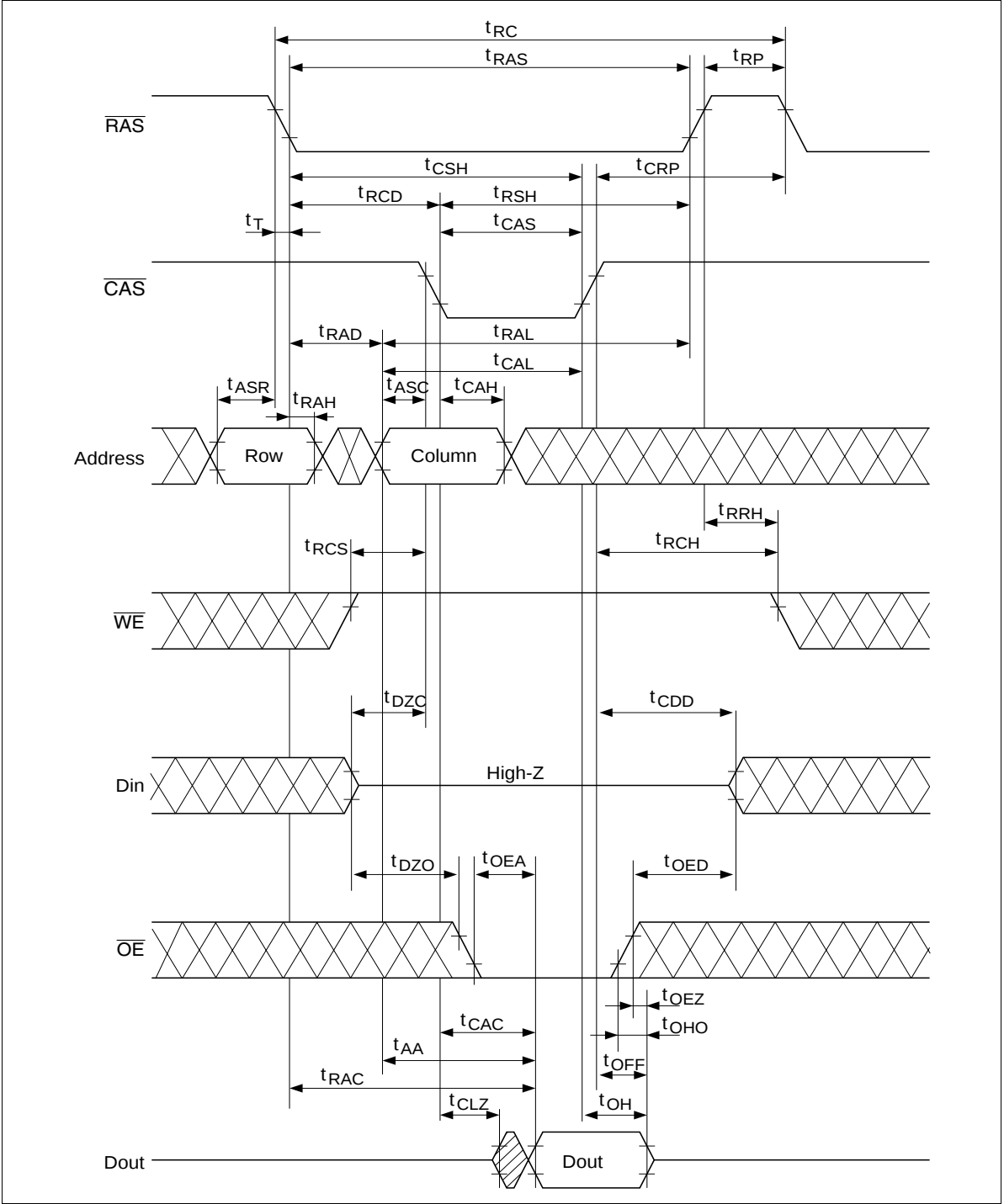
21. XXX: H or L (H: $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$, L: $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$)

//////: Invalid Dout

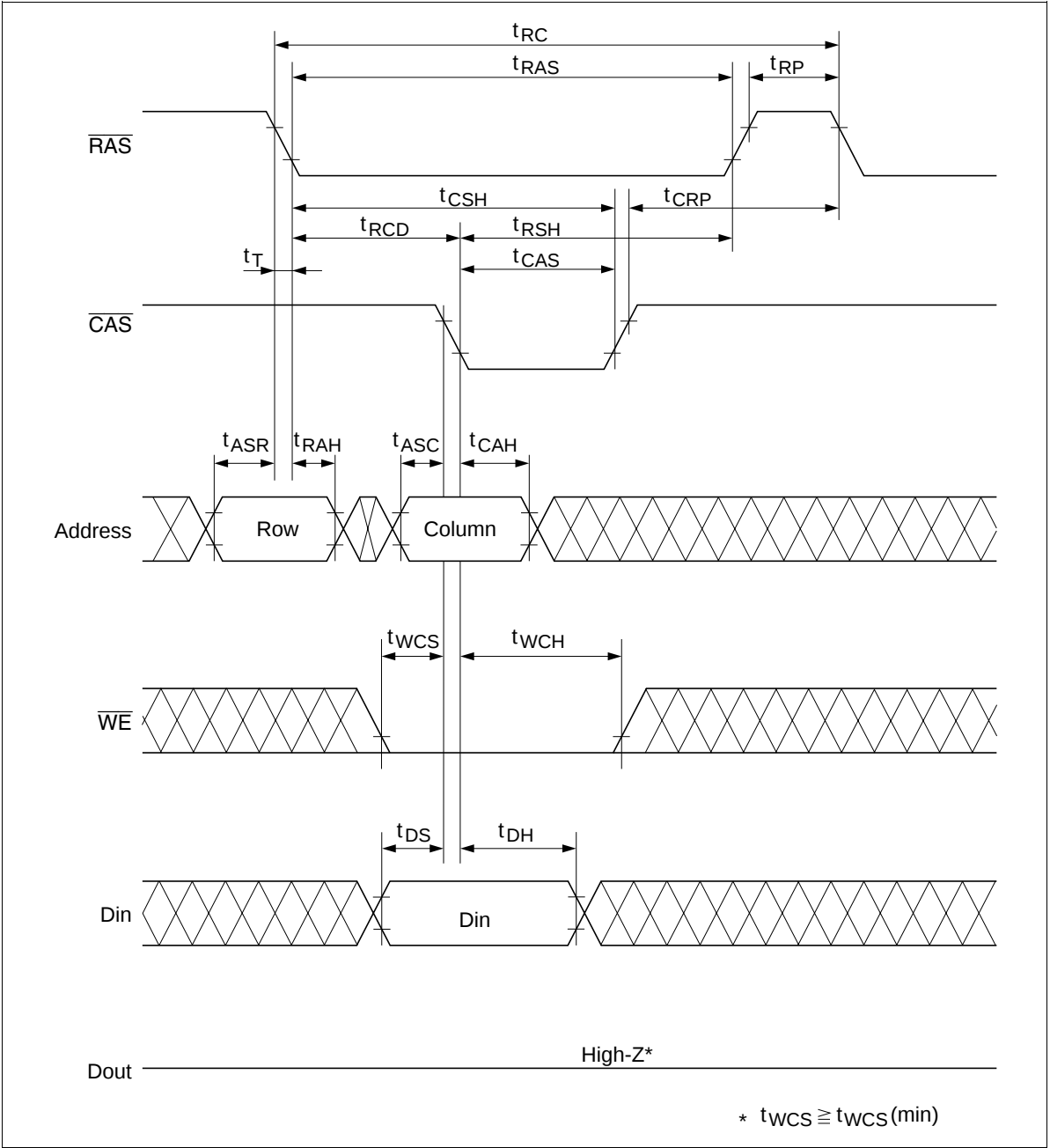
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Timing Waveforms*21

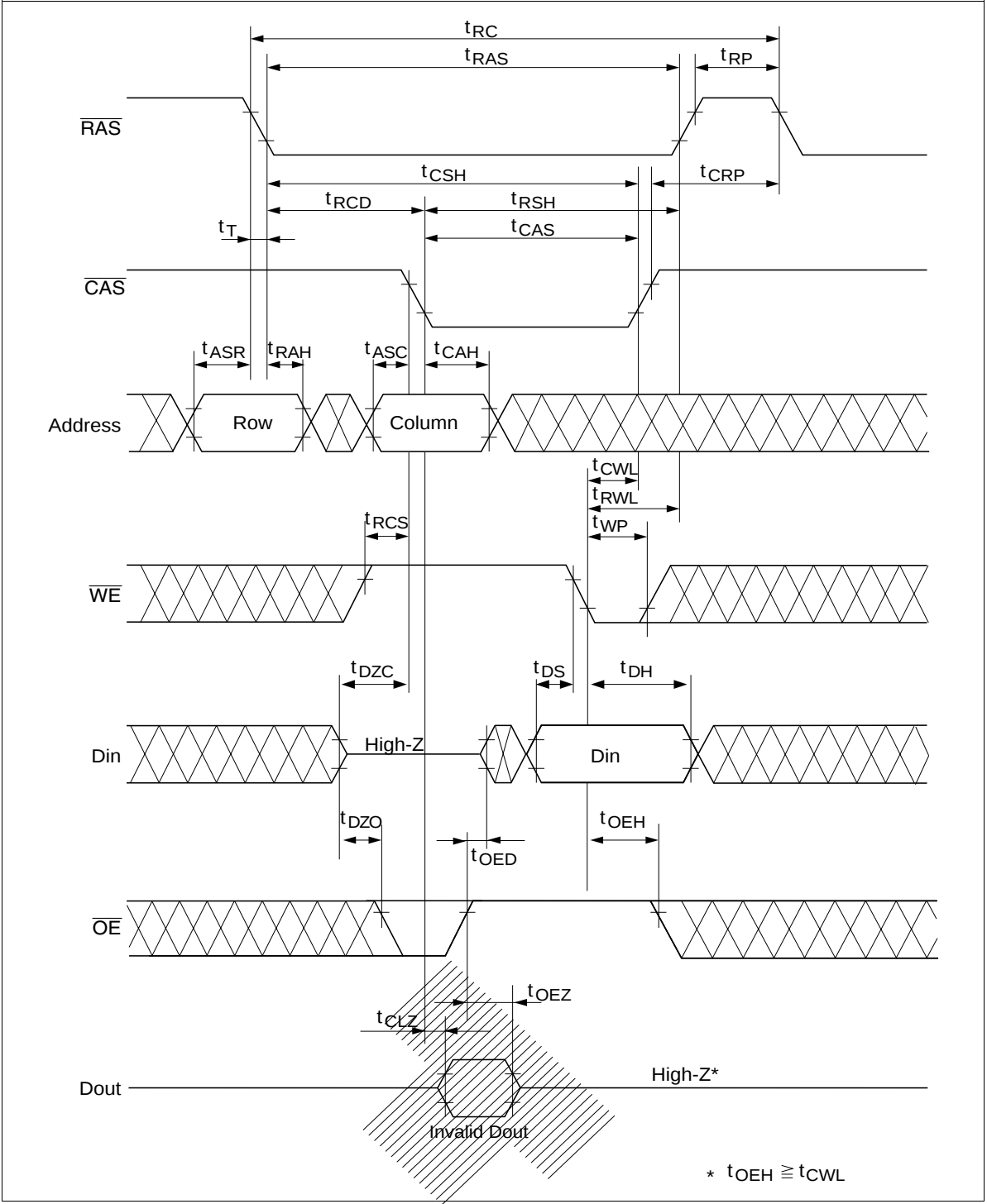
Read Cycle



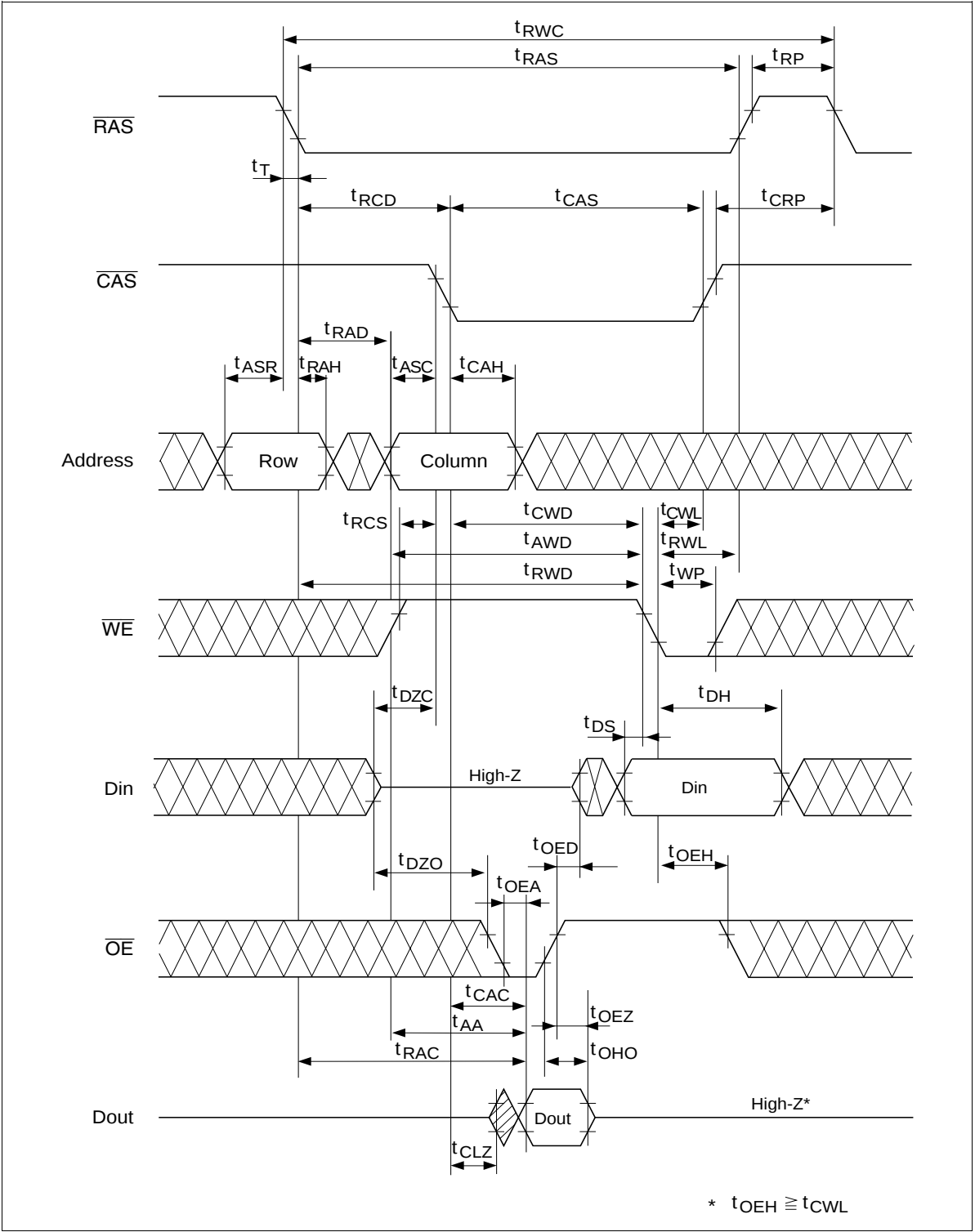
Early Write Cycle



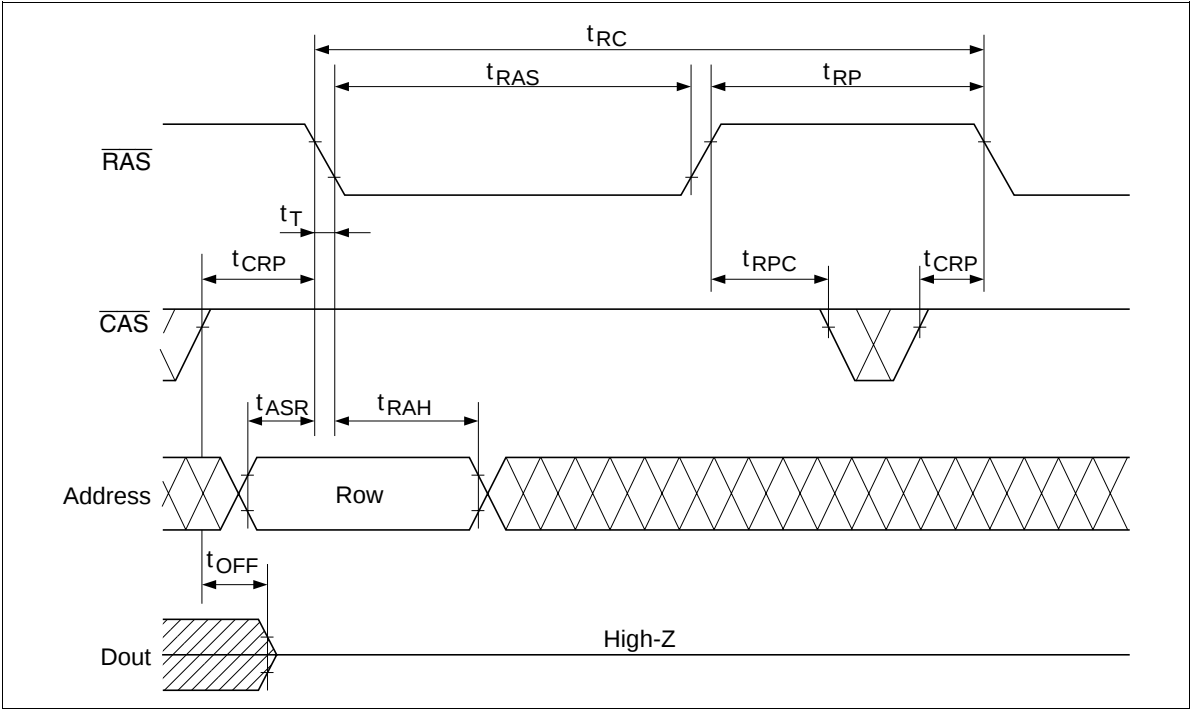
Delayed Write Cycle⁴⁸



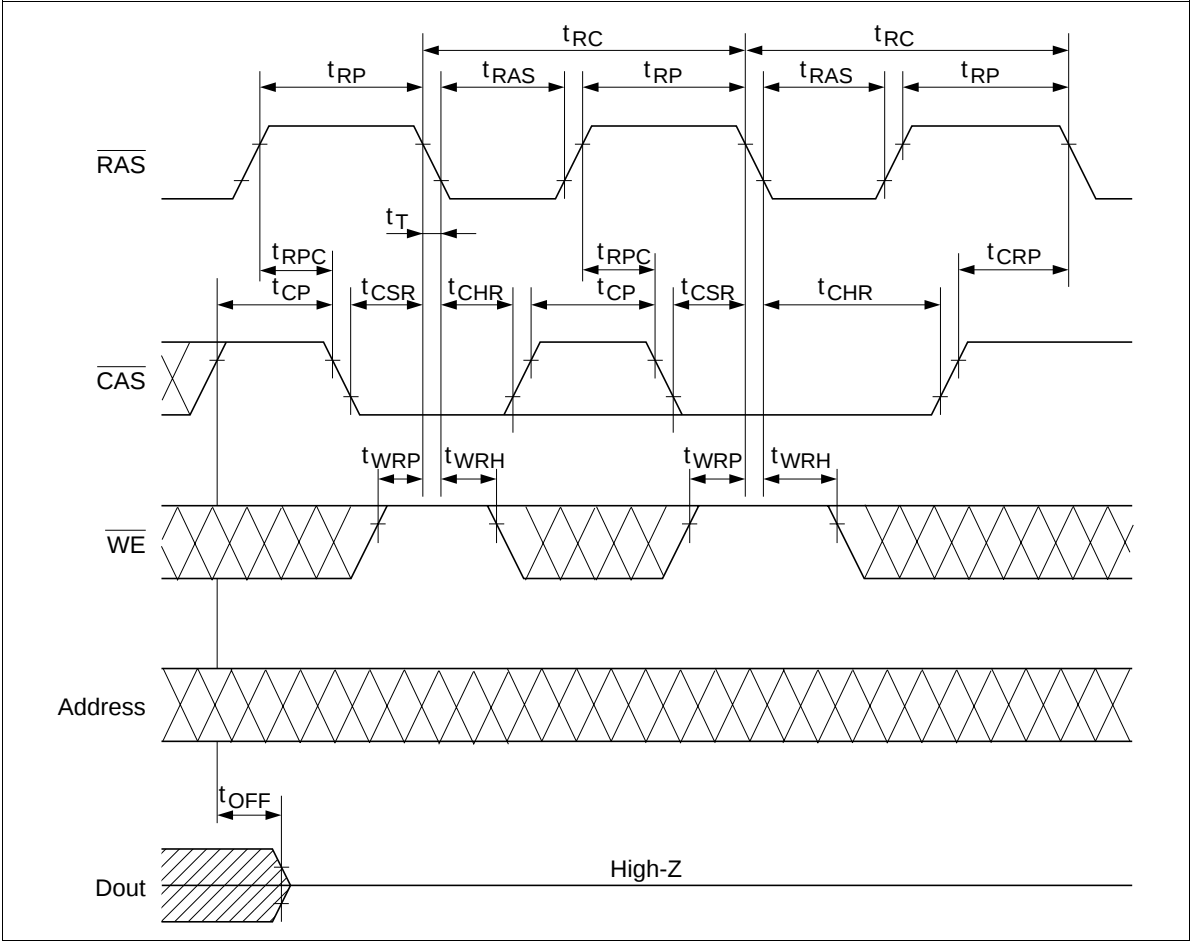
Read-Modify-Write Cycle*18



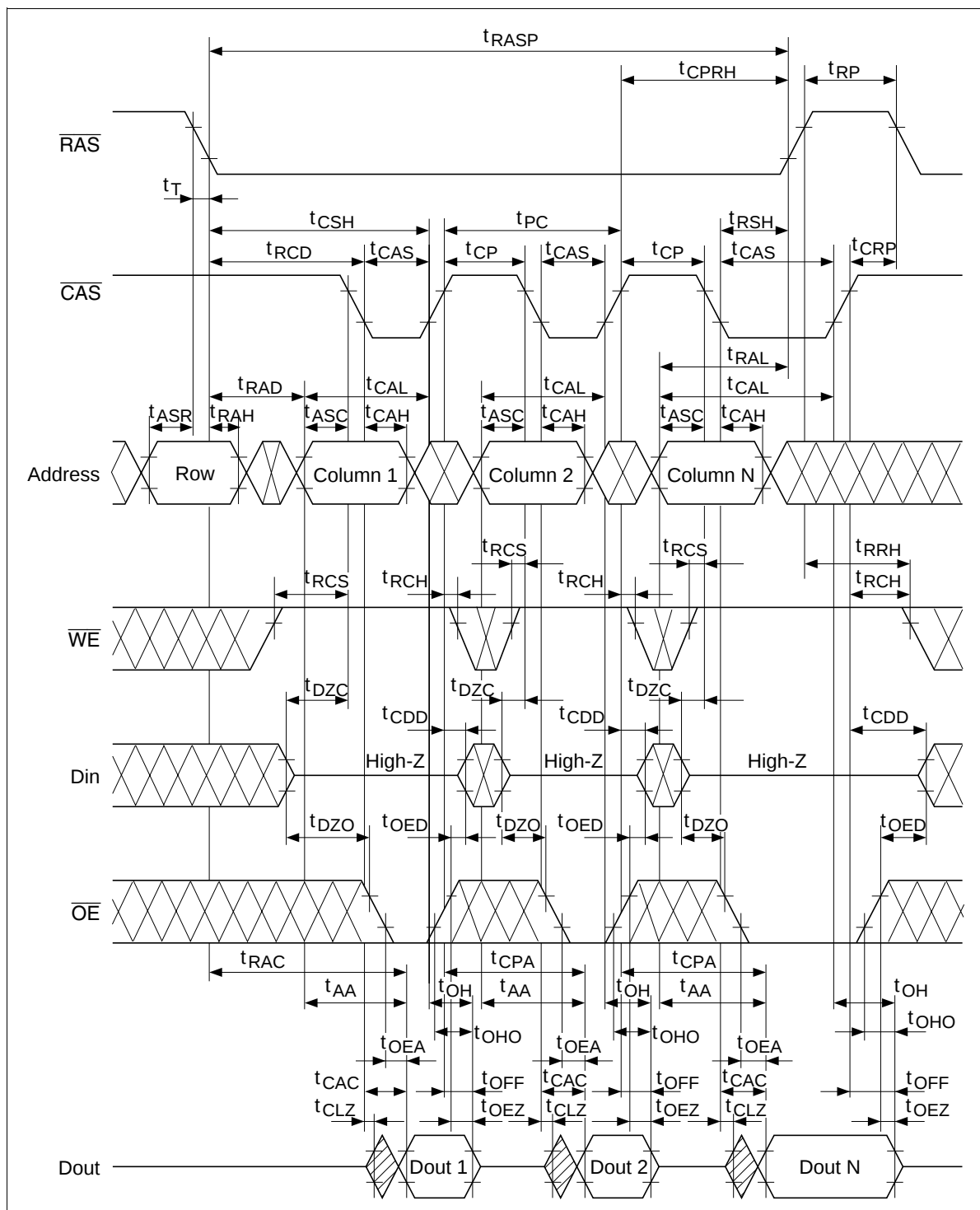
RAS-Only Refresh Cycle



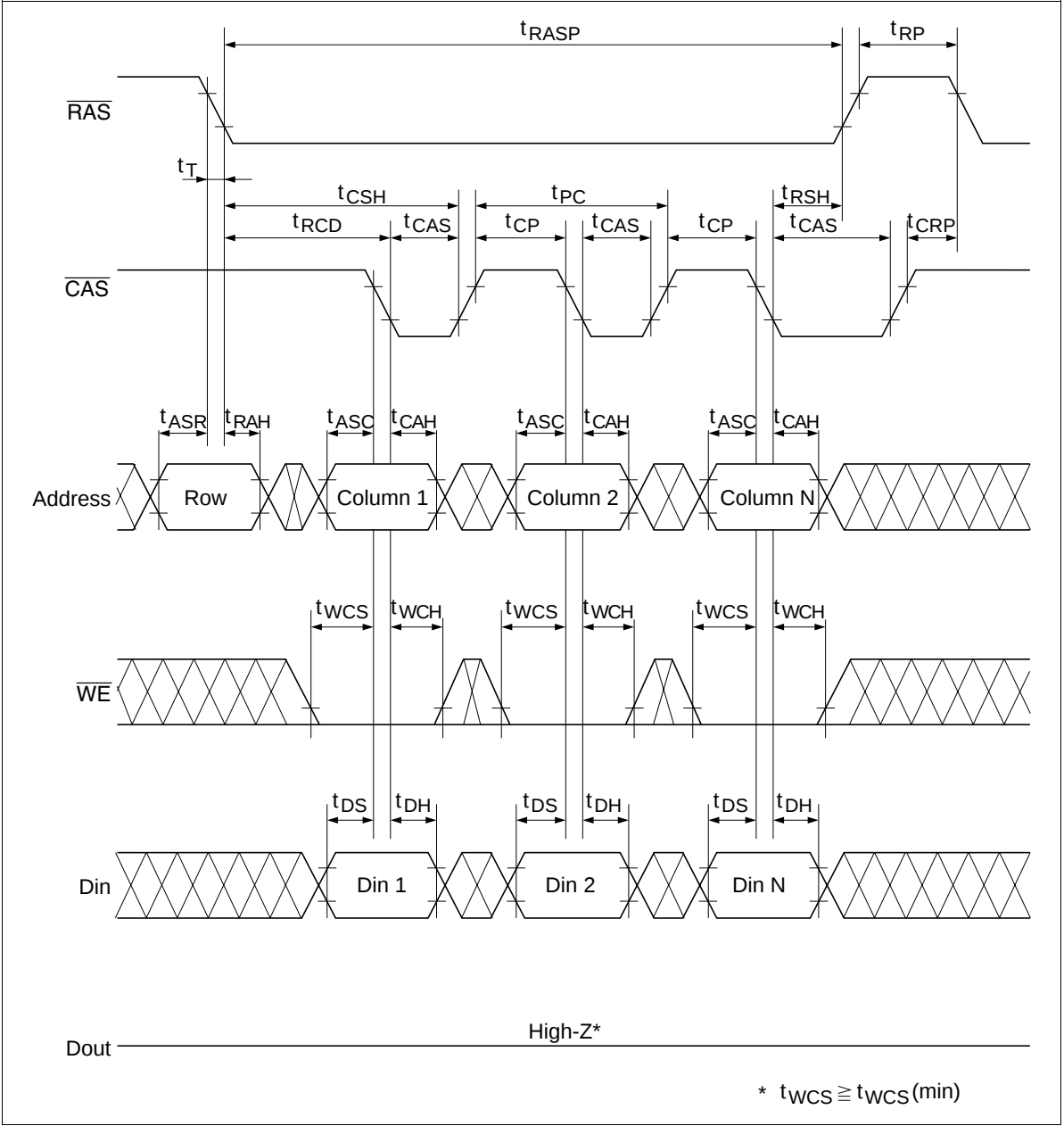
CAS-Before-RAS Refresh Cycle



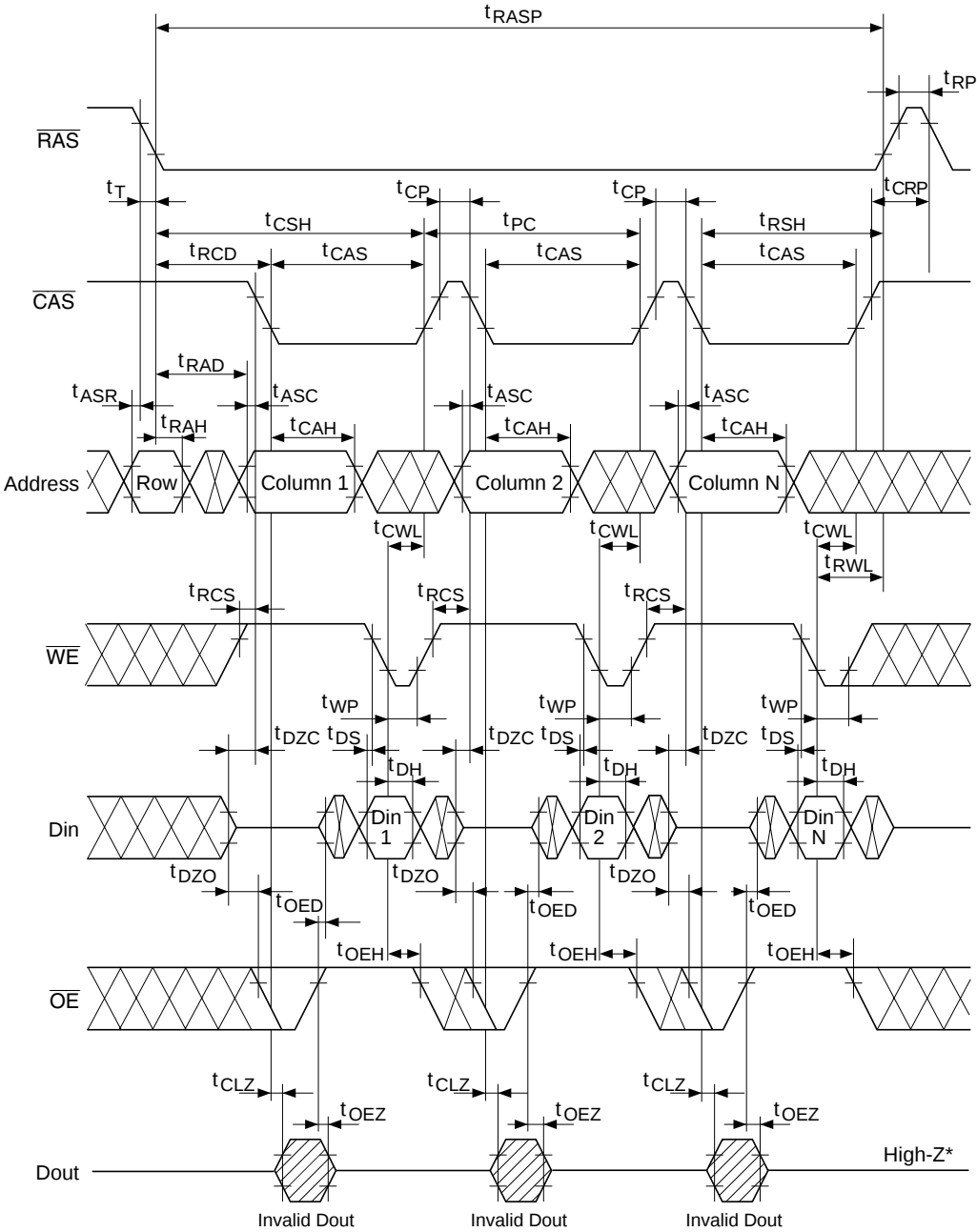
Fast Page Mode Read Cycle



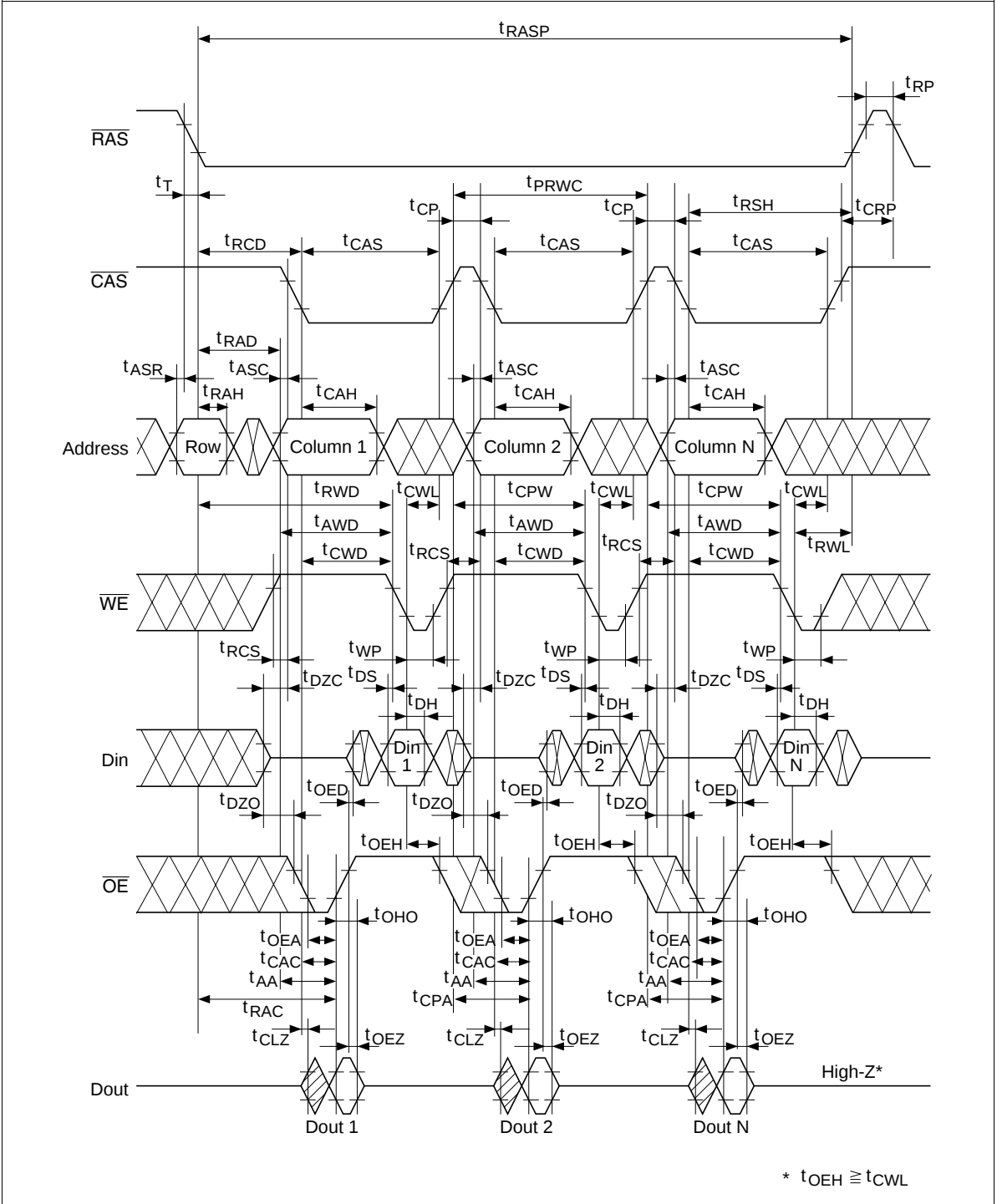
Fast Page Mode Early Write Cycle



Fast Page Mode Delayed Write Cycle*¹⁸

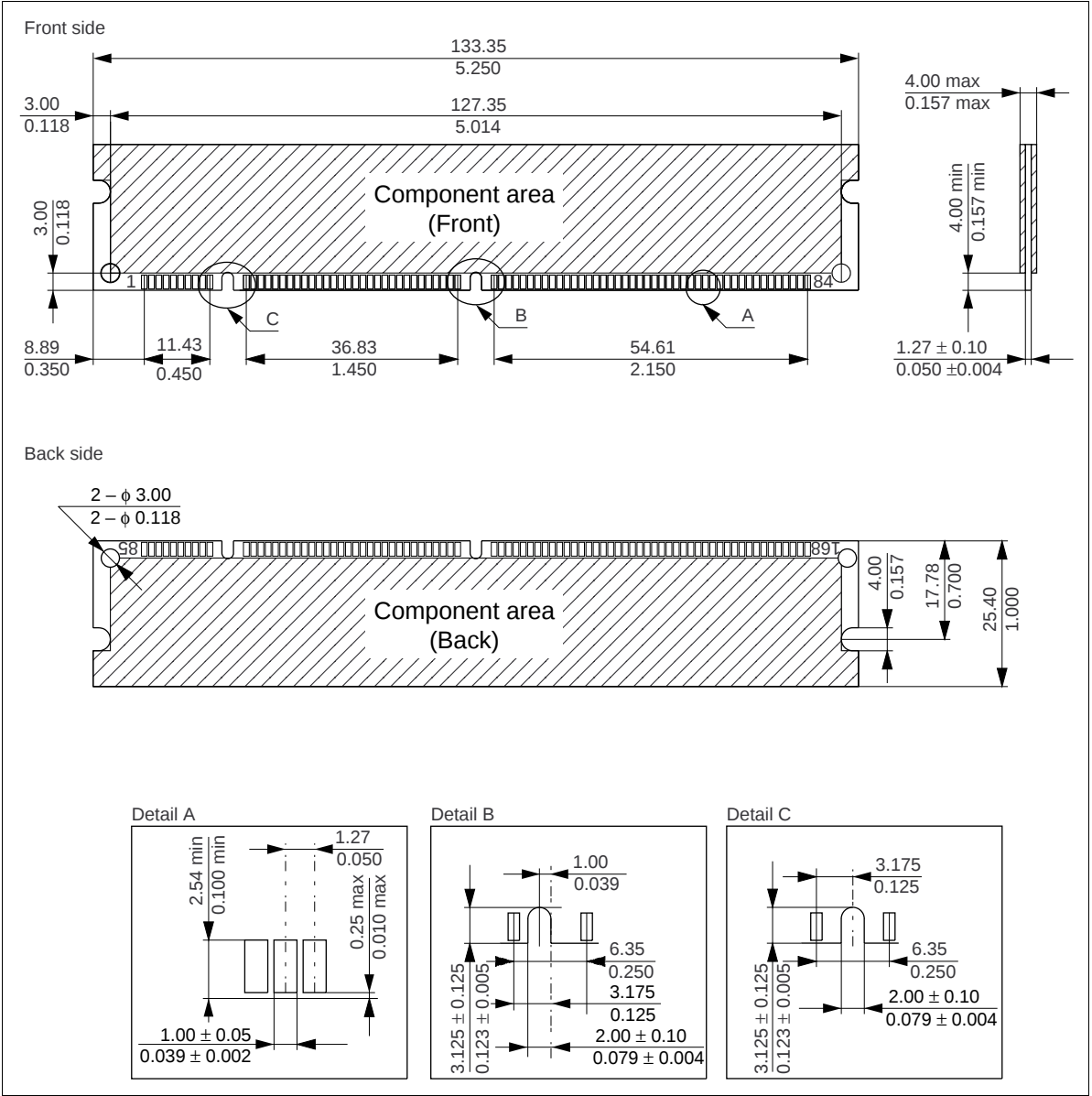


Fast Page Mode Read-Modify-Write Cycle*¹⁸



Physical Outline

Unit: mm/inch



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