LT5500

1.8GHz to 2.7GHz Receiver Front End

December 2001

FEATURES

- **1.8V to 5.25V Supply**
- **Dual LNA Gain Setting: +13.5dB/–14dB at 2.5GHz**
- **Double-Balanced Mixer**
- **Internal LO Buffer**
- LNA Input Internally Matched
- Low Supply Current: 23mA
- Low Shutdown Current: 2μA
- 24-Lead Narrow SSOP Package

APPLICATIONS

- IEEE 802.11 and 802.11b DSSS and FHSS
- High Speed Wireless LAN
- Wireless Local Loop

DESCRIPTION

The LT®5500 is a receiver front end IC designed for low voltage operation and is compatible with the LTC family of WLAN products. The chip contains a low noise amplifier (LNA), a Mixer and an LO buffer. The IC is designed to operate over a power supply voltage range from 1.8V to 5.25V.

The LNA can be set to either high gain or low gain mode. At 2.5GHz, the high gain mode provides 13.5dB gain and a noise figure (NF) of 4dB. The LNA in low gain mode provides –14dB gain and an IIP3 of +8dBm at 2.5GHz.

The mixer has 5dB of conversion gain and an IIP3 of –2.5dBm at 2.5GHz, with –10dBm LO input power.

TYPICAL APPLICATION

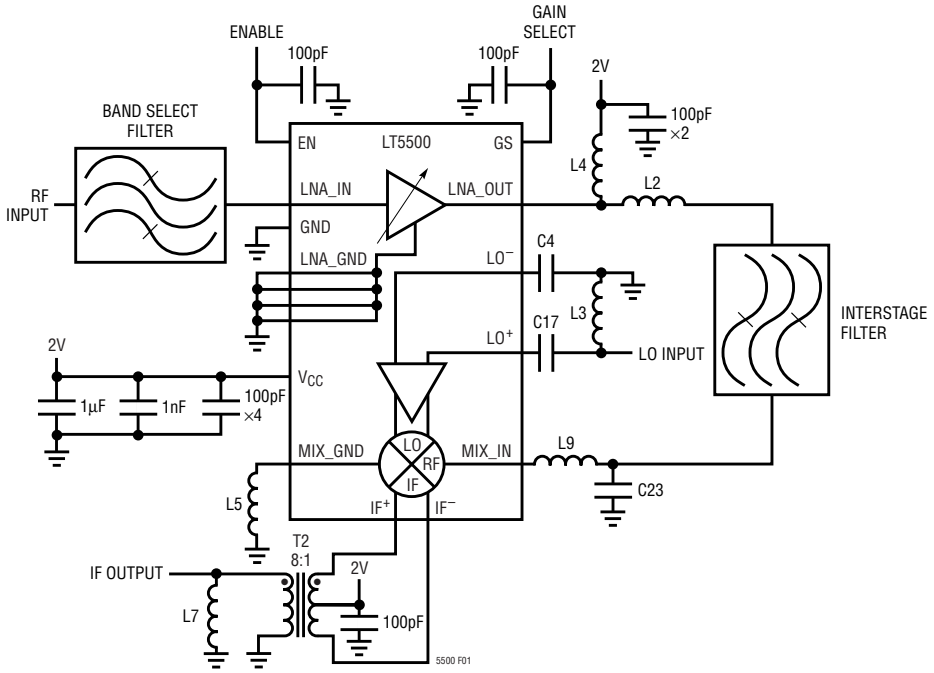
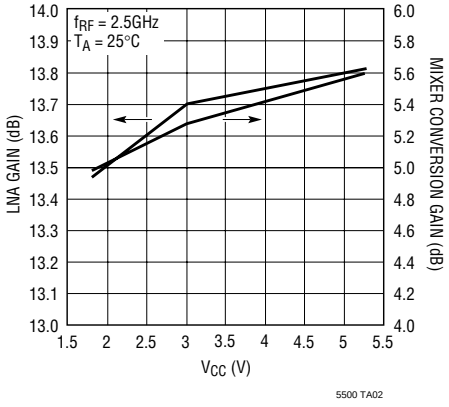


Figure 1. 2.5GHz Receiver. Interstage Filter is Optional

LNA Gain (High Gain Mode) and Mixer Conversion Gain

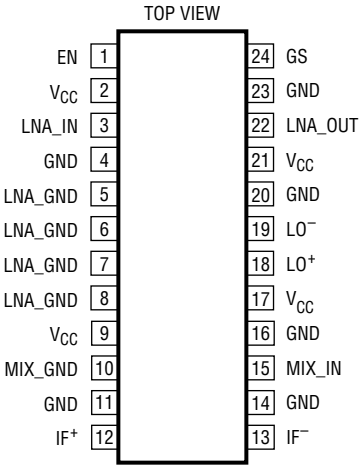


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage 5.5V
LNA RF Input Power 5dBm
Mixer RF Input Power 10dBm
LO Input Power (Note 2) 10dBm
All Other Pins 5.5V
Operating Ambient
Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LT5500EGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

(Test circuit shown in Figure 3 for 1.8GHz application) V_{CC} = 3V DC, LNA: f_{LNA_IN} = 1.8GHz, Mixer: f_{MIX_IN} = 1.8GHz, f_{LO} = 1.52GHz, P_{LO} = –10dBm, T_A = 25°C, unless otherwise noted. (Notes 3, 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LNA High Gain: EN = 1.35V, GS = 1.35V						
	Frequency Range (Note 3)			1.8 to 2.7		GHz
	Forward Gain		15.5	18.5		dB
	Reverse Gain (Isolation)			–39		dB
	Noise Figure	Terminated 50Ω Source		2.5		dB
	Input Return Loss	No External Matching		10.5		dB
	Output Return Loss	With External Matching		15		dB
	Input 1dB Compression			–24		dBm
	Input 3rd Order Intercept	Two Tone Test, Δf = 2MHz	–18	–12		dBm
LNA Low Gain: EN = 1.35V, GS = 0.3V						
	Frequency Range (Note 4)			1.8 to 2.7		GHz
	Forward Gain		–13	–10		dB
	Reverse Gain (Isolation)			–34		dB
	Noise Figure			16.5		dB
	Input 1dB Compression			0		dBm
	Input 3rd Order Intercept	Two Tone Test, Δf = 2MHz	4.5	9		dBm
Mixer: EN = 1.35V, GS = 1.35V						
	RF Frequency Range (Note 4)			1.8 to 2.7		GHz
	Conversion Gain		5.5	8.5		dB
	SSB Noise Figure	Terminated 50Ω Source		7.5		dB
	Input P1dB			–13		dBm
	Input 3rd Order Intercept	Two Tone Test, Δf = 2MHz	–6	–2.5		dBm

ELECTRICAL CHARACTERISTICS

(Test circuit shown in Figure 3 for 1.8GHz application) V_{CC} = 3V DC, LNA: f_{LNA_IN} = 1.8GHz, Mixer: f_{MIX_IN} = 1.8GHz, f_{LO} = 1.52GHz, P_{LO} = –10dBm, T_A = 25°C, unless otherwise noted. (Notes 3, 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	LO Frequency Range (Note 4)			1.35 to 3.15		GHz
	IF Frequency Range (Note 3)			200 to 450		MHz
	LO-IF Isolation			36		dB
	LO-RF Isolation			36		dB
	RF-LO Isolation			40		dB

(Test circuit shown in Figure 3 for 2.5GHz application) V_{CC} = 3V DC, LNA: f_{LNA_IN} = 2.5GHz, Mixer: f_{MIX_IN} = 2.5GHz, f_{LO} = 2.22GHz, P_{LO} = –10dBm, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LNA High Gain: EN = 1.35V, GS = 1.35V						
	Forward Gain			13.5		dB
	Reverse Gain (Isolation)			–35		dB
	Noise Figure	Terminated 50Ω Source		4		dB
	Input Return Loss	No External Matching		12		dB
	Output Return Loss	With External Matching		15		dB
	Input 1dB Compression			–15		dBm
	Input 3rd Order Intercept	Two Tone Test, Δf = 2MHz		–3.5		dBm
LNA Low Gain: EN = 1.35V, GS = 0.3V						
	Forward Gain			–14		dB
	Reverse Gain (Isolation)			–39		dB
	Noise Figure			19		dB
	Input 1dB Compression			–1		dBm
	Input 3rd Order Intercept	Two Tone Test, Δf = 2MHz		8		dBm
Mixer: EN = 1.35V, GS = 1.35V						
	Conversion Gain			5		dB
	SSB Noise Figure	Terminated 50Ω Source		9.5		dB
	Input P1dB			–11		dBm
	Input 3rd Order Intercept	Two Tone Test, Δf = 2MHz		–2.5		dBm
	LO-IF Isolation			33		dB
	LO-RF Isolation			37		dB
	RF-LO Isolation			32		dB

V_{CC} = 3V DC, T_A = 25°C (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
V_{CC}	Supply Voltage			1.8 to 5.25		V
I_{CC} HG	Rx High Gain Mode	EN = 1.35V, GS = 1.35V		23	33	mA
I_{CC} LG	Rx Low Gain Mode	EN = 1.35V, GS = 0.3V		18	31	mA
I_{CC} Off	Shutdown Current	EN = 0.3V, GS = 0.3V		2	25	µA
I_{EN}	Enable Current	EN = 1.35V (Note 5)		21		µA
I_{GS}	Gain Select Current	GS = 1.35V (Note 6)		21		µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: LO Absolute Maximum Ratings apply for each LO pin separately.

Note 3: Component values listed in Figure 3 for 1.8GHz evaluation board were used to guarantee 1.8GHz performance.

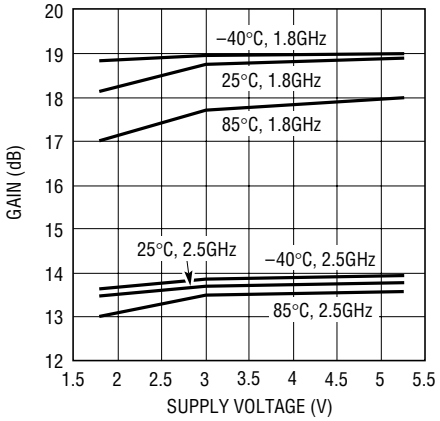
Note 4: Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 5: When EN ≤ 0.3V, enable current is <10µA.

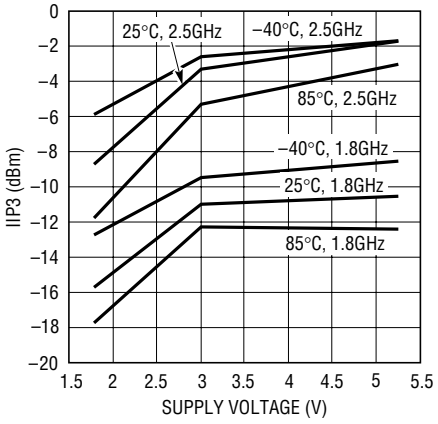
Note 6: When GS ≤ 0.3V, gain select current is <10µA.

TYPICAL PERFORMANCE CHARACTERISTICS

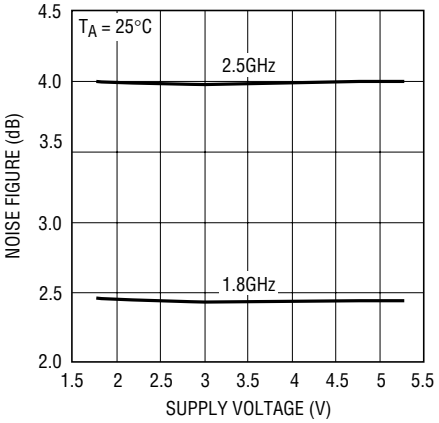
LNA Gain vs Supply Voltage and Temperature (High Gain Mode)



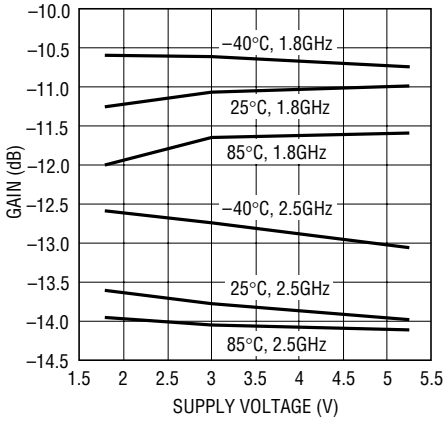
LNA IIP3 vs Supply Voltage and Temperature (High Gain Mode)



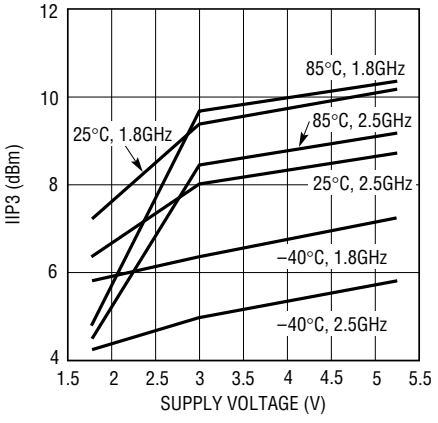
LNA Noise Figure vs Supply Voltage (High Gain Mode)



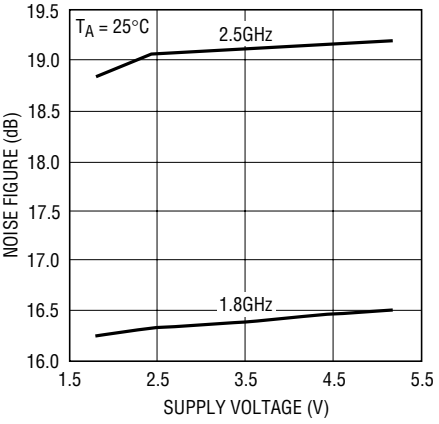
LNA Gain vs Supply Voltage and Temperature (Low Gain Mode)



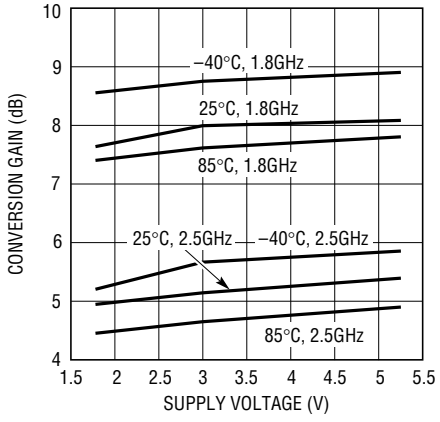
LNA IIP3 vs Supply Voltage and Temperature (Low Gain Mode)



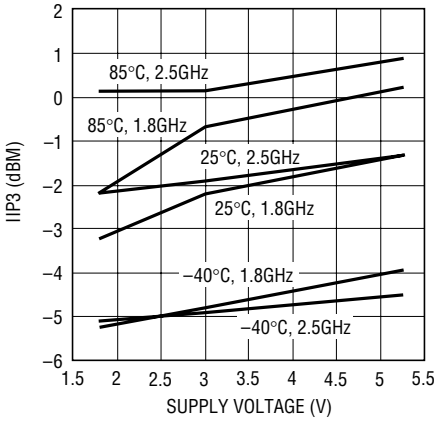
LNA Noise Figure vs Supply Voltage (Low Gain Mode)



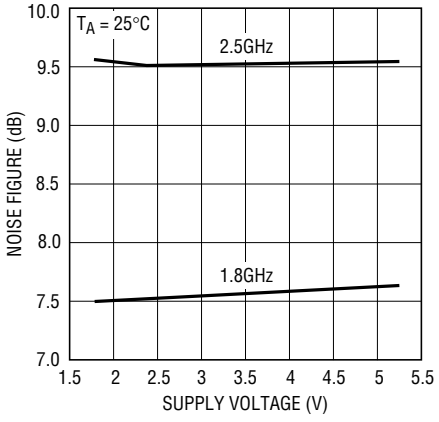
Mixer Conversion Gain vs Supply Voltage and Temperature



Mixer IIP3 vs Supply Voltage and Temperature

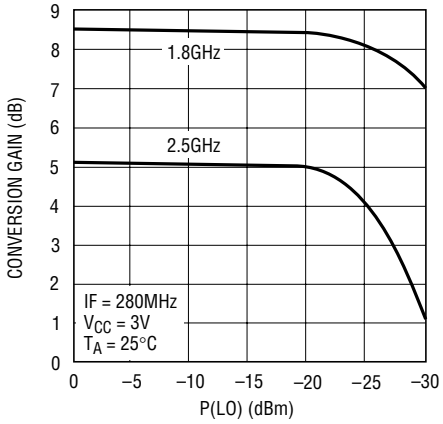


Mixer SSB Noise Figure vs Supply Voltage

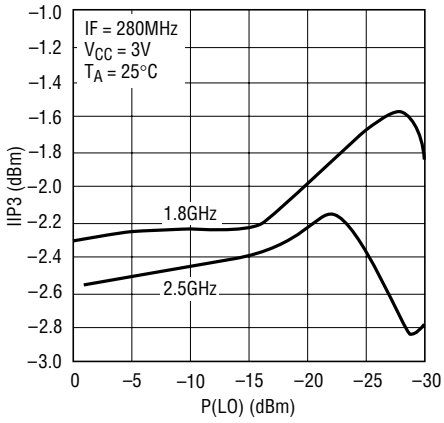


TYPICAL PERFORMANCE CHARACTERISTICS

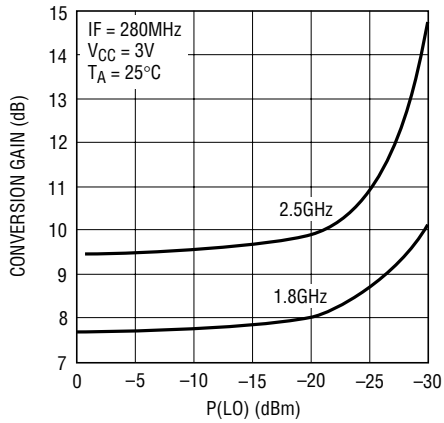
Mixer Conversion Gain vs LO Power



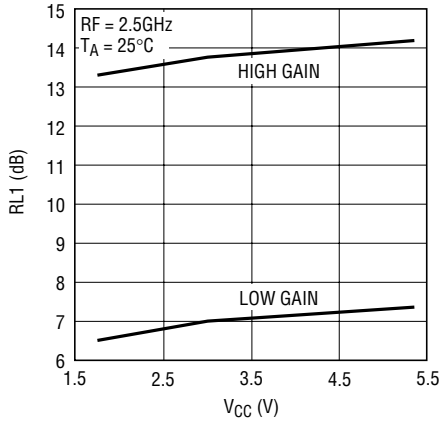
Mixer IIP3 vs LO Power



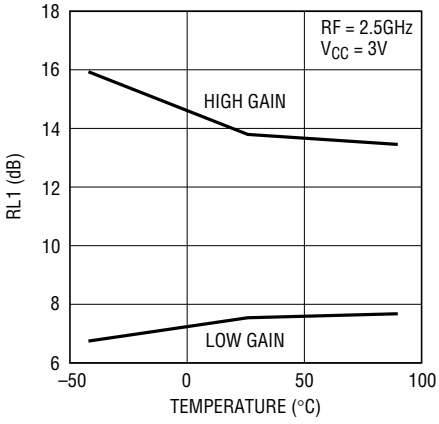
Mixer SSB Noise Figure vs LO Power



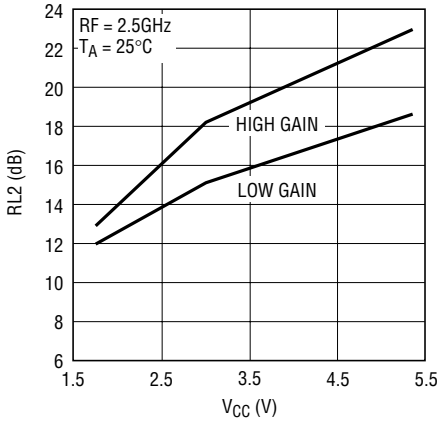
LNA Input Return Loss vs Supply Voltage



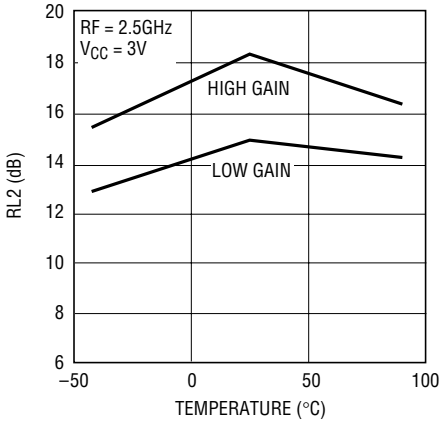
LNA Input Return Loss vs Temperature



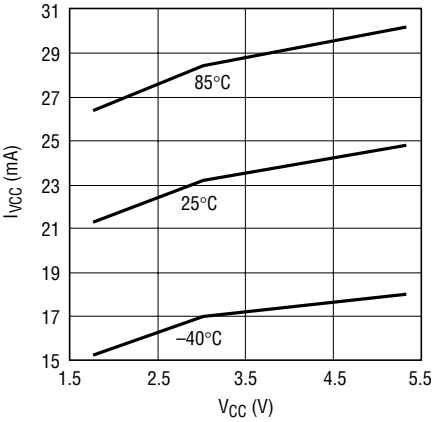
LNA Output Return Loss vs Supply Voltage



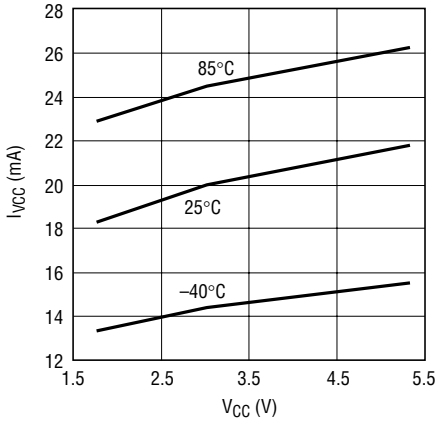
LNA Output Return Loss vs Temperature



I_{VCC} vs Supply Voltage (High Gain Mode)



I_{VCC} vs Supply Voltage (Low Gain Mode)



PIN FUNCTIONS

EN (Pin 1): Enable Pin. A voltage less than 0.3V (Logic Low) disables the part. An input greater than 1.35V (Logic High) enables the part. This pin should be bypassed to ground with a 100pF capacitor. To shut down the part, this pin and GS (Pin 24) must be logic low. Voltage on this pin should not exceed V_{CC} nor fall below ground.

V_{CC} (Pins 2, 9, 17, 21): Power Supply Pins. See Figure 6 for recommended power supply bypassing.

LNA_IN (Pin 3): LNA Input Pin. The LT5500 has better than 10dB input return loss from 1.8GHz to 2.7GHz. This pin is internally biased to 0.8V and must be AC coupled.

GND (Pin 4, 11, 14, 16, 20, 23): Ground Pins. These pins should be connected directly to ground.

LNA_GND (Pins 5, 6, 7, 8): LNA Ground Pins. These pins control the gain of the LNA. At higher frequencies, these pins must be connected directly to ground to maximize the gain.

MIX_GND (Pin 10): Mixer Ground Pin. To optimize the performance of the mixer, a 4.7nH inductor to ground is required for this pin.

IF^+, IF^- (Pins 12, 13): Intermediate Frequency (IF) Mixer Output Pins. These pins must be inductively tied to V_{CC}. The output can be taken differentially or transformed into a single ended output, depending on user preference and performance requirements.

MIX_IN (Pin 15): Mixer RF Input. This pin is internally biased to 0.83V and must be AC coupled. An external matching network is necessary to match to a 50Ω system.

LO^+, LO^- (Pins 18, 19): LO Input Pins. These pins are used to provide the LO drive to the mixer. The signal can be provided either single ended or differentially. These pins are internally biased to V_{CC} – 0.2V and must be AC coupled.

LNA_OUT (Pin 22): The Output Pin for the LNA. An external matching network is necessary to match to a 50Ω system. This pin must be DC coupled to the power supply.

GS (Pin 24): Gain Select Pin. This pin is used to select between high gain and low gain modes. High gain mode is selected when an input voltage greater than 1.35V (Logic High) is applied to this pin. Low gain mode is selected when the applied voltage is less than 0.3V (Logic Low). This pin should be bypassed to ground with a 100pF capacitor. To shut down the part, this pin must be logic low. Voltage on this pin should not exceed V_{CC} nor fall below ground.

BLOCK DIAGRAM

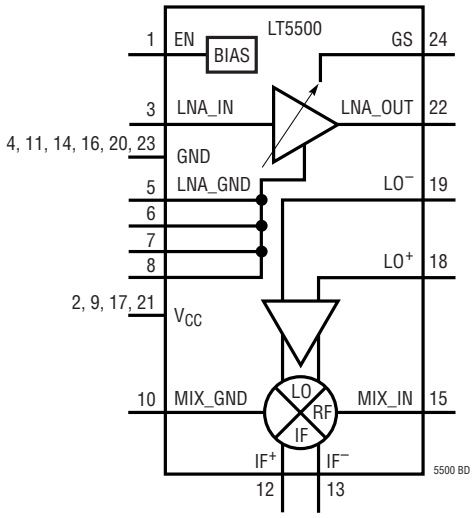


Figure 2. LT5500 Block Diagram

APPLICATIONS INFORMATION

The LT5500 consists of an LNA, a Mixer, an LO buffer and the associated bias circuitry. The chip is designed to be compatible with IEEE802.11b wireless local area network (WLAN), MMDS and other wireless applications. The LNA and Mixer are designed to operate over an input frequency range of 1.8GHz to 2.7GHz with a supply voltage of 1.8V to 5.25V. The Mixer IF output frequency range is 200MHz to 450MHz. The typical LO drive is –10dBm. The LO buffer operation is broadband.

LNA

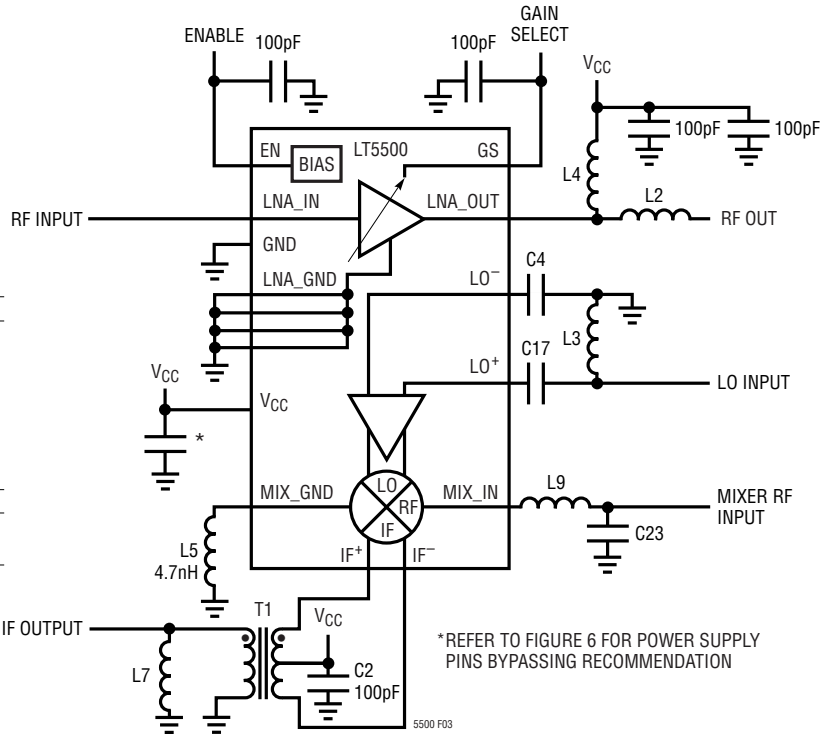
The LNA has two modes of operation: high gain and low gain. In the high gain mode, the LNA is a cascode amplifier. Package inductance is used to achieve better than 10dB input return loss over the entire frequency range. The input of the LNA must be AC coupled. The linearity of the high gain mode of the LNA can be increased by adding inductance to LNA_GND. This will reduce the gain and improve input return loss while having little impact on the low gain mode. In low gain mode, the LNA uses a capacitively coupled diode and a resistively degenerated cascode to attenuate the incoming signal and maintain a moderate VSWR. The LNA output is an open collector, and the matching circuit requires a shunt inductor connected to the power supply to provide the bias current. The component configuration for matching and example component values are listed in Figure 3. If it is desirable to reduce the gain further and simultaneously broaden the LNA bandwidth, an additional shunt resistor to the power supply can be added to the output to reduce the output quality factor (Q).

The LT5500 is designed to allow an interstage bandpass filter to be introduced between the output of the LNA and the input of the Mixer. If such an interstage filter is unnecessary, the output of the LNA can be connected to the Mixer input through a blocking capacitor and small value resistor.

Mixer

The Mixer consists of a single-ended input differential pair followed by a double-balanced mixer cell. The input matching configuration for the Mixer is shown in Figure 3. The Mixer uses a 4.7nH external inductance to act as a high frequency current source at the MIX_GND pin. Example component values for matching the mixer input are tabulated in Figure 3.

APPLICATIONS INFORMATION



APPLICATION DEPENDENT COMPONENT VALUES

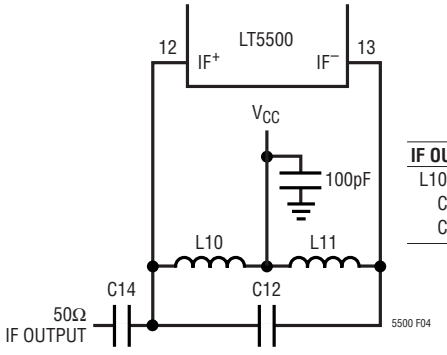
RF INPUT	1.8GHz	2.5GHz
L4	4.7nH	2.7nH
L2	12nH	4.7nH
L3	4.7nH	1.8nH
C4	220pF	220pF
C17	10pF	10pF
L9	5.6nH	2.7nH
C23	1.8pF	1.5pF
280MHz IF OUTPUT		
L7	15nH	
T1	TC8-1 MINI-CIRCUITS	

Figure 3. Simplified Test Schematic for 1.8GHz and 2.5GHz Applications

An IF transformer can be used to create a single-ended output. The additional discrete components necessary to achieve a 50Ω match are tabulated in Figure 3. Alternatively, the discrete solution shown in Figure 4 can be used to perform differential to single-ended conversion. For best LO and RF signal suppression at the IF output, a transformer should be used. If it is desirable to reduce the gain of the mixer, a resistor between the IF outputs can be used.

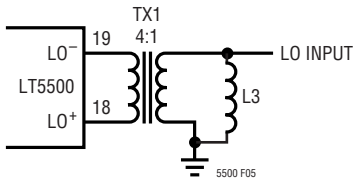
LO Buffer

The LO inputs can be driven either differentially or single ended. A single-ended configuration is shown along with example component values in Figure 3. Optionally, the LO can be driven differentially as shown in Figure 5.



IF OUTPUT	280MHz
L10, L11	27nH
C12	3.3pF
C14	2.2pF

Figure 4. Alternative Mixer IF Output Matching



LO INPUT	2.22GHz
L3	3.3µH
TX1	TOKO-BF4

Figure 5. Optional Transformer-Based Differential LO Drive

APPLICATIONS INFORMATION

Modes of Operation

The LT5500 has three operating modes:

1. Shutdown

2. LNA High Gain

3. LNA Low Gain

For shutdown, the EN pin and the GS pin must be at logic Low. Logic Low is defined as a control voltage below 0.3V. LNA High gain mode requires that both EN and GS pins be at logic High. Logic High is defined as a control voltage above 1.35V. LNA Low gain mode requires that the EN pin be at logic High and that the GS pin be at logic Low. Mixer operation is independent of the GS pin. The Mixer is enabled when the EN pin is at logic High.

Table 1: Mode Selection

EN	GS	LNA	MIXER
High	High	High Gain	On
High	Low	Low Gain	On
Low	Low	Shutdown	Shutdown

Evaluation Board

Figure 6 shows the circuit schematic of the evaluation board. Each signal terminal of the evaluation board has provisions for three matching components in a T-formation. In practice, two or fewer components are needed to achieve the match. In the case of the LNA input, no external components are necessary if the band select filter provides the necessary AC coupling. Otherwise AC coupling must be provided. A similar consideration applies to the Mixer input pin. The LO terminal of the evaluation board was designed to permit evaluation of both single ended and differential matching configurations. The differential configuration anticipates the use of a transformer. Similarly, the IF output board layout was designed to permit evaluation of both transformer based and discrete component based matching.

The evaluation board employs primarily 0402 surface mount components, particularly near the signal paths. All surface mount inductors must have a high self-resonance frequency. The component values necessary for 1.8GHz and 2.5GHz applications are tabulated in Figure 3.

RF Layout Tips

- Use 50Ω impedance transmission lines up to the matching networks. Use of ground planes is a must, particularly beneath the IC.
- Keep the matching networks as close to the pins as possible.
- Surface mount 0402 outline (or smaller) parts are recommended to minimize parasitic capacitances and inductances.
- Improve LO isolation and maximize component density by putting the LO signal trace on the bottom of the board. This permits either the matching components or an interstage filter to be placed directly between the LNA output and the Mixer input.
- Place bypass capacitors to ground in close proximity to the pull-up inductors on the LNA and Mixer outputs to improve component behavior and assure a good small-signal ground.
- V_{CC} lines must be decoupled with low impedance, broadband capacitors to prevent instability. The capacitors should be placed as close as possible to the V_{CC} pins.
- Avoid use of long traces whenever possible. Long RF traces in particular lead to signal radiation, degraded isolation and higher losses.

APPLICATIONS INFORMATION

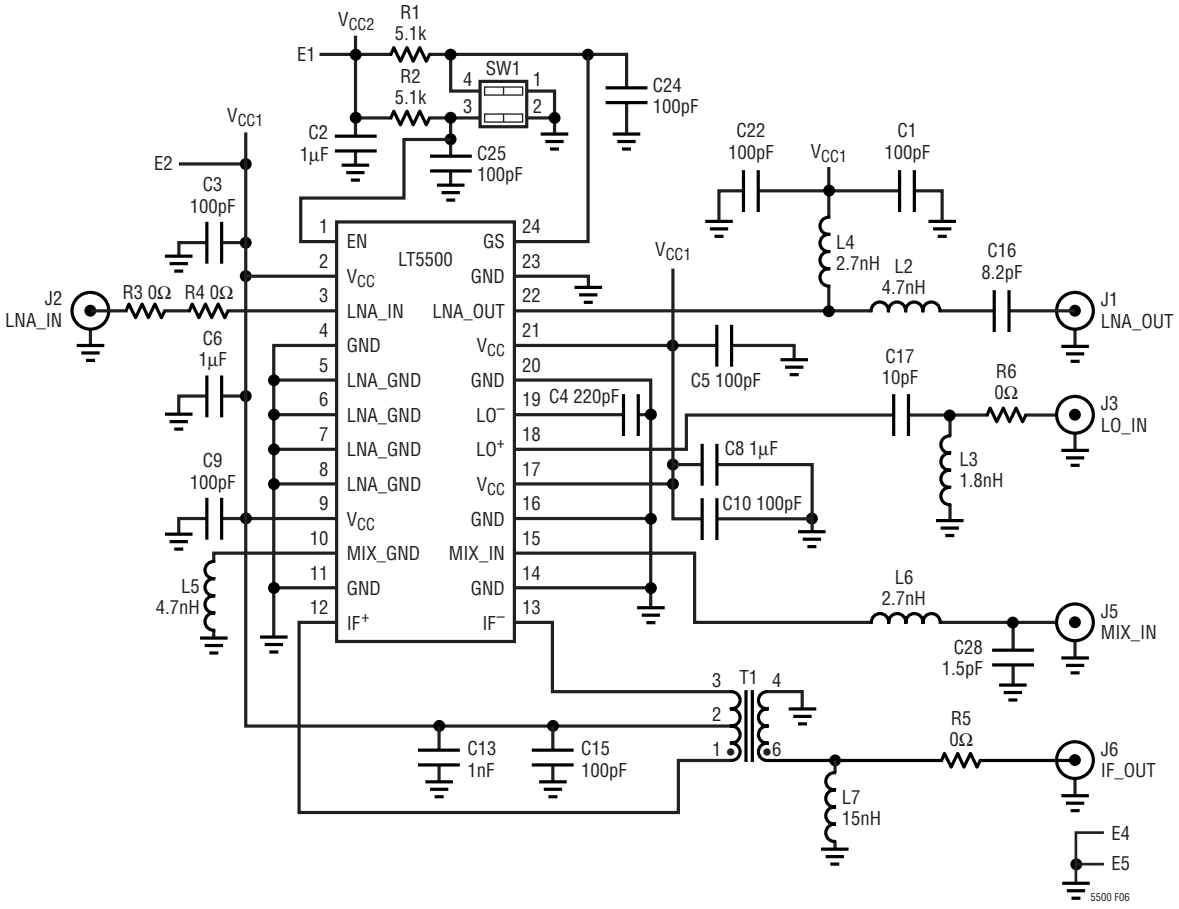


Figure 6. 2.5GHz Evaluation Circuit Schematic

APPLICATIONS INFORMATION

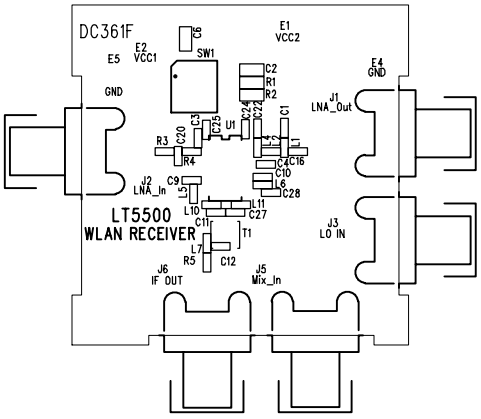


Figure 7. Component Side Silkscreen of Evaluation Board

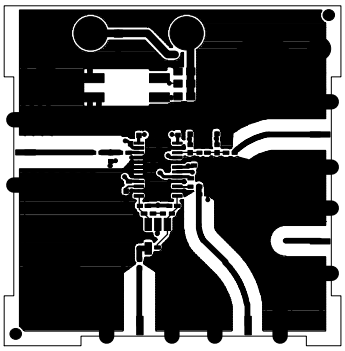


Figure 8. Component Side Layout of Evaluation Board

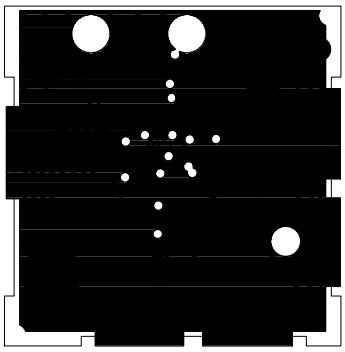


Figure 9. RF Ground (Layer 2) Layout of Evaluation Board

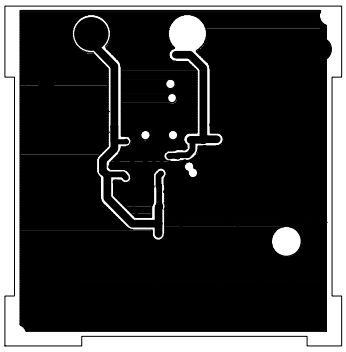


Figure 10. Routing (Layer 3) Layout of Evaluation Board

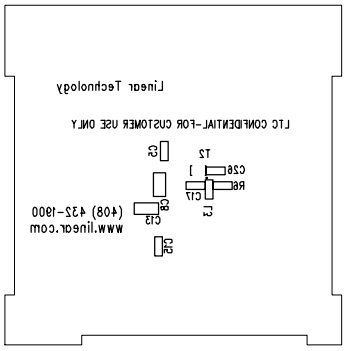


Figure 11. Bottom Side Silkscreen of Evaluation Board

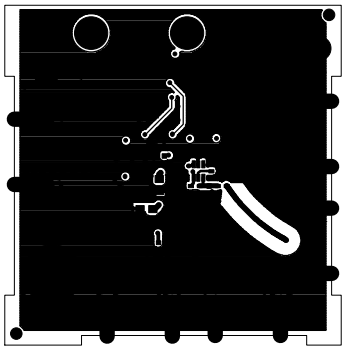
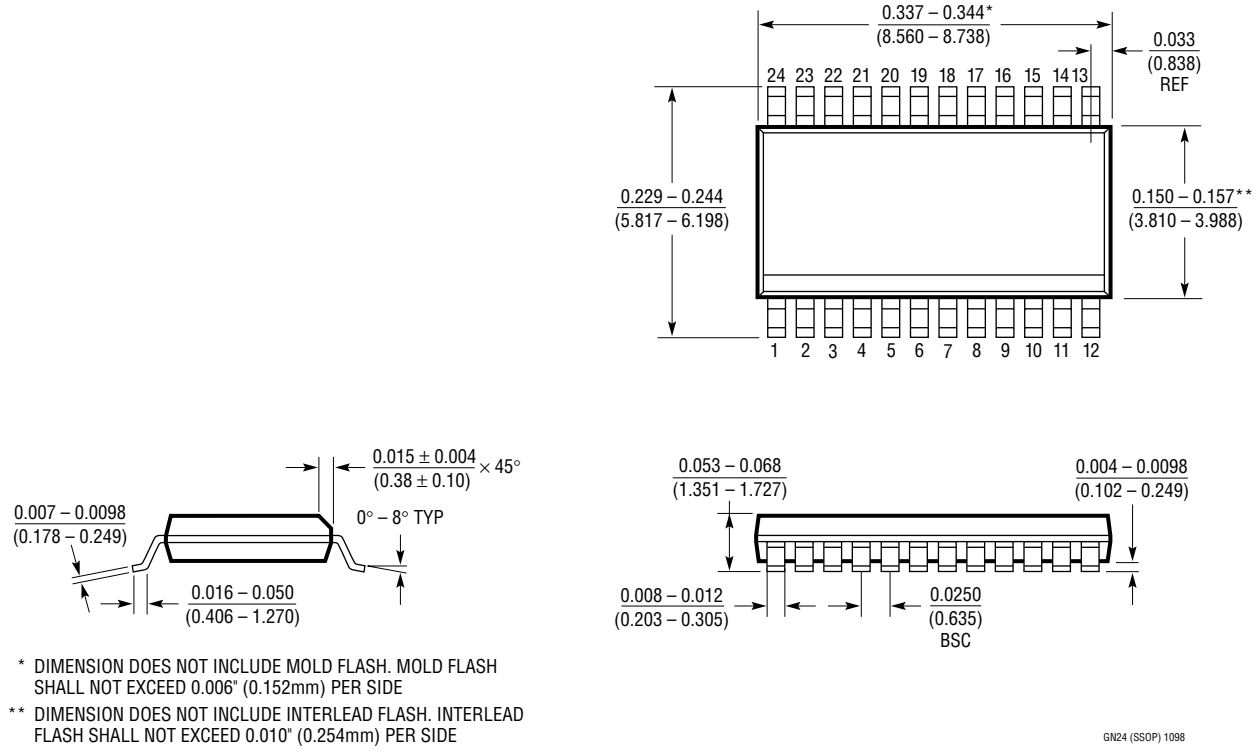


Figure 12. Bottom Side Layout of Evaluation Board

PACKAGE DESCRIPTION

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN24 (SSOP) 1098

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT5502	400MHz Quadrature IF Demodulator with RSSI	1.8V to 5.25V Operation
LT5503	1.2GHz to 2.7GHz Direct IQ Modulator and Mixer	1.8V to 5.25V Operation
LTC5505	ThinSOT™ RF Power Detector with Buffered Output and >40dB Dynamic Range	300MHz to 3GHz, Temperature Compensated, LTC5505-1: –28dBm to 18dBm, LTC5505-2: –32dBm to 12dBm, V_{CC} = 2.7V to 6V

ThinSOT is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT/TP 1201 1.5K • PRINTED IN USA