HB526A164DB Series

524,288-word × 64-bit × 2-bank Synchronous Dynamic RAM Module

HITACHI

ADE-203-606 (Z)
Preliminary
Rev. 0.0
Jun. 18, 1996

Description

The HB526A164DB is a 512k × 64× 2 banks Synchronous Dynamic RAM Small Outline Dual In-line Memory Module (S.O.DIMM), mounted 4 pieces of 16-Mbit SDRAM (HM5216165TT) sealed in TSOP package and 1 piece of serial EEPROM (24C02) for Presence Detect (PD). An outline of the HB526A164DB is 144-pin Zig Zag Dual tabs socket type compact and thin package. Therefore, the HB526A164DB makes high density mounting possible without surface mount technology. The HB526A164DB provides common data inputs and outputs. Decoupling capacitors are mounted beside TSOP on the module board.

Features

- 144-pin Zig Zag Dual tabs socket type
  - — Outline: 67.60 mm (Length) × 25.40 mm (Height) × 3.80 mm (Thickness)
  - — Lead pitch : 0.80 mm
- 3.3V power supply
- Clock frequency : 100 MHz / 83 MHz / 66 MHz
- LVTTL interface
- 2 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length : 1/2/4/8/full page
- Programmable burst sequence
  - — Sequential/interleave
- Full page burst length capability
  - — Sequential burst
  - — Burst stop capability
- Programmable $\overline{\text{CAS}}$ latency : 2/3

Preliminary:The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regrding specification.

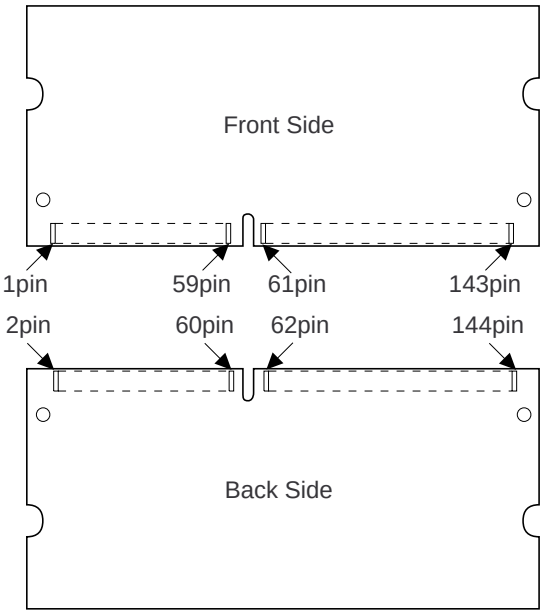
Hitachi semiconductor

- Byte control by DQMB
- 4096 refresh cycles: 64 ms
- 2 variations of refresh
  - — Auto refresh
  - — Self refresh

Ordering Information

Type No.	Frequency	Package	Contact pad
HB526A164DB-10	100 MHz	Small outline DIMM (144-pin)	Gold
HB526A164DB-12	83 MHz		
HB526A164DB-15	66 MHz		

Pin Arrangement



Pin Arrangement (cont.)

Front side				Back side			
Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	V_{SS}	73	NC	2	V_{SS}	74	NC
3	DQ0	75	V_{SS}	4	DQ32	76	V_{SS}
5	DQ1	77	NC	6	DQ33	78	NC
7	DQ2	79	NC	8	DQ34	80	NC
9	DQ3	81	V_{DD}	10	DQ35	82	V_{DD}
11	V_{DD}	83	DQ16	12	V_{DD}	84	DQ48
13	DQ4	85	DQ17	14	DQ36	86	DQ49
15	DQ5	87	DQ18	16	DQ37	88	DQ50
17	DQ6	89	DQ19	18	DQ38	90	DQ51
19	DQ7	91	V_{SS}	20	DQ39	92	V_{SS}
21	V_{SS}	93	DQ20	22	V_{SS}	94	DQ52
23	DQMB0	95	DQ21	24	DQMB4	96	DQ53
25	DQMB1	97	DQ22	26	DQMB5	98	DQ54
27	V_{DD}	99	DQ23	28	V_{DD}	100	DQ55
29	A0	101	V_{DD}	30	A3	102	V_{DD}
31	A1	103	A6	32	A4	104	A7
33	A2	105	A8	34	A5	106	A11 (BS)
35	V_{SS}	107	V_{SS}	36	V_{SS}	108	V_{SS}
37	DQ8	109	A9	38	DQ40	110	NC
39	DQ9	111	A10 (AP)	40	DQ41	112	NC
41	DQ10	113	V_{DD}	42	DQ42	114	V_{DD}
43	DQ11	115	DQMB2	44	DQ43	116	DQMB6
45	V_{DD}	117	DQMB3	46	V_{DD}	118	DQMB7
47	DQ12	119	V_{SS}	48	DQ44	120	V_{SS}
49	DQ13	121	DQ24	50	DQ45	122	DQ56
51	DQ14	123	DQ25	52	DQ46	124	DQ57
53	DQ15	125	DQ26	54	DQ47	126	DQ58
55	V_{SS}	127	DQ27	56	V_{SS}	128	DQ59
57	NC	129	V_{DD}	58	NC	130	V_{DD}
59	NC	131	DQ28	60	NC	132	DQ60
61	CK0	133	DQ29	62	CKE0	134	DQ61
63	V_{DD}	135	DQ30	64	V_{DD}	136	DQ62
65	$\overline{RAS}$	137	DQ31	66	$\overline{CAS}$	138	DQ63

Pin Arrangement (cont.)

Front side				Back side			
Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
67	$\overline{WE}$	139	V_{SS}	68	NC	140	V_{SS}
69	$\overline{S0}$	141	SDA	70	NC	142	SCL
71	NC	143	V_{DD}	72	NC	144	V_{DD}

Pin Description

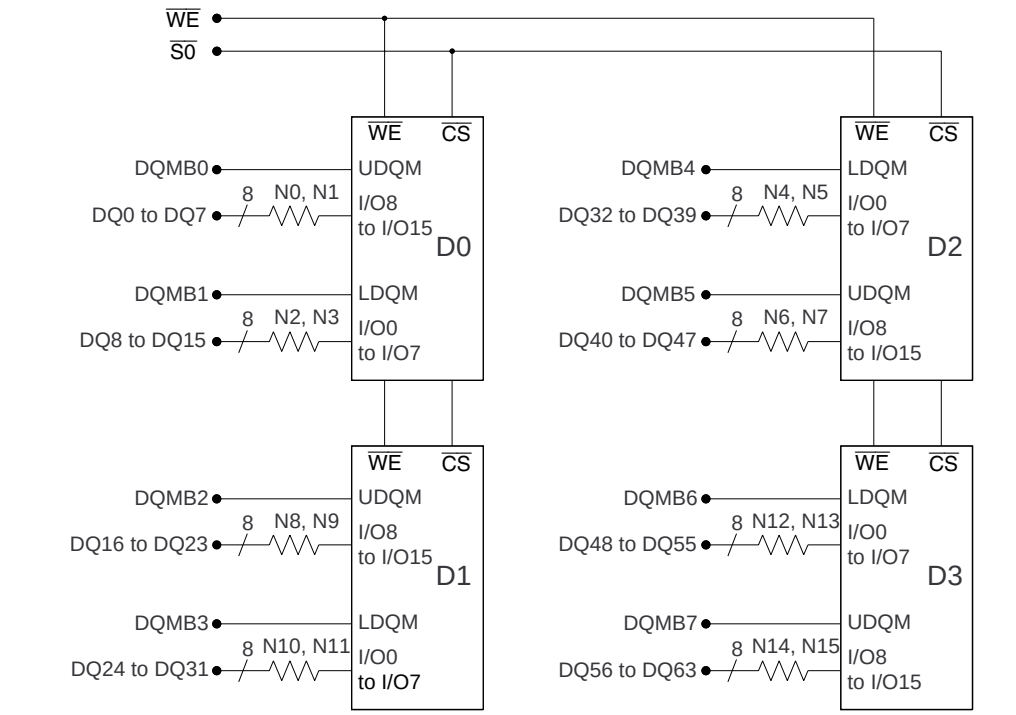
Pin name	Function
A0 to A11	Address input — Row address A0 to A10 — Column address A0 to A7 — Bank select address A11
DQ0 to DQ63	Data-input/output
$\overline{S0}$	Chip select
$\overline{RAS}$	Row address asserted bank enable
$\overline{CAS}$	Column address asserted
$\overline{WE}$	Write enable
DQMB0 to DQMB7	Byte input/output mask
CK0	Clock input
CKE0	Clock enable
SDA	Data-input/output for serial PD
SCL	Clock input for serial PD
V_{DD}	Power supply
V_{SS}	Ground
NC	No connection

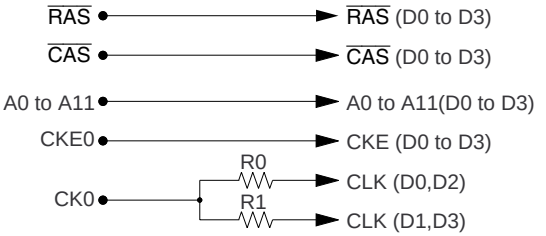
Serial PD Matrix

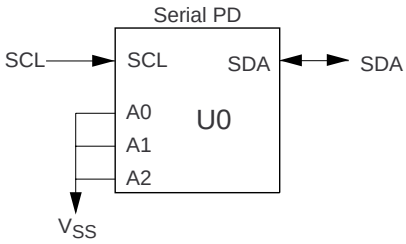
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Notes
0	Number of bytes utilized by module manufacturer	0	0	0	1	0	1	0	1	21
1	Total number bytes in serial PD device	0	0	0	0	1	0	0	0	256byte
2	Memory type	0	0	0	0	0	1	0	0	SDRAM
3	Number of row addresses	0	0	0	0	1	0	1	1	11
4	Number of column addresses	0	0	0	0	1	0	0	0	8
5	Number of DIMM banks	0	0	0	0	0	0	0	1	1
6	Module data width	0	1	0	0	0	0	0	0	64
7	Module data width(continued	0	0	0	0	0	0	0	0	0 (+)
8	Module supply voltage/interface levels	0	0	0	0	0	0	0	1	3.3 V
9	System clock cycle time									
	10 ns	1	0	1	0	0	0	0	0	CL = 3
	12 ns	1	1	0	0	0	0	0	0	
	15 ns	1	1	1	1	0	0	0	0	
10	Access time from clock									
	8 ns	1	0	0	0	0	0	0	0	CL = 3
	9.5 ns	1	0	1	0	0	1	0	1	
	12 ns	1	1	0	0	0	0	0	0	
11	SDRAM DIMM configuration type	0	0	0	0	0	0	0	0	None
12	Refresh rate/type	1	0	0	0	0	0	0	0	Normal (15.625 µs) Self refresh
13	SDRAM module attributes	0	0	0	0	0	0	0	0	
14	SDRAM device attributes: General	0	0	0	0	1	1	1	0	
15	SDRAM device attributes: minimum clock delay, back-to-back random column addresses	0	0	0	0	0	0	0	1	1
16	SDRAM device attributes: Burst lengths supported	1	0	0	0	1	1	1	1	1, 2, 4, 8, full page
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	0	1	0	2
18	SDRAM device attributes: $\overline{\text{CAS}}$ latency	0	0	0	0	0	1	1	0	2, 3
19	SDRAM device attributes: $\overline{\text{S0}}$ latency	0	0	0	0	0	0	0	1	0
20	SDRAM device attributes: $\overline{\text{WE}}$ latency	0	0	0	0	0	0	0	1	0

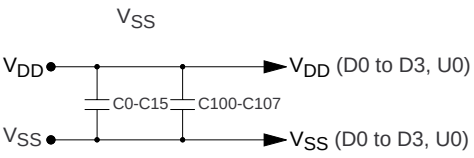
Note: 0: Serial data, “driven Low”, 1: Serial data, “driven High”

Block Diagram









* D0 to D3 : HM5216165TT
U0 : 24C02
C0 to C7 : 0.33 µF
C100 to C107 : 0.1 µF
N0 to N15 : Network Resistors
R0, R1 : Chip Resistors

Notes :

1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{DD}	–1.0 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	4	W	
Operating temperature	Topr	0 to +65	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. V_{IH} (max) = 5.75 V for pulse width ≤ 5 ns.

Recommended DC Operating Conditions (Ta = 0 to +65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{DD}	3.0	3.3	3.6	V	1
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.0	—	4.6	V	1, 2
Input low voltage	V_{IL}	–0.3	—	0.8	V	1, 3

Notes: 1. All voltage referred to V_{SS}
2. V_{IH} (max) = 5.5 V for pulse width ≤ 5 ns
3. V_{IL} (min) = –1.0 V for pulse width ≤ 5 ns

DC Characteristics (Ta = 0 to 65°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB526A164DB								
		-10		-12		-15				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	520	—	420	—	340	mA	Burst length = 1 t_{RC} = min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	—	12	—	12	—	12	mA	CKE0 = V_{IL}, t_{CK} = min	5
		—	8	—	8	—	8	mA	CKE0 = V_{IL} CK0 = V_{IL} or V_{IH} Fixed	6
		—	200	—	164	—	132	mA	CKE0 = V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	28	—	28	—	28	mA	CKE0 = V_{IL}, t_{CK} = min, DQ = High-Z	1, 2
		—	204	—	172	—	136	mA	CKE0 = V_{IH}, NOP command t_{CK} = min, DQ = High-Z	1, 2, 3
Burst operating current ($\overline{CAS}$ Latency = 2)	I_{CC4}	—	400	—	340	—	260	mA	t_{CK} = min, BL = 4	1, 2, 4
($\overline{CAS}$ Latency = 3)	I_{CC4}	—	600	—	500	—	400	mA		
Refresh current	I_{CC5}	—	340	—	280	—	240	mA	t_{RC} = min	
Self refresh current	I_{CC6}	—	8	—	8	—	8	mA	$V_{IH} \geq V_{DD} - 0.2$ $V_{IL} \leq 0.2$ V	7
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	$0 \leq Vin \leq V_{DD}$	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	$0 \leq Vout \leq V_{DD}$ DQ = disable	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CK0 cycles.
4. Input signal transition is once per one CK0 cycle.
5. After power down mode, CK0 operating current.
6. After power down mode, no CK0 operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25°C, V_{DD} = 3.3 V ± 0.3 V)

Parameter	Symbol	Max	Unit	Notes
Input capacitance (Address)	C_{IN}	40	pF	1, 3
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CK0, CKE0)	C_{IN}	40	pF	1, 3
Input capacitance ($\overline{S0}$)	C_{IN}	40	pF	1, 3
Input capacitance (DQMB0 to DQMB7)	C_{IN}	25	pF	1, 2, 3
Input/Output capacitance (DQ0 to DQ63)	$C_{I/O}$	20	pF	1, 3

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

		HB526A164DB							
		-10		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
System clock cycle time ($\overline{CAS}$ Latency = 2)	t_{CK}	15	—	18	—	22.5	—	ns	1
($\overline{CAS}$ Latency = 3)	t_{CK}	10	—	12	—	15	—		
CK0 high pulse width	t_{CKH}	3	—	4	—	5	—	ns	1
CK0 low pulse width	t_{CKL}	3	—	4	—	5	—	ns	1
Access time from CK0 ($\overline{CAS}$ Latency = 2)	t_{AC}	—	9.5	—	12	—	17	ns	1, 2
($\overline{CAS}$ Latency = 3)	t_{AC}	—	8	—	9.5	—	12		
Data-out hold time	t_{OH}	3	—	3	—	3	—	ns	1, 2
CK0 to Data-out low impedance	t_{LZ}	0	—	0	—	0	—	ns	1, 2, 3
CK0 to Data-out high impedance	t_{HZ}	—	7	—	9	—	11	ns	1, 4
Data-in setup time	t_{DS}	2	—	3	—	3	—	ns	1
Data in hold time	t_{DH}	1	—	1	—	1	—	ns	1
Address setup time	t_{AS}	2	—	3	—	3	—	ns	1
Address hold time	t_{AH}	1	—	1	—	1	—	ns	1
CKE0 setup time	t_{CES}	2	—	3	—	3	—	ns	1, 5
CKE0 setup time for power down exit	t_{CESP}	2	—	3	—	3	—	ns	1
CKE0 hold time	t_{CEH}	1	—	1	—	1	—	ns	1

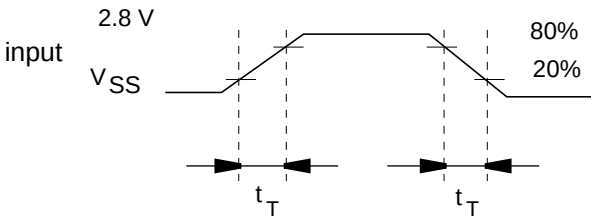
AC Characteristics (Ta = 0 to 65°C, V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (cont)

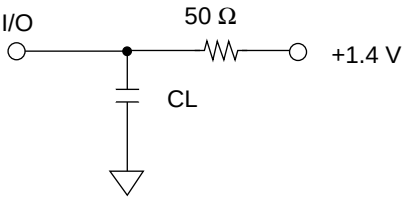
		HB526A164DB							
		-10		-12		-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Command ($\overline{S0}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQMB) setup time	t_{CS}	2	—	3	—	3	—	ns	1
Command ($\overline{S0}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQMB) hold time	t_{CH}	1	—	1	—	1	—	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	—	108	—	135	—	ns	1
Active to precharge command period	t_{RAS}	60	120000	72	120000	90	120000	ns	1
Active to precharge on full page mode	t_{RASC}	—	120000	—	120000	—	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	—	36	—	45	—	ns	1
Precharge to active command period	t_{RP}	30	—	36	—	45	—	ns	1
The last data-in the precharge lead time	t_{RWL}	15	—	18	—	22.5	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	—	24	—	30	—	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	—	64	—	64	—	64	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.40 V.
2. Access time is measured at 1.40 V. Load condition is C_L = 50 pF with current source.
3. t_{LZ} (max) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} defines CKE0 setup time to CKE0 rising edge except power down exit command.

Test Conditions

- Input and output timing reference levels: 1.4 V
- Input waveform and output load: See following figures





Relationship Between Frequency and Minimum Latency

Parameter		HB526A164DB									
		-10			-12			-15			
Frequency (MHz)		100	66	33	83	55	28	66	44	22	
t_{CK} (ns)	Symbol	10	15	30	12	18	36	15	22.5	45	Notes
Active command to column command (same bank)	t_{RCD}	3	2	1	3	2	1	3	2	1	1
Active command to active command (same bank)	t_{RC}	9	6	3	9	6	3	9	6	3	= [t_{RAS} + t_{RP}] 1
Active command to precharge command (same bank)	t_{RAS}	6	4	2	6	4	2	6	4	2	1
Precharge command to active command (same bank)	t_{RP}	3	2	1	3	2	1	3	2	1	1
Last data input to precharge command (same bank)	t_{RWL}	2	1	1	2	1	1	2	1	1	1
Active command to active command (different bank)	t_{RRD}	2	2	1	2	2	1	2	2	1	1
Self refresh exit time	I_{SREX}	2	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)	I_{APW}	5	3	2	5	3	2	5	3	2	= [t_{RWL} + t_{RP}]
Self refresh exit to command input	I_{SEC}	9	6	3	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance ($\overline{CAS}$ latency = 3)	I_{HZP}	3	3	3	3	3	3	3	3	3	
($\overline{CAS}$ latency = 2)	I_{HZP}	—	2	2	—	2	2	—	2	2	
Last data out to active command (auto precharge) (same bank)	I_{APR}	1	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge) ($\overline{CAS}$ latency = 3)	I_{EP}	–2	–2	–2	–2	–2	–2	–2	–2	–2	
($\overline{CAS}$ latency = 2)	I_{EP}	—	–1	–1	—	–1	–1	—	–1	–1	
Column command to column command	I_{CCD}	1	1	1	1	1	1	1	1	1	
Write command to data in latency	I_{WCD}	0	0	0	0	0	0	0	0	0	
DQMB to data in	I_{DID}	0	0	0	0	0	0	0	0	0	
DQMB to data out	I_{DOD}	2	2	2	2	2	2	2	2	2	
CKE0 to CK0 disable	I_{CLE}	1	1	1	1	1	1	1	1	1	

Relationship Between Frequency and Minimum Latency (cont)

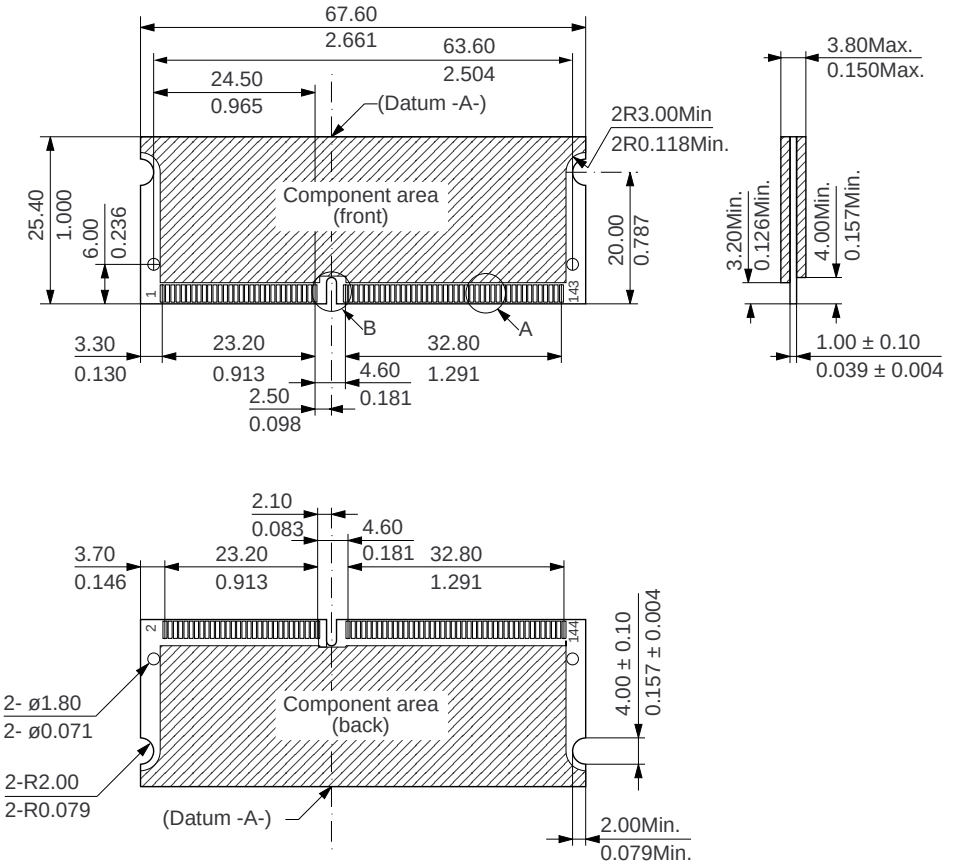
Parameter		HB526A164DB									
		-10			-12			-15			
Frequency (MHz)		**100**	**66**	**33**	**83**	**55**	**28**	**66**	**44**	**22**	
t_{CK} (ns)	**Symbol**	**10**	**15**	**30**	**12**	**18**	**36**	**15**	**22.5**	**45**	**Notes**
Register set to active command	t_{RSA}	1	1	1	1	1	1	1	1	1	
$\overline{S0}$ to command disable	I_{CDD}	0	0	0	0	0	0	0	0	0	
Power down exit to command input	I_{PEC}	1	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold ($\overline{CAS}$ latency = 3)	I_{BSR}	2	2	2	2	2	2	2	2	2	
($\overline{CAS}$ latency = 2)	I_{BSR}	—	1	1	—	1	1	—	1	1	
Burst stop to output high impedance ($\overline{CAS}$ latency = 3)	I_{BSH}	3	3	3	3	3	3	3	3	3	
($\overline{CAS}$ latency = 2)	I_{BSH}	—	2	2	—	2	2	—	2	2	
Burst stop to write data ignore	I_{BSW}	0	0	0	0	0	0	0	0	0	

Notes: 1. t_{RCD} to t_{RRD} are recommended value.
2. When self refresh exit is executed, CKE0 should be kept “H” longer than I_{SREX} from exit cycle.

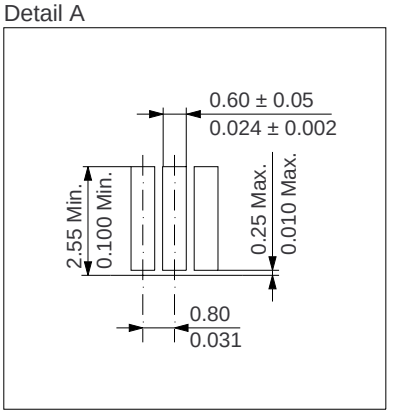
Refer to the HB526C264EN/HB526C464EN Series for the details.

Physical Outline

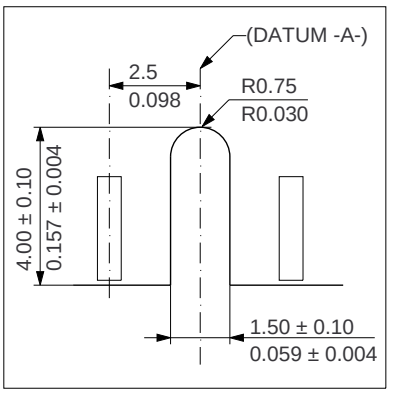
Unit: mm / inch



Detail A



Detail B



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