2SJ451

Silicon P Channel MOS FET

Application

Low frequency power switching

Features

- Low on-resistance.
- Low drive power
- 2.5V gate drive device.
- Small package (MPAK).

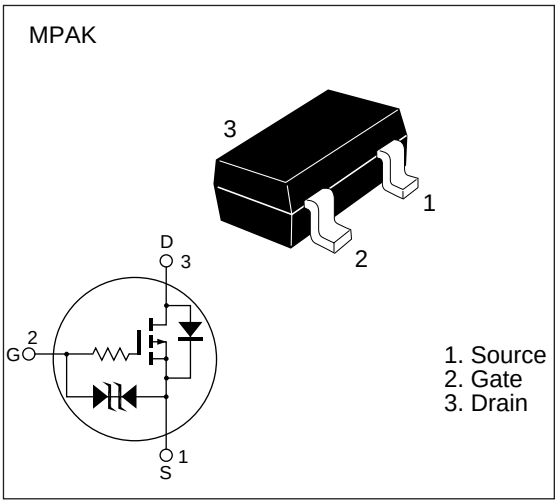


Table 1 Absolute Maximum Ratings (Ta = 25°C)

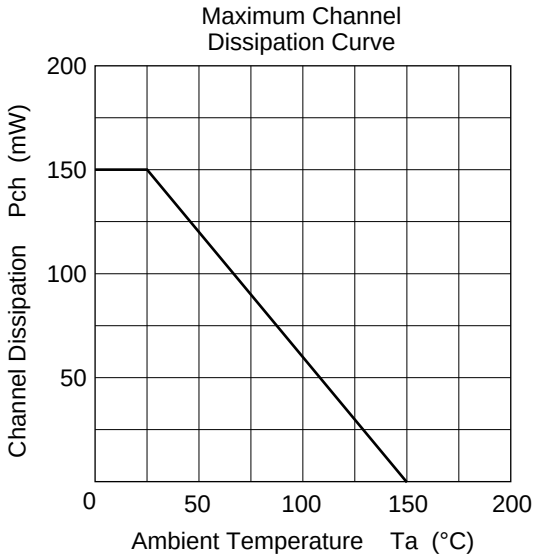
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–20	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	–0.2	A
Drain peak current	$I_{D(pulse)}$*	–0.4	A
Channel dissipation	Pch**	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
Marking is "ZK–".

Table 2 Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–20	—	—	V	I_D = –100 µA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1.0	µA	V_{DS} = –16 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±2.0	µA	V_{GS} = ±16 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.5	—	–1.5	V	I_D = –10 µA, V_{DS} = –5 V
Static drain to source on state resistance	$R_{DS(on)}1$	—	2.3	3.5	Ω	I_D = –100 mA V_{GS} = –4 V *
Static drain to source on state resistance	$R_{DS(on)}2$	—	5.0	9.0	Ω	I_D = –40 mA V_{GS} = –2.5 V *
Foward transfer admittance	$\|y_{fs}\|$	0.13	0.23	—	S	I_D = –100 mA V_{DS} = –10 V
Input capacitance	Ciss	—	2.4	—	pF	V_{DS} = –10 V
Output capacitance	Coss	—	31	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	0.6	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	0.17	—	µs	V_{GS} = –10 V, I_D = –0.1 A
Rise time	t_r	—	0.68	—	µs	R_L = 100 Ω
Turn–off delay time	$t_{d(off)}$	—	3.0	—	µs	
Fall time	t_f	—	2.8	—	µs	

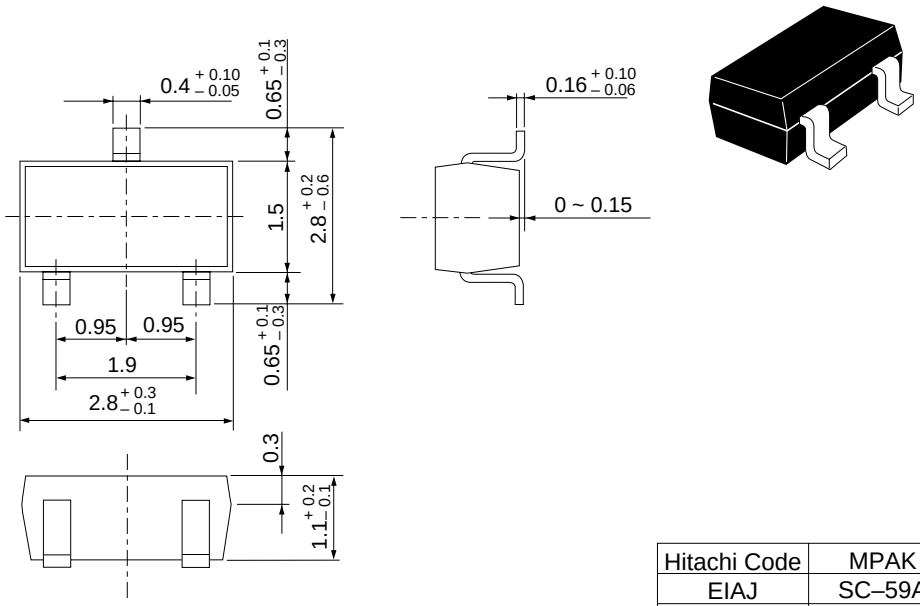
* Pulse Test



Package Dimensions

Unit : mm

• MPAK



Hitachi Code	MPAK
EIAJ	SC–59A
JEDEC	—