



MX23L1010

1M-BIT MASK ROM (8-BIT OUTPUT)

FEATURES

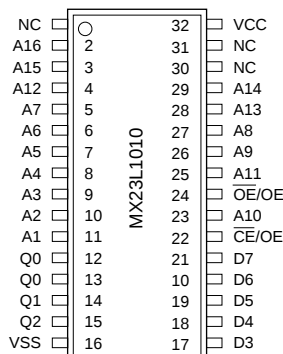
- Bit organization
 - 128K x 8 (byte mode)
- Fast access time
 - Random access: 150ns
- Current
 - Operating: 20mA
 - Standby: 20uA
- Supply voltage
 - 2.7V ~ 3.6V
- Package
 - 32 pin SOP (450 mil)
 - 32 pin TSOP (8mm x 20mm)

ORDER INFORMATION

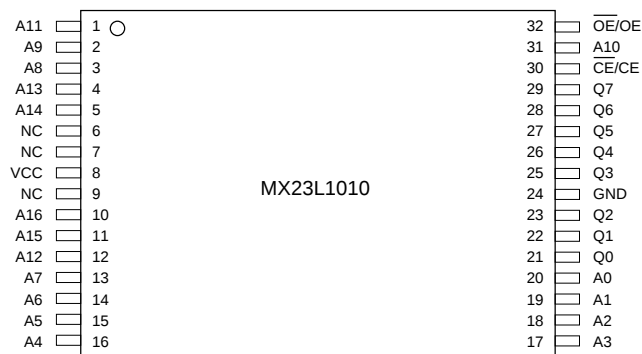
Part No.	Access Time	Package
MX23L1010MI-15	150ns	32 pin SOP (Industrial)
MX23L1010MI-20	200ns	32 pin SOP (Industrial)
MX23L1010TI-15	150ns	32 pin TSOP (Industrial)
MX23L1010TI-20	200ns	32 pin TSOP (Industrial)

PIN CONFIGURATION

32 SOP



32 TSOP



PIN DESCRIPTION

Symbol	Pin Function
A0~A16	Address Inputs
D0~D7	Data Outputs
CE	Chip Enable Input
OE	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	-40°C to 85°C
Storage Temperature	Tstg	-65°C to 125°C

DC CHARACTERISTICS (Ta = -40°C ~ 85°C, VCC = 2.7V ~ 3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	VCC-0.2V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.2V	IOL = 1.6mA
Input High Voltage	VIH	2.0V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.4V	
Input Leakage Current	ILI	-	5uA	VIN = 0 to VCC
Output Leakage Current	ILO	-	5uA	VOUT = 0 to VCC
Operating Current	ICC1	-	20mA	VCC=3V, f = 5MHz
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$ = VIH
Standby Current (CMOS)	ISTB2	-	20uA	$\overline{CE}$ > VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta=25°C, f=1MHz, VIN=0V
Output Capacitance	COUT	-	10pF	Ta=25°C, f=1MHz, VOUT=0V

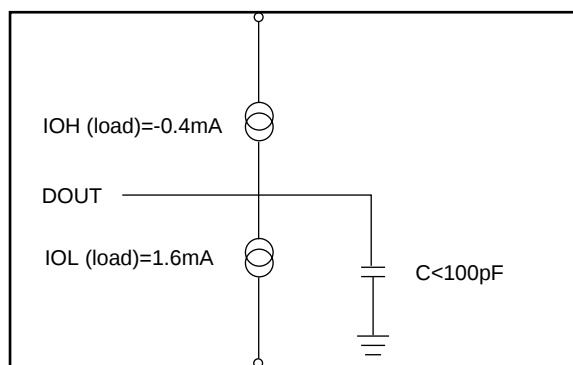
AC CHARACTERISTICS (Ta = -40°C ~ 85°C, VCC = 2.7V ~ 3.6V)

Item	Symbol	23L1010-15		23L1010-20	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	150ns	-	200ns	-
Address Access Time	tAA	-	150ns	-	200ns
Chip Enable Access Time	tACE	-	150ns	-	200ns
Output Enable Time	tOE	-	70ns	-	100ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note :Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



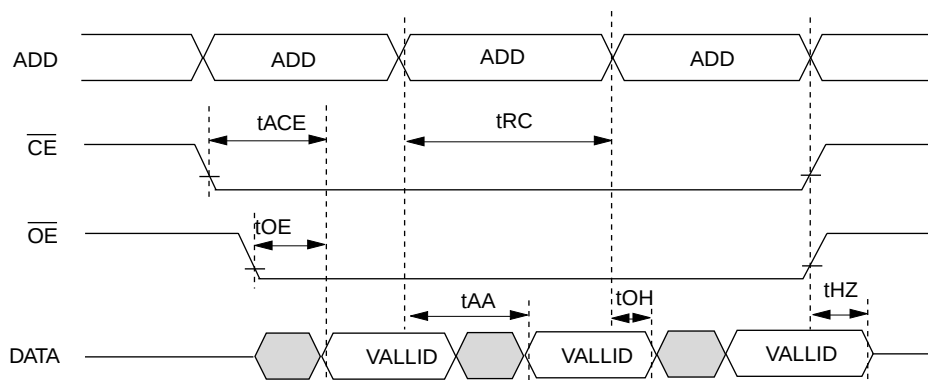
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

RANDOM READ



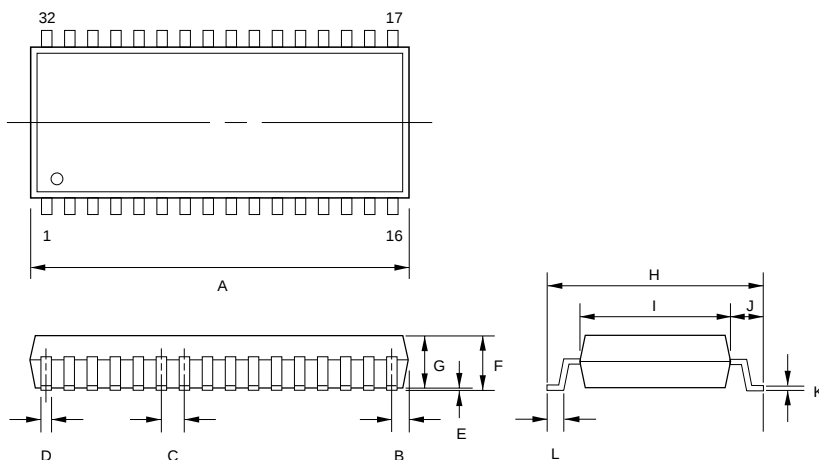
Note : $\overline{CE}$, $\overline{OE}$ are enable.

PACKAGE INFORMATION

32-PIN PLASTIC SOP (450 mil)

ITEM	MILLIMETERS	INCHES
A	20.95 max.	.825 max.
B	1.00 [REF]	.039 [REF]
C	1.27 [TP]	.050 [TP]
D	.40 [Typ.]	.016 [Typ.]
E	.05 min.	.002 min.
F	3.05 max.	.120 max.
G	2.69±.13	.106±.005
H	14.12±.25	.556±.010
I	11.30±.13	.445±.005
J	1.42	.056
K	.20 [Typ.]	.008 [Typ.]
L	.79	.031

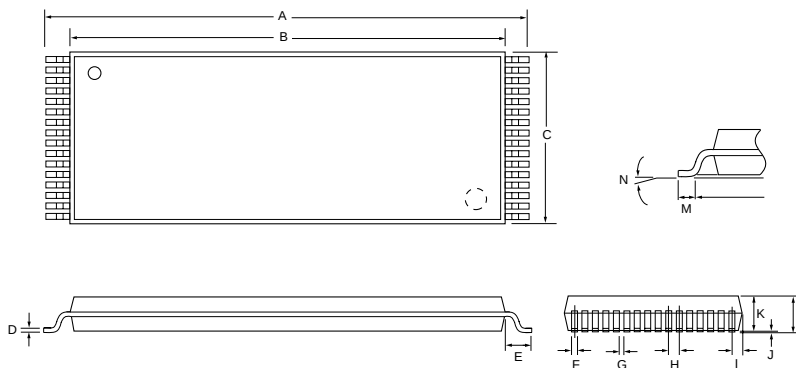
NOTE: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



32-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	20.0±.20	.078±.006
B	18.40±.10	.724±.004
C	8.20 max.	.323 max.
D	.15 [Typ.]	.006 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20±.10	.008±.004
G	.30±.10	.012±.004
H	.50 [Typ.]	.020 [Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00±.10	.039±.004
L	1.27 max.	.050 max.
M	.50	.020
N	0 ~ 5°	.500

NOTE: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.





REVISION HISTORY

Revision	Description	Page	Date
1.4	AC Characteristics: tOH 10ns --> 0ns	P3	FEB/01/1999



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